PanaXSeries

The One to Watch for Constant Innovation-Making the Future Come Alive

MICROCOMPUTER MN101C

MN101C527
LSI User's Manual

Pub.No.21452-034E

Panasonic

PanaX Series is a trademark of Matsushita Electric Industrial Co., Ltd.
The other corporation names, logotype and product names written in this book are trademarks or registered trademarks of their corresponding corporations.

Request for your special attention and precautions in using the technical informaition and semiconductors described in this book

(1) An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this book and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan.

(2) The contents of this book are subject to change without notice in matters of improved function.When finalizing your design, therefore, ask for the most up-to-date version in advance in order to check for any changes.

(3) We are not liable for any damage arising out of the use of the contents of this book, or for any infringement of patents or any other rights owned by a third party.

(4) No part of this book may be reprinted or reproduced by any means without written permission from our company.

(5) This book deals with standard specification. Ask for the latest individual Product Standards or Specifications in advance for more detailsd infomation required for your design, purchasing and applications.

If you have any inquiries or questions about this book or our semiconductors, please contact one of our sales offices listed at the back of this book.

About This Manual

■Organization

In this LSI manual, this LSI functions are presented in the following order : overview, basic CPU functions, interrupt functions, port functions, timer functions, serial functions, and other peripheral hardware functions.

Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.

The layout and definition of each section are shown below.

Subtitle

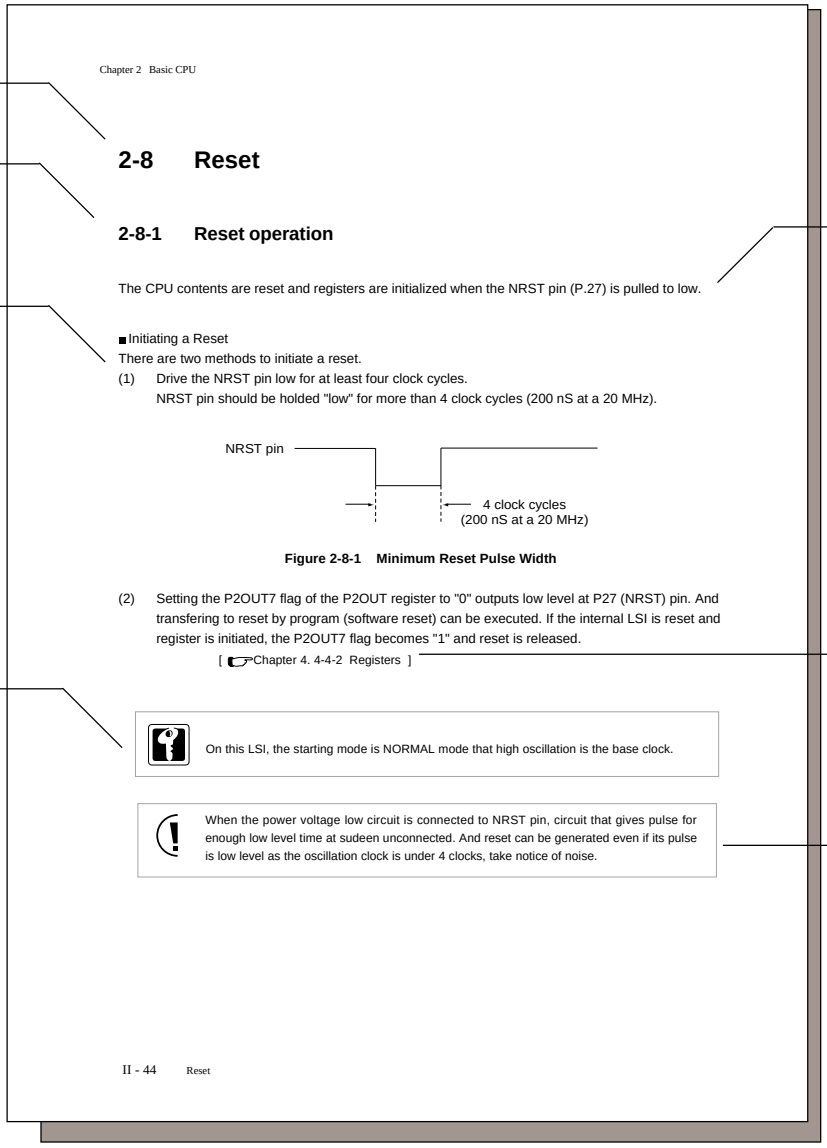
Sub-subtitle

The smallest block in this manual.

Main text

Key information

Important information from the text.



Chapter 2 Basic CPU

2-8 Reset

2-8-1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin (P.27) is pulled to low.

■ Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the NRST pin low for at least four clock cycles.
NRST pin should be holded "low" for more than 4 clock cycles (200 nS at a 20 MHz).

NRST pin

4 clock cycles
(200 nS at a 20 MHz)

Figure 2-8-1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.

[☞Chapter 4. 4-4-2 Registers]

On this LSI, the starting mode is NORMAL mode that high oscillation is the base clock.

When the power voltage low circuit is connected to NRST pin, circuit that gives pulse for enough low level time at sudeen unconnected. And reset can be generated even if its pulse is low level as the oscillation clock is under 4 clocks, take notice of noise.

II - 44 Reset

Summary

Introduction to the section.

References

References for the main text.

Precautions and warnings

Precautions are listed in case.
Be sure to read these of lost functionality or damage.

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.
(2) Consult the table of contents at the front of the manual to locate desired titles.
(3) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■Rated Manuals

Note that the following related documents are available.

"MN101C Series LSI User's Manual"
<Describes the device hardware.>
"MN101C Series Instruction Manual"
<Describes the instruction set.>
"MN101C Series C Compiler User's Manual: Usage Guide"
<Describes the installation, the commands, and options of the C Compiler.>
"MN101C Series C Compiler User's Manual: Language Description"
<Describes the syntax of the C Compiler.>
"MN101C Series C Compiler User's Manual: Library Reference"
<Describes the standard library of the C Compiler.>
"MN101C Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>
"MN101C Series C Source Code Debugger User's Manual"
<Describes the use of C source code debugger.>
"MN101C Series PanaX Series Installation Manual"
<Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

Chapter 1	Overview	1
Chapter 2	Basic CPU	2
Chapter 3	Interrupts	3
Chapter 4	I/O Ports	4
Chapter 5	Prescaler	5
Chapter 6	8-bit Timers	6
Chapter 7	16-bit Timers	7
Chapter 8	Time Base Timer / 8-bit Free-running Timer	8
Chapter 9	Watchdog Timer	9
Chapter 10	Buzzer	10
Chapter 11	Serial Interface 0	11
Chapter 12	A/D Converter	12
Chapter 13	LCD	13
Chapter 14	Appendices	14

Contents

Chapter 1 Overview

1-1 Overview ..... I - 2
1-1-1 Overview ..... I - 2
1-1-2 Product Summary ..... I - 2
1-2 Hardware Functions ..... I - 3
1-3 Pin Description ..... I - 8
1-3-1 Pin Configuration ..... I - 8
1-3-2 Pin Specification ..... I - 9
1-3-3 Pin Functions ..... I - 10
1-4 Block Diagram ..... I - 16
1-4-1 Block Diagram ..... I - 16
1-5 Electrical Characteristics ..... I - 17
1-5-1 Absolute Maximum Ratings ..... I - 17
1-5-2 Operating Conditions ..... I - 18
1-5-3 DC Characteristics ..... I - 21
1-5-4 A/D Converter Characteristics ..... I - 26
1-6 Cautions for Circuit Setup ..... I - 27
1-6-1 General Usage ..... I - 27
1-6-2 Unused Pins ..... I - 28
1-6-3 Power Supply ..... I - 30
1-6-4 Power Supply Circuit ..... I - 31
1-6-5 Oscillators ..... I - 32
1-7 Package Dimension ..... I - 34
1-8 Operation Mode Check List ..... I - 36

Chapter 2 Basic CPU

2-1 Overview ..... II - 2
2-1-1 Block Diagram ..... II - 3
2-1-2 CPU Control Registers ..... II - 4
2-1-3 Instruction Execution Controller ..... II - 5
2-1-4 Pipeline Process ..... II - 6
2-1-5 Registers for Address ..... II - 6
2-1-6 Registers for Operation ..... II - 7
2-1-7 Processor Status Word ..... II - 8
2-1-8 Addressing Modes ..... II - 10
2-2 Memory Space ..... II - 12
2-2-1 Memory Mode ..... II - 12
2-2-2 Single-chip Mode ..... II - 13
2-2-3 Special Function Registers ..... II - 14

2-3 Bus Interface ..... II - 15
2-3-1 Bus Controller ..... II - 15
2-3-2 Control Registers ..... II - 16
2-4 Standby Function ..... II - 17
2-4-1 Outline ..... II - 17
2-4-2 CPU Mode Control Register ..... II - 19
2-4-3 Transition Between SLOW and NORMAL Modes ..... II - 20
2-4-4 Transition to STANDBY Modes ..... II - 21
2-5 Clock Switching ..... II - 23
2-6 Reset ..... II - 25
2-6-1 Reset Operation ..... II - 25
2-6-2 Oscillation Stabilization Wait Time ..... II - 27

Chapter 3 Interrupts

3-1 Overview ..... III - 2
3-1-1 Functions ..... III - 3
3-1-2 Block Diagram ..... III - 4
3-1-3 Operation ..... III - 5
3-1-4 Interrupt Flag Setup ..... III - 14
3-2 Control Registers ..... III - 15
3-2-1 Registers List ..... III - 15
3-2-2 Interrupt Control Registers ..... III - 16
3-3 External Interrupts ..... III - 34
3-3-1 Overview ..... III - 34
3-3-2 Block Diagram ..... III - 35
3-3-3 Control Registers ..... III - 38
3-3-4 Programmable Active Edge Interrupt ..... III - 42
3-3-5 Both Edges Interrupt ..... III - 43
3-3-6 Key Input Interrupt ..... III - 45
3-3-7 Noise Filter ..... III - 47
3-3-8 AC Zero-Cross Detector ..... III - 50

Chapter 4 I/O Ports

4-1 Overview ..... IV - 2
4-1-1 I/O Port Diagram ..... IV - 2
4-1-2 I/O Port Status at Reset ..... IV - 3
4-1-3 Control Registers ..... IV - 4
4-2 Port 0 ..... IV - 6
4-2-1 Description ..... IV - 6
4-2-2 Registers ..... IV - 7
4-2-3 Block Diagram ..... IV - 8

4-3 Port 1 ..... IV - 10
4-3-1 Description ..... IV - 10
4-3-2 Registers ..... IV - 11
4-3-3 Block Diagram ..... IV - 13
4-4 Port 2 ..... IV - 14
4-4-1 Description ..... IV - 14
4-4-2 Registers ..... IV - 15
4-4-3 Block Diagram ..... IV - 16
4-5 Port 3 ..... IV - 17
4-5-1 Description ..... IV - 17
4-5-2 Registers ..... IV - 18
4-5-3 Block Diagram ..... IV - 20
4-6 Port 5 ..... IV - 21
4-6-1 Description ..... IV - 21
4-6-2 Registers ..... IV - 22
4-6-3 Block Diagram ..... IV - 24
4-7 Port 6 ..... IV - 25
4-7-1 Description ..... IV - 25
4-7-2 Registers ..... IV - 26
4-7-3 Block Diagram ..... IV - 29
4-8 Port 7 ..... IV - 30
4-8-1 Description ..... IV - 30
4-8-2 Registers ..... IV - 31
4-8-3 Block Diagram ..... IV - 34
4-9 Port 8 ..... IV - 35
4-9-1 Description ..... IV - 35
4-9-2 Registers ..... IV - 36
4-9-3 Block Diagram ..... IV - 38
4-10 Port A ..... IV - 39
4-10-1 Description ..... IV - 39
4-10-2 Registers ..... IV - 40
4-10-3 Block Diagram ..... IV - 42
4-11 Synchronous Output (Port 6) ..... IV - 43
4-11-1 Block Diagram ..... IV - 43
4-11-2 Registers ..... IV - 44
4-11-3 Operation ..... IV - 45
4-11-4 Setup example ..... IV - 47

Chapter 5 Prescaler

5-1 Overview ..... V - 2
5-1-1 Peripheral Functions ..... V - 3
5-1-2 Block Diagram ..... V - 4

5-2 Control Registers ..... V - 5
5-2-1 Registers List ..... V - 5
5-2-2 Control Registers ..... V - 6
5-3 Operation ..... V - 10
5-3-1 Operation ..... V - 10
5-3-2 Setup Example ..... V - 11

Chapter 6 8-bit Timers

6-1 Overview ..... VI - 2
6-1-1 Functions ..... VI - 2
6-1-2 Block Diagram ..... VI - 3
6-2 Control Registers ..... VI - 6
6-2-1 Registers ..... VI - 6
6-2-2 Programmable Timer Registers ..... VI - 8
6-2-3 Timer Mode Registers ..... VI - 10
6-3 Operation ..... VI - 15
6-3-1 Operation ..... VI - 15
6-3-2 Setup Example ..... VI - 17
6-4 8-bit Event Count ..... VI - 19
6-4-1 Operation ..... VI - 19
6-4-2 Setup Example ..... VI - 21
6-5 8-bit Timer Pulse Output ..... VI - 23
6-5-1 Operation ..... VI - 23
6-5-2 Setup Example ..... VI - 24
6-6 8-bit PWM Output ..... VI - 26
6-6-1 Operation ..... VI - 26
6-6-2 Setup Example ..... VI - 28
6-6-3 PWM Output With Additional Pulse ..... VI - 30
6-7 Synchronous Output ..... VI - 32
6-7-1 Operation ..... VI - 32
6-7-2 Setup Example ..... VI - 33
6-8 Serial Transfer Clock Output ..... VI - 35
6-8-1 Operation ..... VI - 35
6-8-2 Setup Example ..... VI - 36
6-9 Simple Pulse Width Measurement ..... VI - 38
6-9-1 Operation ..... VI - 38
6-9-2 Setup Example ..... VI - 39
6-10 Cascade Connection ..... VI - 41
6-10-1 Operation ..... VI - 41
6-10-2 Setup Example ..... VI - 43
6-11 Remote Control Carrier Output ..... VI - 45
6-11-1 Operation ..... VI - 45

6-11-2 Setup Example ..... VI - 46

Chapter 7 16-bit Timers

7-1 Overview ..... VII - 2
7-1-1 Functions ..... VII - 2
7-1-2 Block Diagram ..... VII - 3
7-2 Control Registers ..... VII - 5
7-2-1 Registers ..... VII - 5
7-2-2 Programmable Timer Registers ..... VII - 6
7-2-3 Timer Mode Registers ..... VII - 10
7-3 Operation ..... VII - 14
7-3-1 Operation ..... VII - 14
7-3-2 Setup Example ..... VII - 18
7-4 16-bit Event Count ..... VII - 20
7-4-1 Operation ..... VII - 20
7-4-2 Setup Example ..... VII - 22
7-5 16-bit Timer Pulse Output ..... VII - 24
7-5-1 Operation ..... VII - 24
7-5-2 Setup Example ..... VII - 26
7-6 16-bit Standard PWM Output (Only duty can be changed consecutively) ..... VII - 28
7-6-1 Operation ..... VII - 28
7-6-2 Setup Example ..... VII - 30
7-7 16-bit High Precision PWM Output (Cycle/Duty can be changed consecutively) . VII - 32
7-7-1 Operation ..... VII - 32
7-7-2 Setup Example ..... VII - 34
7-8 16-bit Timer Synchronous Output ..... VII - 36
7-8-1 Operation ..... VII - 36
7-8-2 Setup Example ..... VII - 37
7-9 16-bit Timer Capture ..... VII - 39
7-9-1 Operation ..... VII - 39
7-9-2 Setup Example ..... VII - 42
7-10 Cascade Connection ..... VII - 44
7-10-1 Operation ..... VII - 44
7-10-2 Setup Example ..... VII - 46

Chapter 8 Time Base Timer / 8-bit Free-running Timer

8-1 Overview ..... VIII - 2
8-1-1 Functions ..... VIII - 2
8-1-2 Block Diagram ..... VIII - 3

8-2 Control Registers ..... VIII - 4
8-2-1 Control Registers ..... VIII - 4
8-2-2 Programmable Timer Registers ..... VIII - 5
8-2-3 Timer Mode Registers ..... VIII - 6
8-3 8-bit Free-running Timer ..... VIII - 7
8-3-1 Operation ..... VIII - 7
8-3-2 Setup Example ..... VIII - 10
8-4 Time Base Timer ..... VIII - 12
8-4-1 Operation ..... VIII - 12
8-4-2 Setup Example ..... VIII - 14

Chapter 9 Watchdog Timer

9-1 Overview ..... IX - 2
9-1-1 Block Diagram ..... IX - 2
9-2 Control Registers ..... IX - 3
9-3 Operation ..... IX - 4
9-3-1 Operation ..... IX - 4
9-3-2 Setup Example ..... IX - 7

Chapter 10 Buzzer

10-1 Overview ..... X - 2
10-1-1 Block Diagram ..... X - 2
10-2 Control Register ..... X - 3
10-3 Operation ..... X - 4
10-3-1 Operation ..... X - 4
10-3-2 Setup Example ..... X - 5

Chapter 11 Serial Interface 0

11-1 Overview ..... XI - 2
11-1-1 Functions ..... XI - 2
11-1-2 Block Diagram ..... XI - 3
11-2 Control Registers ..... XI - 4
11-2-1 Registers ..... XI - 4
11-2-2 Data Buffer Registers ..... XI - 5
11-2-3 Mode Registers ..... XI - 6
11-3 Operation ..... XI - 12
11-3-1 Clock Synchronous Serial Interface ..... XI - 12
11-3-2 Setup Example ..... XI - 27
11-3-3 UART Serial Interface ..... XI - 30
11-3-4 Setup Example ..... XI - 44

Chapter 12 A/D Converter

12-1 Overview ..... XII - 2
12-1-1 Functions ..... XII - 2
12-1-2 Block Diagram ..... XII - 3
12-2 Control Registers ..... XII - 4
12-2-1 Registers ..... XII - 4
12-2-2 Control Registers ..... XII - 5
12-2-3 Data Buffers ..... XII - 7
12-3 Operation ..... XII - 8
12-3-1 Setup ..... XII - 10
12-3-2 Setup Example ..... XII - 12
12-3-3 Cautions ..... XII - 14

Chapter 13 LCD

13-1 LCD Functions ..... XIII - 2
13-1-1 Functions ..... XIII - 2
13-1-2 LCD Operation in Standby Mode ..... XIII - 3
13-1-3 Maximum Pixels ..... XIII - 3
13-1-4 Switching I/O ports and LCD segment pins ..... XIII - 4
13-1-5 LCD Driver Circuit Block Diagram ..... XIII - 5
13-2 13-2 Control Registers ..... XIII - 6
13-2-1 Registers ..... XIII - 6
13-2-2 Mode Control Register 1 (LCDMD1) ..... XIII - 7
13-2-3 Mode Control Register2 (LCDMD2) ..... XIII - 8
13-2-4 Output Control Register 1 (LCCTR1) ..... XIII - 9
13-2-5 Output Control Register 2 (LCCTR2) ..... XIII - 10
13-2-6 Segment Output Latch ..... XIII - 11
13-3 Operation ..... XIII - 12
13-3-1 Circuit Operation for LCD drive ..... XIII - 12
13-3-2 Voltage Booster Circuit for LCD Drive ..... XIII - 13
13-3-3 Power Supply ..... XIII - 15
13-3-4 Frame Cycle ..... XIII - 20
13-3-5 Setup Example of the LCD Driver Circuit ..... XIII - 21
13-4 Display ..... XIII - 24
13-4-1 Static ..... XIII - 24
13-4-2 Setup Example (static) ..... XIII - 26
13-4-3 1/2 duty ..... XIII - 28
13-4-4 Setup Example (1/2 duty) ..... XIII - 30
13-4-5 1/3 duty ..... XIII - 32
13-4-6 Setup Example (1/3 duty) ..... XIII - 34
13-4-7 1/4 duty ..... XIII - 36
13-4-8 Setup Example (1/4 duty) ..... XIII - 38

Chapter 14 Appendices

14-1 EPROM Versions ..... XIV - 2
14-1-1 Overview ..... XIV - 2
14-1-2 Caution on Use ..... XIV - 3
14-1-3 Erasing Data in Windowed Package ..... XIV - 4
14-1-4 Differences between Mask ROM Version and EPROM Version ..... XIV - 5
14-1-5 Writing to EPROM built-in Microcontroller ..... XIV - 6
14-1-6 Cautions on Operation of ROM Writer ..... XIV - 8
14-1-7 Programming Adapter Connection ..... XIV - 9
14-2 Probe Switches ..... XIV - 10
14-2-1 PRB-MBB101C52-M ..... XIV - 10
14-2-2 PX-CN101-M ..... XIV - 11
14-2-3 PRB-ADP101-64-M ..... XIV - 12
14-2-4 PRB-DMY101C52-M ..... XIV - 13
14-3 Instruction Set ..... XIV - 14
14-4 Instruction Map ..... XIV - 20
14-5 Special Function Registers List ..... XIV - 22

Chapter 1 Overview

1-1 Overview

1-1-1 Overview

The MN101C series of 8-bit single-chip microcomputers incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, remote control, fax machine, musical instrument, Health care and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. This LSI has an internal 16 KB of ROM and 1.5 KB of RAM. Peripheral functions include 4 external interrupts, 13 internal interrupts including NMI, 9 timer counters, 2 sets of serial interfaces, A/D converter, watchdog timer, synchronous output function, buzzer output, and remote control output. The configuration of this microcomputer is well suited for application as a system controller in a camera, a sphygmomanometer, CD player, or MD.

With two oscillation system (max. 20 MHz/32 kHz) contained on the chip, the system clock can be switched to **high frequency input** (high speed mode), or to **low frequency input** (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software.

A **machine cycle** (min. instruction execution time) is 250 ns when the oscillation source (fosc) is 8 MHz, and a **machine cycle** is 100 ns when fosc is 20 MHz. Two types of packages are available, 64-pin LQFP.

1-1-2 Product Summary

This manual describes the following models of the MN101C52 series. These products have identical functions.

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101C527	16 KB	1.5 KB	Mask ROM version
MN101CP52A	32 KB	1.5 KB	EPROM version

1-2 Hardware Functions

CPU Core **MN101C Core**

- LOAD-STORE architecture (3-stage pipeline)
- Half-byte instruction set / Handy addressing
- Machine cycle (at 2-divide of crystal oscillation)

High speed mode	0.10 µs / 20 MHz	(4.5 V to 5.5 V)
	0.25 µs/ 8 MHz	(2.7 V to 5.5 V)
	0.5 µs / 4 MHz	(2.3 V to 5.5 V)
	1.0 µs/ 2 MHz	(2.0 V to 5.5 V) *1
Low speed mode	62.5 µs / 32 kHz	(2.0 V to 5.5 V) *1

*1: Minimum rating for EPROM vers. is 2.3 V to 5.5 V.

- Clock gear
  The operation speed of system clock can be changed by switching divide ratio of the oscillation with software.
- Operation modes
  NORMAL mode (High speed mode)
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)

Internal memory **ROM 16 KB**
RAM 1.5 KB

Interrupts **13 Internal interrupts**

< Non maskable interrupt (NMI) >
- Incorrect code execution interrupt

< Timer interrupts >
- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Timer 6 interrupt
- Time base interrupt
- Timer 7 interrupt
- Match interrupt for Timer 7 compare register 2
- Timer 8 interrupt

< Serial interrupts >
- Serial 0 interrupt 1
- Serial 0 interrupt 2

< A/D interrupt >
- A/D conversion interrupt

4 External interrupts

- IRQ0 : Edge selectable. With/without noise filter.
- IRQ1 : Edge selectable. With/without noise filter.
  AC zero cross detector.
- IRQ2 : Edge selectable. Both edges interrupt.
  (STOP/HALT: can be recovered at the both edges.)
- IRQ4 : Key interrupt only.

Timers / Counters 9 timers (8 can be operated independently)

- 8-bit timer for general use	4 sets
- 8-bit timer (used as UART baud rate timer as well)	1 set
- 8-bit free-running timer	1 set
Time base timer	1 set
- 16-bit timer for general use	2 sets

Timer 0 (8-bit timer for general use)

- Square wave output (Timer pulse output), PWM output,
  Event count, Remote control carrier output, Simple pulse width measurement
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock
- Square wave output and PWM output can be output to large current driver port P50 (TM0O).

Timer 1 (8-bit timer for general use)

- Square wave output (Timer pulse output), Event count,
  16-bit cascade connection (connected to timer 0),
  Timer synchronous output
- Clock source
  fosc, fosc/4, fosc/16, fosc/2^{13}, fosc/2^{15}, fs/2, fs/8, fx, external clock

Timer 2 (8-bit timer for general use)

- Square wave output (Timer pulse output), Added pulse (2-bit) type PWM output, Event count, Timer synchronous output, Simple pulse width measurement
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock
- Square wave output and PWM output can be output to large current driver port P52 (TM2O).

Timer 3 (8-bit timer for general use)

- Square wave output (Timer pulse output), Event count, Serial transfer clock, 16-bit cascade connection (connect to timer2), Remote control carrier output
- Clock source

  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/, fx, external clock
- Can be used as UART baud rate timer as well.

Timer 6 (8-bit free-running timer, Time base timer)

❑ **8-bit free-running timer**

- Clock source

  fosc, fosc/2^{12}, fosc/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

❑ **Time base timer**

- Interrupt generation cycle

  fosc/2^{7}, fosc/2^{8}, fosc/2^{9}, fosc/2^{10}, fosc/2^{13}, fosc/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)

- Clock source

  fosc, fosc/2, fosc/4, fosc/16, fs, fs/2, fs/4, fs/16,
  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	2 sets
Input capture register	1 set
Timer interrupt	2 vectors

- Timer functions

  Square wave output (Timer pulse output), Event count,
  High precision PWM output (Cycle/Duty can be changed constantly),
  Timer synchronous output, Input capture function (Both edges can be operated)
- Square wave output and PWM output can be output to large current driver port P51 (TM7O).

Timer 8 (16-bit timer for general use)

- Clock source

  fosc, fosc/2, fosc/4, fosc/16, fs, fs/2, fs/4, fs/16,
  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	1 set
Input capture register	1 set
Timer interrupt	1 vector

- Timer functions

  Square wave output (Timer pulse output), Event count,
  Standard PWM output (Duty can be changed constantly),
  Input capture function (Both edges can be operated).
- 32-bit cascade connection (connected to timer 7, Square wave output, Input capture function)
- Square wave output and PWM output can be output to large current driver port P53 (TM8O).

Watchdog timer

- Time-out period can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$.
- On detection of errors, hardware reset is done by force in LSI.

Synchronous output function

Timer synchronous output, Interrupt synchronous output

- Port 6 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, or 7, or of the external interrupt 2 (IRQ2).

Buzzer output Output frequency can be selected from $fosc/2^9$, $fosc/2^{10}$, $fosc/2^{11}$, $fosc/2^{12}$, $fosc/2^{13}$, $fosc/2^{14}$, $fx/2^3$ and $fx/2^4$.

Remote control output

Based on the timer 0 and timer 3 output, a remote control carrier with duty cycle of 1/2 or 1/3 can be output.

A/D converter **10 bits X 4 channels**

Serial interface **1 type**

Serial 0 (Duplex UART / Synchronous serial interface)

❑ **Synchronous serial interface**

- Transfer clock source
  fosc/2, fosc/4, fosc/16, fosc/64, fs/2, fs/4
  1/2 of UART baud rate timer (timers 3) output
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

❑ **Duplex UART (Baud rate timer : Timers 3)**

- Parity check, Overrun error / framing error detection
- Transfer size 7 to 8 bits can be selected.

LED driver **4 pins (push-pull configuration)**

LCD driver **LCD driver pins**

- Segment output : 24 pins max. (SEG0 to 23)
  SEG0 to 15 are switchable to I/O ports in unit of 2 pins.
  SEG16 to 23 are switchable to I/O ports in 1 pin unit.
  [Note : At reset, SEG0 to 23 are input ports.]
- Common output pins : 4 pins
  COM0 to 3 are switchable to I/O ports in 1 pin unit.

Display mode selection

static
1/2 duty, 1/2 bias
1/3 duty, 1/3 bias
1/4 duty, 1/3 bias

LCD driver clock

The source clock is the main clock (fosc) :

$1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$

The source clock is the sub-clock (fx) :

$1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

LCD power supply

LCD power supply is separated from V_{DD}. (Available at $V_{LCD} \geq V_{DD}$, $V_{LCD} \leq 5.5$ V)
Supply voltage can be selected from internal voltage booster output or external supply voltage.
(The voltage booster performs three times boosting of V_{LCIN3} input voltage, or 3/2 times boosting of V_{LCIN2} input voltage.)
(External supply voltage is input from V_{LC1}, V_{LC2} and V_{LC3} pins. Or voltage applied to V_{LC1} pin is divided by internal resistance to be used.)

Port

I/O ports 42 ports

- LED (large current) driver ports 4 ports (push-pull configuration)
  (All 4 ports can be switched to PWM output.)
- LCD segment ports 24 ports
- LCD common ports 4 ports
- Serial ports 3 ports
- Timer I/O ports 5 ports
- Timer, remote control carrier output port 1 port
- Buzzer output port 1 port

Input ports 7 ports

- External interrupt 3 ports (one pin is also used as zero-cross input.)
- A/D input ports 4 ports

Special pins 15 ports

- Analog reference voltage input pins : 2 pins
- Operation mode input port : 1 pin
- Reset input pins : 1 pin
- Connection pins for boost up capacitor : 2 pins
- LCD power supply pin (including reference power supply for boosting) : 3 pins
- Oscillation pins : 4 pins
- Power pins : 2 pins

Package **64-pin LQFP (14 mm square / 0.8 mm pitch)**

Package code **LQFP064-P-1414**

1-3 Pin Description

1-3-1 Pin Configuration

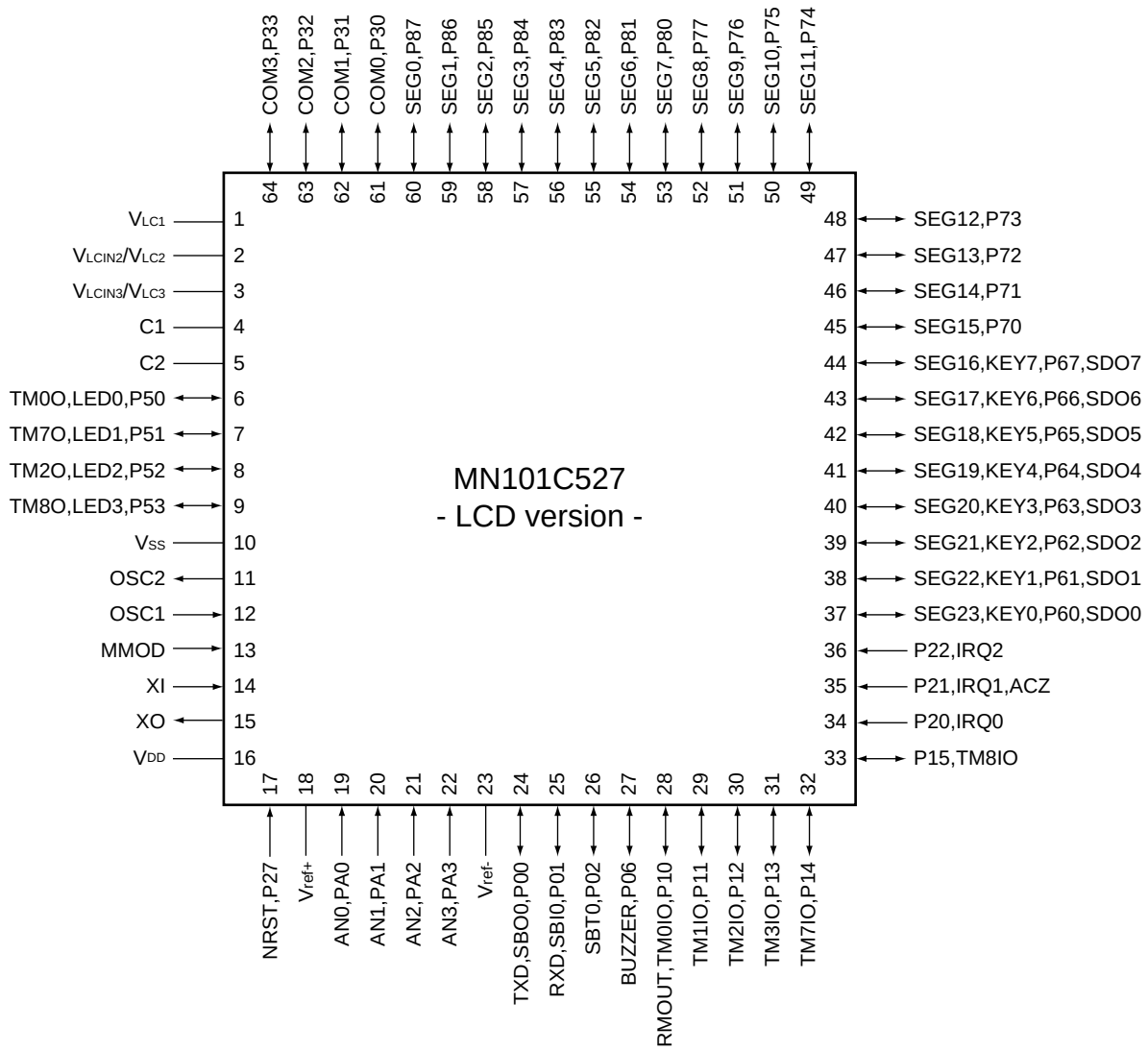


Figure 1-3-1 Pin Configuration (64LQFP : Top view)

1-3-2 Pin Specification

Table 1-3-1 Pin Specification

Pins	Special Funcion		I/O	Direction Control	Pin Control	Functions Descroption	
P00	SBO0	TXD	in/out	P0DIR0	P0PLU0	SBO0: Serial 0 transmission data output	TXD: UART transmission data output
P01	SBI0	RXD	in/out	P0DIR1	P0PLU1	SBI0: Serial 0 reception data input	RXD: UART reception data input
P02	SBT0		in/out	P0DIR2	P0PLU2	SBT0: Serial 0 clock input/output	
P06	BUZZER		in/out	P0DIR6	P0PLU6	BUZZER: Buzzer output	
P10	TM0IO	RMOUT	in/out	P1DIR0	P1PLU0	TM0IO: Timer 0 input/output	RMOUT: Remoto control carrier output
P11	TM1IO		in/out	P1DIR1	P1PLU1	TM1IO: Timer 1 nitput/output	
P12	TM2IO		in/out	P1DIR2	P1PLU2	TM2IO: TImer 2 input/output	
P13	TM3IO		in/out	P1DIR3	P1PLU3	TM3IO: Timer 3 input/output	
P14	TM7IO		in/out	P1DIR4	P1PLU4	TM7IO: Timer 7 input/output	
P15	TM8IO		in/out	P1DIR5	P1PLU5	TM8IO: Timer 8 input/output	
P20	IRQ0		in	-	P2PLU0	IRQ0: External interruption 0	
P21	IRQ1	ACZ	in	-	P2PLU1	IRQ1: External interruption 1	ACZ: Zero-cross input
P22	IRQ2		in	-	P2PLU2	IRQ2: External interruption 2	
P27	NRST		in	-	-	NRST: Reset	
P30	COM0		in/out	P3DIR0	P3PLU0	COM0: LCD common output	
P31	COM1		in/out	P3DIR1	P3PLU1	COM1: LCD common output	
P32	COM2		in/out	P3DIR2	P3PLU2	COM2: LCD common output	
P33	COM3		in/out	P3DIR3	P3PLU3	COM3: LCD common output	
P50	TM0O	LED0	in/out	P5DIR0	P5PLU0	TM0O: Timer 0 output	LED0: LED driver pin
P51	TM7O	LED1	in/out	P5DIR1	P5PLU1	TM7O: Timer 7 output	LED1: LED driver pin
P52	TM2O	LED2	in/out	P5DIR2	P5PLU2	TM2O: Timer 2 output	LED2: LED driver pin
P53	TM8O	LED3	in/out	P5DIR3	P5PLU3	TM8O: Timer 8 output	LED3: LED driver pin
P60	KEY0	SEG23	in/out	P6DIR0	P6PLUD0	KEY0: KEY interrupt input 0	SEG23: LCD segment output
P61	KEY1	SEG22	in/out	P6DIR1	P6PLUD1	KEY1: KEY interrupt input 1	SEG22: LCD segment output
P62	KEY2	SEG21	in/out	P6DIR2	P6PLUD2	KEY2: KEY interrupt input 2	SEG21: LCD segment output
P63	KEY3	SEG20	in/out	P6DIR3	P6PLUD3	KEY3: KEY interrupt input 3	SEG20: LCD segment output
P64	KEY4	SEG19	in/out	P6DIR4	P6PLUD4	KEY4: KEY interrupt input 4	SEG19: LCD segment output
P65	KEY5	SEG18	in/out	P6DIR5	P6PLUD5	KEY5: KEY interrupt input 5	SEG18: LCD segment output
P66	KEY6	SEG17	in/out	P6DIR6	P6PLUD6	KEY6: KEY interrupt input 6	SEG17: LCD segment output
P67	KEY7	SEG16	in/out	P6DIR7	P6PLUD7	KEY7: KEY interrupt input 7	SEG16: LCD segment output
P70	SEG15		in/out	P7DIR0	P7PLUD0	SEG15: LCD segment output	
P71	SEG14		in/out	P7DIR1	P7PLUD1	SEG14: LCD segment output	
P72	SEG13		in/out	P7DIR2	P7PLUD2	SEG13: LCD segment output	
P73	SEG12		in/out	P7DIR3	P7PLUD3	SEG12: LCD segment output	
P74	SEG11		in/out	P7DIR4	P7PLUD4	SEG11: LCD segment output	
P75	SEG10		in/out	P7DIR5	P7PLUD5	SEG10: LCD segment output	
P76	SEG9		in/out	P7DIR6	P7PLUD6	SEG9 : LCD segment output	
P77	SEG8		in/out	P7DIR7	P7PLUD7	SEG8 : LCD segment output	
P80	SEG7		in/out	P8DIR0	P8PLU0	SEG7 : LCD segment output	
P81	SEG6		in/out	P8DIR1	P8PLU1	SEG6 : LCD segment output	
P82	SEG5		in/out	P8DIR2	P8PLU2	SEG5 : LCD segment output	
P83	SEG4		in/out	P8DIR3	P8PLU3	SEG4 : LCD segment output	
P84	SEG3		in/out	P8DIR4	P8PLU4	SEG3 : LCD segment output	
P85	SEG2		in/out	P8DIR5	P8PLU5	SEG2 : LCD segment output	
P86	SEG1		in/out	P8DIR6	P8PLU6	SEG1 : LCD segment output	
P87	SEG0		in/out	P8DIR7	P8PLU7	SEG0 : LCD segment output	
PA0	AN0		in	-	PAPLUD0	AN0: Analog 0 input	
PA1	AN1		in	-	PAPLUD1	AN1: Analog 1 input	
PA2	AN2		in	-	PAPLUD2	AN2: Analog 2 input	
PA3	AN3		in	-	PAPLUD3	AN3: Analog 3 input	

1-3-3 Pin Functions

Table 1-3-2 Pin Function Summary (1/6)

Name	No.	I/O	Other Function	Function	Description
VSS VDD	10 16			Power supply pin	Supply 2.0 V to 5.5 V to VDD, and 0 V to VSS.
OSC1 OSC2	12 11	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	14 15	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.
NRST	17	Input	P27	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated to P27 and contains an internal pull-up resistor. Setting this pin low initializes the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD.
P00 P01 P02 P06	24 25 26 27	I/O	SBO0, TXD SBI0, RXD SBT0	I/O port 0	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance output).
P10 P11 P12 P13 P14 P15	28 29 30 31 32 33	I/O	TM0IO, RMOUT TM1IO TM2IO TM3IO TM7IO TM8IO	I/O port 1	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance output).

Table 1-3-3 Pin Function Summary (2/6)

Name	No.	I/O	Other Function	Function	Description
P20 P21 P22	34 35 36	Input	IRQ0 IRQ1, ACZ IRQ2	Input port 2	3-bit input port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, pull-up resistor is disabled.
P27	17	Input	NRST	I/O port 2	Port P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
P30 P31 P32 P33	61 62 63 64	I/O	COM0 COM1 COM2 COM3	I/O port 3	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance output).
P50 P51 P52 P53	6 7 8 9	I/O	TM0O, LED0 LED1 TM2O, LED2 LED3	I/O port 5	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, when the single chip mode is selected, pull-up resistor is disabled (high impedance output) on P50 to P53 input mode.
P60 P61 P62 P63 P64 P65 P66 P67	37 38 39 40 41 42 43 44	I/O	KEY0, SEG23 KEY1, SEG22 KEY2, SEG21 KEY3, SEG20 KEY4, SEG19 KEY5, SEG18 KEY6, SEG17 KEY7, SEG16	I/O port 6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up/pull-down resistor for each bit can be selected individually by the P6PLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, when the single chip mode is selected, pull-up resistor is disabled (high impedance output) on P60 to P67 input mode.
P70 P71 P72 P73 P74 P75 P76 P77	45 46 47 48 49 50 51 52	I/O	SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be switched individually as either an input or output by the P7DIR register. A pull-up/pull-down resistor for each bit can be selected individually by the P7PLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, when the single chip mode is selected, pull-up resistor is disabled (high impedance output) on P70 to P77 input mode.

Table 1-3-4 Pin Function Summary (3/6)

Name	No.	I/O	Other Function	Function	Description
P80 P81 P82 P83 P84 P85 P86 P87	53 54 55 56 57 58 59 60	I/O	SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0	I/O port 8	8-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At output, LED can be directly driven. At reset, when the single chip mode is selected, pull-up resistor is disabled (high impedance output) on P80 to P87 input mode.
PA0 PA1 PA2 PA3	19 20 21 22	Input	AN0 AN1 AN2 AN3	Input port A	4-bit input port. A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD resister. However, pull-up and pull-down resistors cannot be mixed. At reset, pull-up resistor is disabled (high impedance output) on PA0 to PA3 input mode.
SBO0	24	Output	P00, TXD	Serial interface transmission data output pins	Transmission data output pins for serial interface 0. For the output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistor can be selected by the P0PLU register. Select output mode by the P0DIR register, and serial data output mode by serial mode register 1 (SC0MD1). This can be used as a normal I/O pin when the serial interface is not used.
SBI0	25	Input	P01, RXD	Serial interface received data input pins	Receive data input pins for serial interface 0. Pull-up resistor can be selected by the P0PLU register. Select input mode by the P0DIR register, and serial input mode by the serial mode register 1 (SC0MD1). This can be used as a normal I/O pin when the serial interface is not used.
SBT0	26	I/O	P02	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 . For the output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistor can be selected by the P0PLU register. Select clock I/O for each communication mode by the P0DIR register and serial mode register 1 (SC0MD1). This can be used as a normal I/O pin when the serial interface is not used.

Table 1-3-5 Pin Function Summary (4/6)

Name	No.	I/O	Other Function	Function	Description
TXD	24	Output	SBO0, P00	UART transmission data output pins	When the serial interface is used in UART mode, this pin is configured as the transmission data output pin. For the output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistor can be selected by the P0PLU resister. Select output mode by the P0DIR register, and serial data output by serial 0 mode register 1 (SC0MD1). This can be used as a normal I/O pin when the serial interface is not used.
RXD	25	Input	SBI0, P01	UART received data input pin	When the serial interface is used in UART mode, this pin is configured as the received data input pin. Pull-up resistor can be selected by the P0PLU register. Select the input mode by the P0DIR register, and the serial input mode by the serial 0 mode register 1 (SC0MD1). This can be used as a normal I/O pin when the serial interface is not used.
TM0IO TM1IO TM2IO TM3IO	28 29 30 31	I/O	P10, RMOUT P11 P12 P13	Timer I/O pins	Event counter clock input pins, timer output and PWM signal output pins for 8-bit timers 0 to 3. To use these pins as event clock inputs, configure them as inputs by the P1DIR register. When the pins are used as inputs, pull-up resistor can be specified by the P1PLU register. For timer output and PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. When not used for timer I/O, these can be used as normal I/O pins.
RMOUT	28	I/O	P10,TM0IO	Remote control transmission signal output pin	Output pin for remote control transmission signal with a carrier signal. For remote control carrier output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. Also, set to the remote control carrier output by the remote control carrier output control register (RMCTR). This can be used as a normal I/O pin when remote control is not used.
BUZZER	27	Output	P06	Buzzer output	Piezoelectric buzzer driver pin. The driving frequency can be selected by the DLYCTR register. Select output mode by the P0DIR register and select P06 buzzer output by the DLYCTR register. When not used as a buzzer output pin, this can be used as a normal I/O pin.

Table 1-3-6 Pin Function Summary (5/6)

Name	No.	I/O	Other Function	Function	Description
TM7IO TM8IO	32 33	I/O	P14 P15	Timer I/O pin	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer 7. To use this pin as event clock input, configure this as input by the P1DIR register. In the input mode, pull-up resistor can be selected by the P1PLU register. For timer output and PWM signal output, select the special function pin by the port 1 output mode register (P1OMD), and set to the output mode by the P1DIR register. When not used for timer I/O, this can be used as normal I/O pin.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	37 38 39 40 41 42 43 44	Output	P60, KEY0, SEG23 P61, KEY1, SEG22 P62, KEY2, SEG21 P63, KEY3, SEG20 P64, KEY4, SEG19 P65, KEY5, SEG18 P66, KEY6, SEG17 P67, KEY7, SEG16	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 6 synchronous output control register (P6SYO). Set to the output mode by the P6DIR register. When not used as synchronous output, these can be used as normal I/O pins.
V_{ref+} V_{ref-}	18 23	- -		+power supply for A/D converter -power supply for A/D converter	Reference power supply pins for the A/D converter. Normally, the value of V_{DD}=V_{ref+} and V_{DD}=V_{ref-} are used.
AN0 AN1 AN2 AN3	19 20 21 22	Input	PA0 PA1 PA2 PA3	Analog input pins	Analog input pins for an 4-channel, 10-bit A/D converter. When not used as an analog input pin, these can be used as normal input pins.
IRQ0 IRQ1 IRQ2	34 35 36	Input	P20 P21, ACZ P22	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 2 can be selected with the IRQnICR register. IRQ1 is able to determine AC zero crossings. Both edge for IRQ2 is valid for interrupt. When not used as a interrupt pin, these can be used as normal input pins.
ACZ	35	Input	P21, IRQ1	AC zero-cross detection input pins	Input pins for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level. It outputs a low level at all other times. ACZ input signal is connected to the P21 input circuit and the IRQ1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	37 38 39 40 41 42 43 44	Input	P60, SEG23, SDO0 P61, SEG22, SDO1 P62, SEG21, SDO2 P63, SEG20, SDO3 P64, SEG19, SDO4 P65, SEG18, SDO5 P66, SEG17, SDO6 P67, SEG16, SDO7	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. Key input pin by 1 bit can be selected individually by the key interrupt control register (P6IMD). When not used as KEY input, these can be used as normal I/O pins.

Table 1-3-7 Pin Function Summary (6/6)

Name	No.	I/O	Other Function	Function	Description
C1 C2	4 5			Capacitor connection pins for LCD voltage booster	Capacitor connection pins for LCD voltage booster
V_{LCIN2} V_{LCIN3}	2 3			Reference power supply pins for LCD voltage booster	Reference power supply input pins for LCD voltage booster *1
V_{LC1} V_{LC2} V_{LC3}	1 2 3		 V_{LCIN2} V_{LCIN3}	Input pins for LCD power supply	Supply LCD power. Supply 5.5 V ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ 0 V. *2
COM0 COM1 COM2 COM3	61 62 63 64	output	P30 P31 P32 P33	Output pins for LCD common	These pins output the common signal with the required timing to the LCD display. Connect to the common pins of LCD display panel. When the LCD display panel is turned off, V_{SS} is output. *3
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7 SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15 SEG16 SEG17 SEG18 SEG19 SEG20 SEG21 SEG22 SEG23	60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37	output	P87 P86 P85 P84 P83 P82 P81 P80 P77 P76 P75 P74 P73 P72 P71 P70 P67, KEY7, SDO7 P66, KEY6, SDO6 P65, KEY5, SDO5 P64, KEY4, SDO4 P63, KEY3, SDO3 P62, KEY2, SDO2 P61, KEY1, SDO1 P60, KEY0, SDO0	LCD segment output pins	These pins are LCD segment output pins. When not used as segment output, these pins can be used as normal I/O pins by setting the LCD control register (LCCTR1, 2). SEG0 to 15 can be switched in 2-bits units to I/O ports. SEG16 to 23 can be switched in 1-bit units to I/O ports.
MMOD	12	input		Momory mode switch input pin	This pin set the mode for memory expansion. Input 'L'. (This LSI does not have the memory expasion mode.)

*1 When the reference voltage is input to V_{LCIN2} pin, 3/2 times voltage of the reference voltage is output to V_{LC1} pin, 1/2 times voltage of the reference voltage is output to V_{LC3} pin.
When the reference voltage is input to V_{LCIN3} pin, 3 times voltage of the reference voltage is output to V_{LC1} pin, twice voltage of the reference voltage is output to V_{LC2} pin.

*2 The voltage input to V_{LC2} pin can be devided to V_{LC2} pin and V_{LC3} pin, with the internal voltage divider resistors.

*3 COM0 to 3 can be switched to normal ports 1 bit unit with the LCDMD2 register.

1-4 Block Diagram

1-4-1 Block Diagram

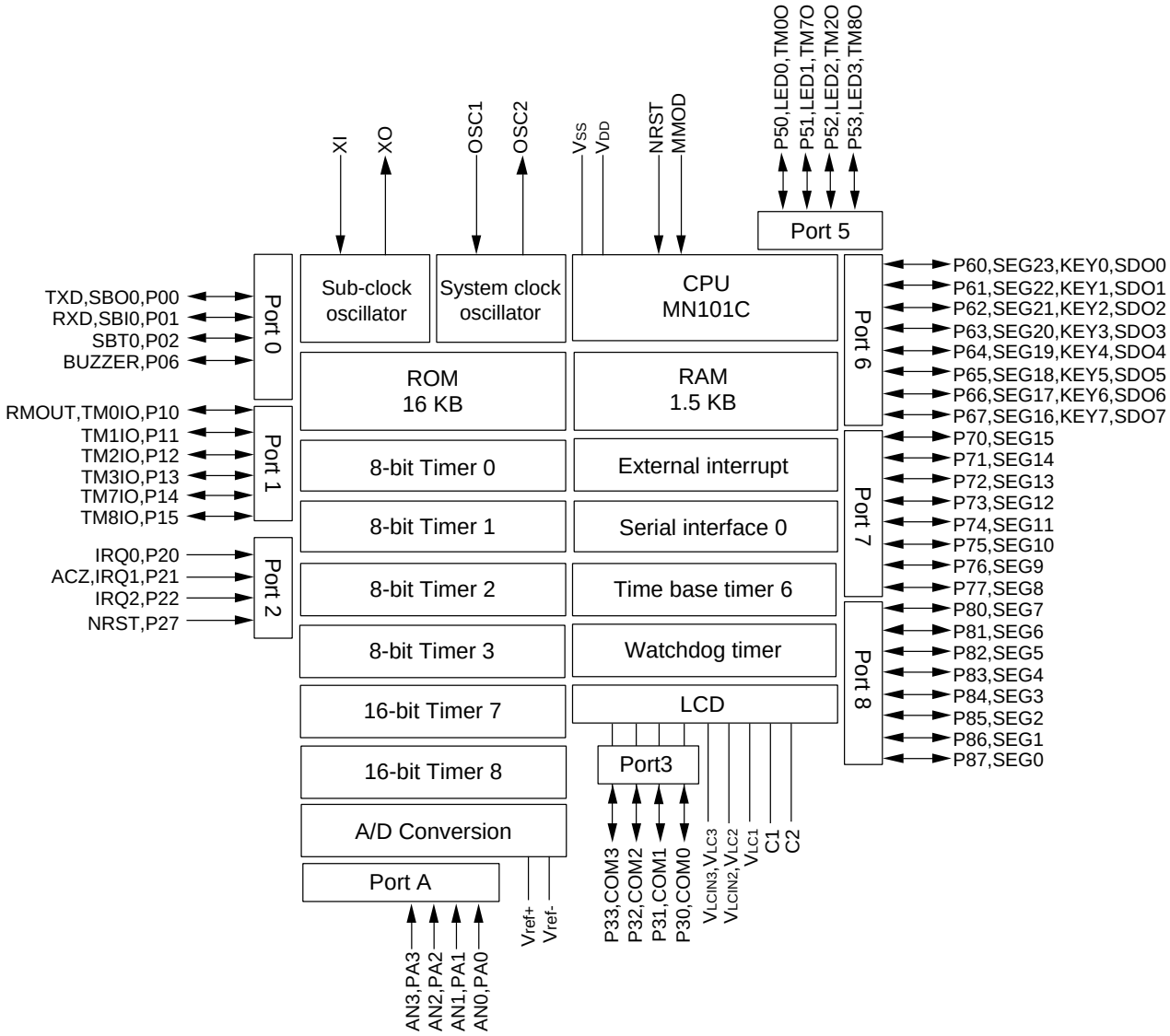


Figure 1-4-1 Block Diagram

1-5 Electrical Characteristics

This LSI user's manual describes the standard specification. Machine cycle (system clock fs) is describe based on the standard mode : 1/2 of high oscillation at NORMAL mode, or on the clock frequency : 1/2 of low oscillation at SLOW mode. Please ask our sales offices for its own product specifications.

Contents \ Model	MN101C527
Structure	CMOS integrated circuit
Appliction	General purpose
Function	CMOS, 8-bit, single-chip microcontroller

1-5-1 Absolute Maximum Ratings*2,*3

No.	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	- 0.3 to +7.0	V
2	Input clamp current (ACZ)		I_C	- 400 to 400	µA
3	Input pin voltage		V_I	- 0.3 to V_{DD} +0.3	V
4	Output pin voltage		V_O	- 0.3 to V_{DD} +0.3	
5	I/O pin voltage		V_{IO1}	- 0.3 to V_{DD} +0.3	
6	Peak output current	P5	I_{OL1} (peak)	30	mA
7		Other than P5	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	- 10	
9	Average output current *1	P5	I_{OL1} (avg)	20	
10		Other than P5	I_{OL2} (avg)	15	
11		All pins	I_{OH} (avg)	- 5	
12	Power dissipation		P_D	400	mW
13	Operating ambient temperature		T_{opr}	- 40 to +85	°C
14	Storage temperature		T_{stg}	- 55 to +125	

*1 Applied to any 100-ms period.

*2 Connect at least one bypass capacitor of 0.1 µF or larger between the power supply pin and the ground for latch-up prevention.

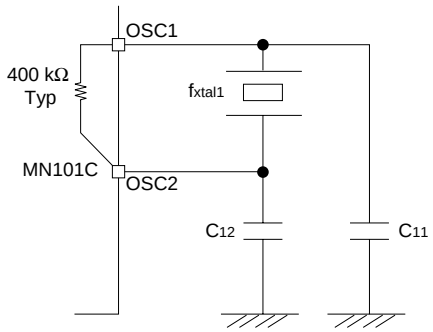
*3 The absolute maximum ratings are the tolerance for the LSI to be operated properly.

1-5-2 Operating Conditions [NORMAL mode : fs=fosc/2, SLOW mode : fs=fx/2]

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

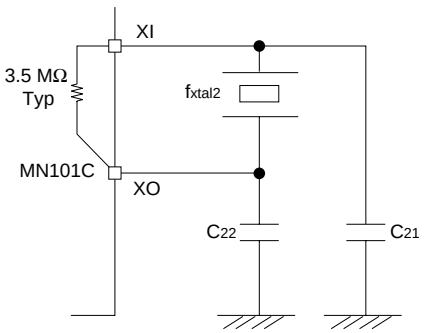
	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Power supply voltage	V_{DD1}	fosc ≤ 20.0 MHz (-40 ºC to +70 ºC)	4.5		5.5	V
2		V_{DD2}	fosc ≤ 8.39 MHz	2.7		5.5	
3		V_{DD3}	fosc ≤ 2.00 MHz	2.0		5.5	
4		V_{DD4}	fx=32.768 kHz	2.0		5.5	
5	Voltage for maintaining RAM data	V_{DD5}	During STOP mode	1.8		5.5	
Operation speed *4							
6	Instruction execution time (fs)	t_{c1}	V_{DD}=4.5 V to 5.5 V	0.100			µs
7		t_{c2}	V_{DD}=2.7 V to 5.5 V	0.238			
8		t_{c3}	V_{DD}=2.0 V to 5.5 V	1.00			
9		t_{c4}	V_{DD}=2.0 V to 5.5 V		61		
Crystal oscillator 1 Figure 1-5-1							
10	Crystal frequency	f_{xtal1}	V_{DD}=4.5 V to 5.5 V	1.0		20.0	MHz
11	External capacitors	C_{11}			20		pF
12		C_{12}			20		
13	Internal feedback resistor	R_{f10}			400		kΩ
Crystal oscillator 2 Figure 1-5-2							
14	Crystal frequency	f_{xtal2}			32.768		kHz
15	External capacitors	C_{21}			20		pF
16		C_{22}			20		
17	Internal feedback resistor	R_{f20}			3.5		MΩ

*4 t_{c1}, t_{c2}, t_{c3}: OSC1 is the CPU clock.
t_{c4} : XI is the CPU clock.



The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected.)							
18	Clock frequency	f_{OSC1}		1.0		20.0	MHz
19	High level pulse width	t_{wh1}	*5 Figure 1-5-3	22.5			ns
20	Low level pulse width	t_{wl1}		22.5			
21	Rising time	t_{wr1}	Figure 1-5-3			5.0	
22	Falling time	t_{wf1}				5.0	
External clock input 2 XI (XO is unconnected.)							
23	Clock frequency	f_{OSC2}		32.768		100	kHz
24	High level pulse width	t_{wh2}	*5 Figure 1-5-4	4.5			µs
25	Low level pulse width	t_{wl2}		4.5			
26	Rising time	t_{wr2}	Figure 1-5-4			20	ns
27	Falling time	t_{wf2}				20	

*5 The clock duty rate in the standard mode should be 45 % to 55 %.

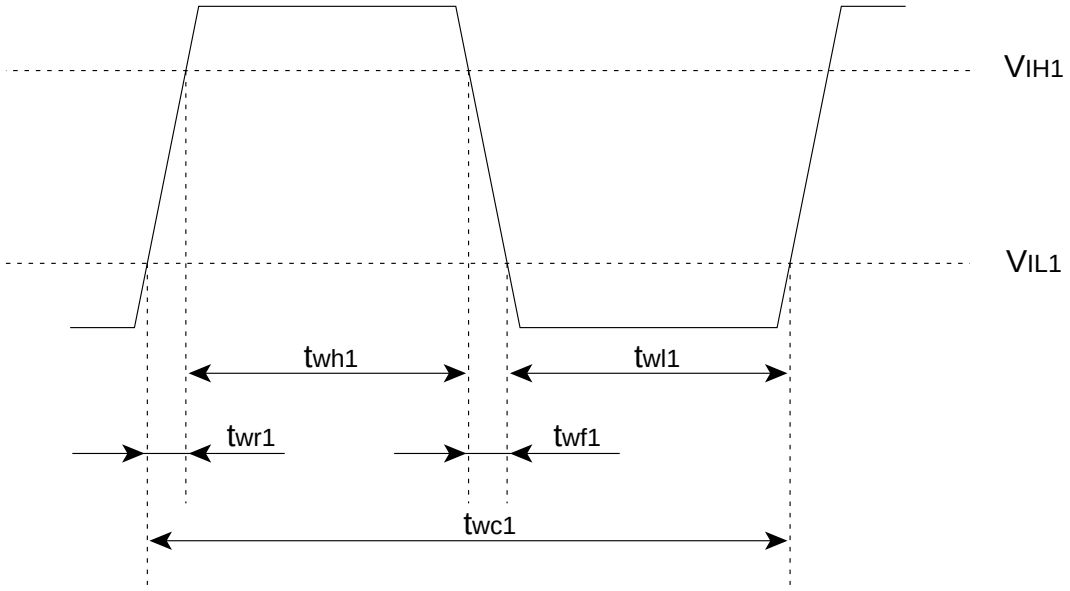


Figure 1-5-3 OSC1 Timing Chart

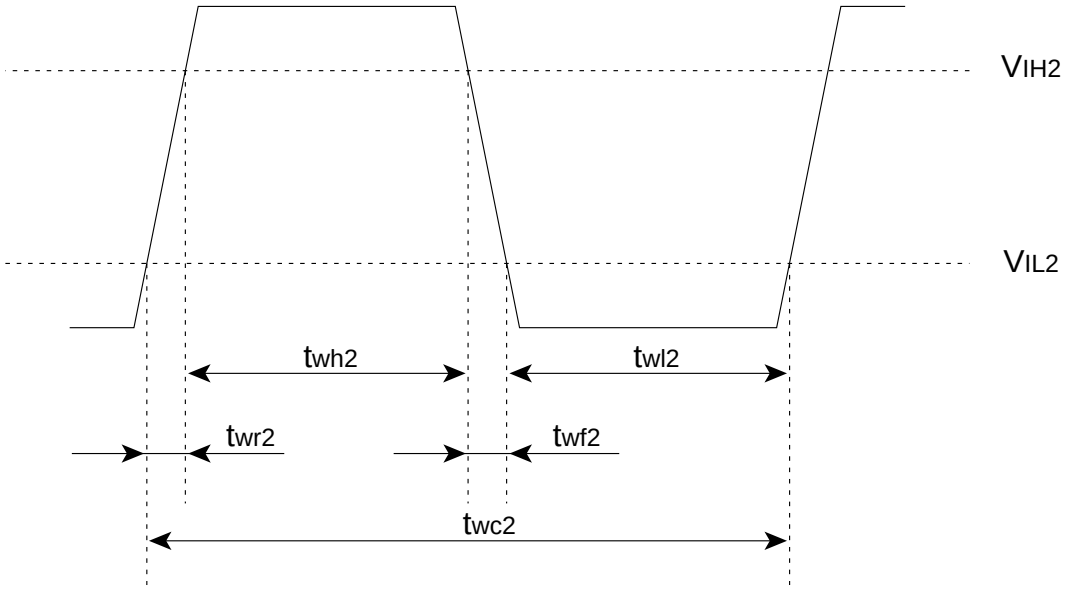


Figure 1-5-4 XI Timing Chart

1-5-3 DC Characteristics

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current (without load at output) *6							
1	Power supply current	I_{DD1}	fosc=20.0 MHz V_{DD}=5 V Ta= -40 ºC to +85 ºC (fs=fosc/2)		25	60	mA
2		I_{DD2}	fosc=8.39 MHz V_{DD}=5 V (fs=fosc/2)		10	25	
3		I_{DD3}	fx=32.768 kHz V_{DD}=3 V (fs=fx/4)		30	100	µA
4	Supply surrent during HALT1 mode	I_{DD4}	fx=32.768 kHz V_{DD}=3 V Ta=25 ºC		4	8	
5		I_{DD5}	fx=32.768 kHz V_{DD}=3 V Ta =-40 ºC to +85 ºC			30	
6	Supply current during STOP mode	I_{DD6}	V_{DD}=5 V Ta=25 ºC			2	
7		I_{DD7}	V_{DD}=5 V Ta =-40 ºC to +85 ºC			35	

*8 Measured under conditions without load.

- The supply current during operation, I_{DD1}(I_{DD2}), is measured under the following condi tions : After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 20 MHz(8.39 MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD3}, is measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32.768 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD4}(I_{DD5}), is measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and an 32.768 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD6}, is measured under the following conditions : After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and the OSC1 and XI pins are unconnected.

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD							
8	Input high voltage 1	V_{IH1}		0.8 V_{DD}		V_{DD}	V
9	Input high voltage 2	V_{IH2}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
10	Input low voltage 1	V_{IL1}		0		0.2 V_{DD}	
11	Input low voltage 2	V_{IL2}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
12	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD}			± 10	µA
Input pin 2 P20 and P22 (Schmitt trigger input)							
13	Input high voltage	V_{IH3}		0.8 V_{DD}		V_{DD}	V
14	Input low voltage	V_{IL3}		0		0.2 V_{DD}	
15	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD}			± 10	µA
16	Input current 1	I_{IH3}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
Input pin 3 to 1 P21 (Schmitt trigger input)							
17	Input high voltage	V_{IH4}		0.8 V_{DD}		V_{DD}	V
18	Input low voltage	V_{IL4}		0		0.2 V_{DD}	
19	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD}			± 10	µA
20	Input current 1	I_{IH4}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
Input pin 3 to 2 P21 (When used as ACZ)							
21	High detection voltage	V_{DLH}	Figure 1-5-5			3.5	V
22		V_{DHL}		1.5			
23	Low detection voltage	V_{DHH}		4.5			
24		V_{DLL}				0.5	
25	Input leakage current	I_{LK10}	V_{IN}=0 V to V_{DD}			± 10	µA
26	Input clamp current	I_{C10}	V_{IN}>V_{DD} V_{IN}<0 V			± 400	
ACZ pin							
27	Rising time	t_{rs}	Figure 1-5-5	30			µs
28	Falling time	t_{fs}		30			

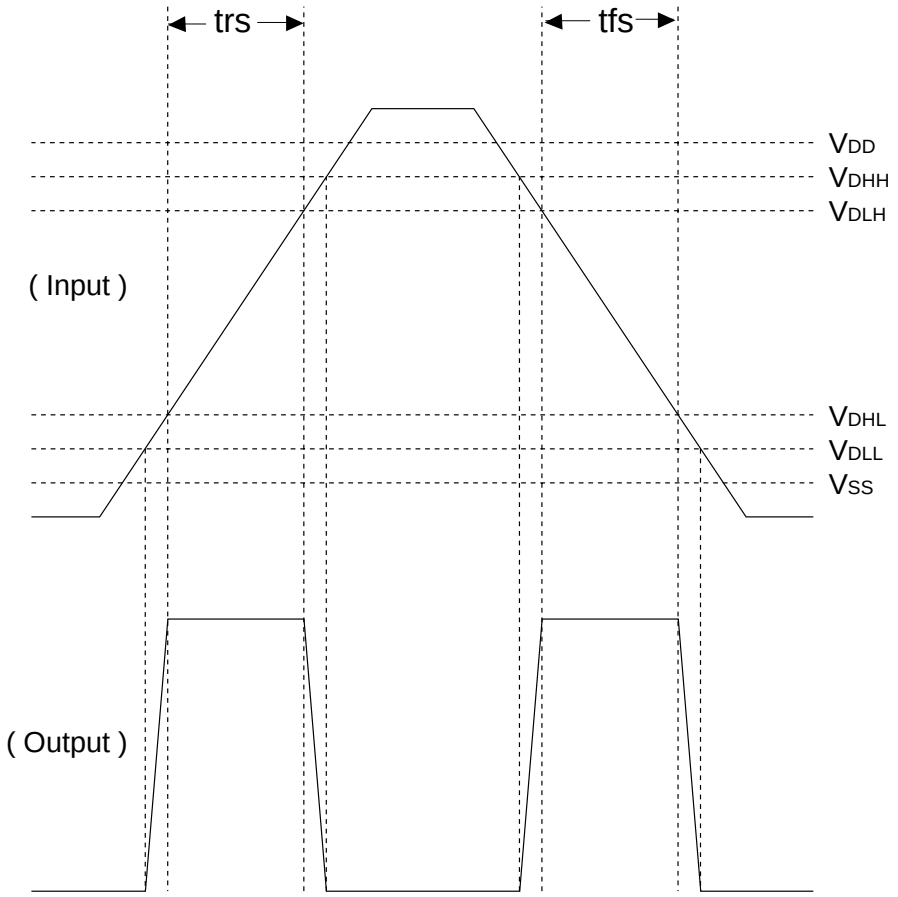


Figure 1-5-5 Operation of AC Zero-Cross Detection Circuit

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input 4 PA0 to PA3							
29	Input high voltage 1	V_{IH5}		0.8 V_{DD}		V_{DD}	V
30	Input high voltage 2	V_{IH6}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
31	Input low voltage 1	V_{IL5}		0		0.2 V_{DD}	
32	Input low voltage 2	V_{IL6}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
33	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD}			± 2	µA
34	Input current 1	I_{IH5}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
35	Input current 2	I_{IL5}	V_{DD}=5.0 V V_{IN}=3.5 V Pull-down resistor ON	30	100	300	
I/O pin 1 P27 (NRST)							
36	Input high voltage	V_{IH7}		0.8 V_{DD}		V_{DD}	V
37	Input low voltage	V_{IL7}		0		0.2 V_{DD}	
38	Input leakage current	I_{LK7}	V_{IN}=0 V to V_{DD}			± 10	µA
39	Input current 1	I_{IH7}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
40	Output low voltage	V_{OL7}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	V
I/O pin 2 P00, P01, P02, P06, P10 to P15, P30 to P33 (Schmitt trigger input)							
41	Input high voltage	V_{IH8}		0.8 V_{DD}		V_{DD}	V
42	Input low voltage	V_{IL8}		0		0.2 V_{DD}	
43	Input leakage current	I_{LK8}	V_{IN}=0 V to V_{DD}			± 10	µA
44	Input current 1	I_{IH8}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
45	Output high voltage	V_{OH8}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
46	Output low voltage	V_{OL8}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	
I/O pin 3 P50 to P53							
47	Input high voltage 1	V_{IH9}		0.8 V_{DD}		V_{DD}	V
48	Input high voltage 2	V_{IH10}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
49	Input low voltage 1	V_{IL9}		0		0.2 V_{DD}	
50	Input low voltage 2	V_{IL10}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
51	Input leakage current	I_{LK9}	V_{IN}=0 V to V_{DD}			± 10	µA
52	Input current 1	I_{IH9}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
53	Output high voltage	V_{OH9}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
54	Output low voltage	V_{OL9}	V_{DD}=5.0 V I_{OL}=15 mA			1.0	
I/O pin 4 P60 to P67 (Schmitt trigger input)							
55	Input high voltage	V_{IH11}		0.8 V_{DD}		V_{DD}	V
56	Input low voltage	V_{IL11}		0		0.2 V_{DD}	
57	Input leakage current	I_{LK11}	V_{IN}=0 V to V_{DD}			± 10	µA
58	Input current 1	I_{IH11}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
59	Input current 2	I_{IH12}	V_{DD}=5.0 V V_{IN}=3.5 V Pull-down resistor ON	30	100	300	
60	Output high voltage	V_{OH11}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
61	Output low voltage	V_{OL11}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	

Ta=-40 ºC to +85 ºC V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 5 P70 to P77							
62	Input high voltage 1	V_{IH13}		0.8 V_{DD}		V_{DD}	V
63	Input high voltage 2	V_{IH14}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
64	Input low voltage 1	V_{IL13}		0		0.2 V_{DD}	
65	Input low voltage 2	V_{IL14}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
66	Input leakage current	I_{LK13}	V_{IN}=0 V to V_{DD}			± 10	µA
67	Input current 1	I_{IH13}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
68	Input current 2	I_{IL13}	V_{DD}=5.0 V V_{IN}=3.5 V Pull-down resistor ON	30	100	300	
69	Output high voltage	V_{OH13}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
70	Output low voltage	V_{OL13}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	
I/O pin 6 P80 to P87							
71	Input high voltage 1	V_{IH15}		0.8 V_{DD}		V_{DD}	V
72	Input high voltage 2	V_{IH16}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
73	Input low voltage 1	V_{IL15}		0		0.2 V_{DD}	
74	Input low voltage 2	V_{IL16}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
75	Input leakage current	I_{LK15}	V_{IN}=0 V to V_{DD}			± 10	µA
76	Input high current	I_{IH15}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
77	Output high voltage	V_{OH15}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
78	Output low voltage	V_{OL15}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	
Boost output pin 1 V_{LC1}, V_{LC2} (boost output)							
79	Output voltage	V_{LC1}	V_{DD}=3 V V_{LCIN3}=1.5 V LCD OFF SEG, COM pins no load	4.3	4.5	4.7	V
80		V_{LC2}		2.8	3.0	3.2	
Display output pin 1 COM0 to COM3							
81	Output impedance	R_{ICOM1}	V_{DD}=5 V ± 0.5 V	-	3	6	kΩ
82		R_{ICOM2}	V_{DD}=3 V ± 0.3 V	-	8	15	
Display output pin 2 SEG0 to SEG23							
83	Output impedance	R_{ISEG1}	V_{DD}=5 V ± 0.5 V	-	15	30	kΩ
84		R_{ISEG2}	V_{DD}=3 V ± 0.3 V	-	30	60	
Dislpay power supply pin 1 V_{LC1}, V_{LC2}, V_{LC3}							
85	Internal divided resistor	R_{VL1}	Ta=+25 ºC (V_{LC3} - V_{SS} impedance)	47.5	95	190	kΩ
Display power supply pin 2 V_{LCIN2}, V_{LCIN3}							
86	Input voltage	V_{LCIN2}	at 3/2 times boost	2 V_{DD}/3		3.6	V
87		V_{LCIN3}	at 3 times boost	V_{DD}/3		1.8	

1-5-4 A/D Converter Characteristics

Ta=-40 °C to +85 °C V_{DD}=2.0 V to 5.5 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Non-linearity error 1		V_{DD}=5.0 V V_{SS}=0 V V_{ref+}=5.0 V V_{ref-}=5.0 V T_{AD}=1.00 µs *7			±3	LSB
3	Differential non-linearity error 1					±3	
4	Zero transition voltage		V_{DD}=5.0 V V_{SS}=0 V V_{ref+}=5.0 V V_{ref-}=5.0 V T_{AD}=1.00 µs		30	100	mV
5	Full-scale transition voltage			4900	4970		
6	A/D conversion time		f_{OSC}=8 MHz T_{AD}=1.00 µs	12		28	µs
7			fx=32.768 kHz T_{AD}=15.2 µs	183.12		427.28	
8	Sampling time		f_{OSC}=8 MHz T_{AD}=1.00 µs	2.0		18.0	
9			fx=32.768 kHz T_{AD}=15.2 µs	30.52		274.68	
10	Reference voltage	V_{ref+}	*	2.0		V_{DD}	V
11		V_{ref-}	*	V_{SS}		3.0	
12	Analog input voltage			V_{ref-}		V_{ref+}	
13	Analog input leakage current		When channel is OFF V_{ADIN}=0 V to 5 V			±2	µA
14	Reference voltage pin input leakage current		When V_{ref+} is OFF $V_{ref-} \leq V_{ref+} \leq V_{DD}$			±10	
15	Ladder resistance	R_{LADD}	V_{DD}=5.0 V	20	50	80	kΩ

*7 T_{AD} means A/D conversion clock cycle.

The values of 2 and 3 are guaranteed on the condition that V_{DD}=V_{ref+}=5 V and V_{SS}=V_{ref-}=0 V.

Note) The gap between V_{ref+} and V_{ref-} should be set over 2 V.

1-6 Cautions for Circuit Setup

1-6-1 General Usage

■Connection of V_{DD} pin, and V_{SS} pin

All of the V_{DD} and V_{SS} pins should be connected directly to the power source and ground in the external. Put them on printed circuit board after the location of LSI (package) pin is considered.
Incorrect connection may lead a fusion and break a microcontroller.

■Cautions for Operation

(1) If you install the product close to high-field emissions (under the cathode ray tube, etc.), shield the package surface to ensure normal performance.

(2) Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, its operation may be executed wrongly.

(3) Operation voltage should be also well considered. Each product has different operating range.
- If the operation voltage is over the operating range, it can be shortened the length of its life.
- If the operation voltage is below the operating range, the operation may be executed wrongly.

1-6-2 Unused Pins

■Unused Pins (output exclusive pins and LCD output pins)
Set unused pins (output exclusive pins and LCD output pins) open.

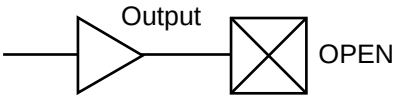


Figure 1-6-1 Unused Pins (output exclusive pins and LCD output pins)

■Unused Pins (only for input)
Insert some 10 kΩ resistor to unused pins (only for input) for pull-up or pull-down. If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

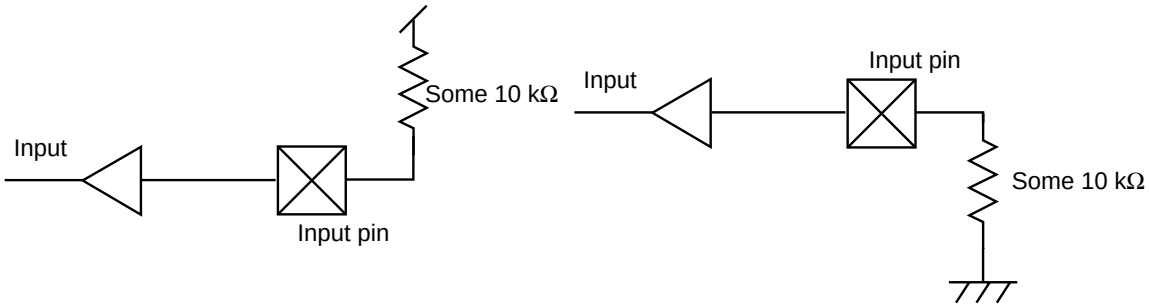


Figure 1-6-2 Unused Pins (only for input)

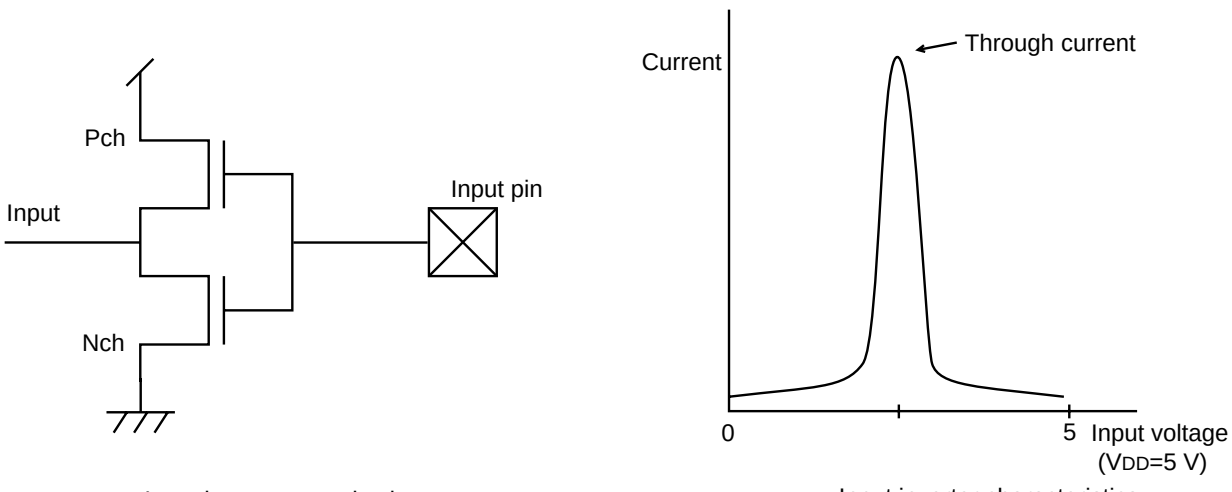


Figure 1-6-3 Input Inverter Organization and Characteristics

■Unused pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor : output off) at reset, to stabilize input, set some 10 kΩ resistor to be pull-up or pull-down. If the output is on at reset, set them open.

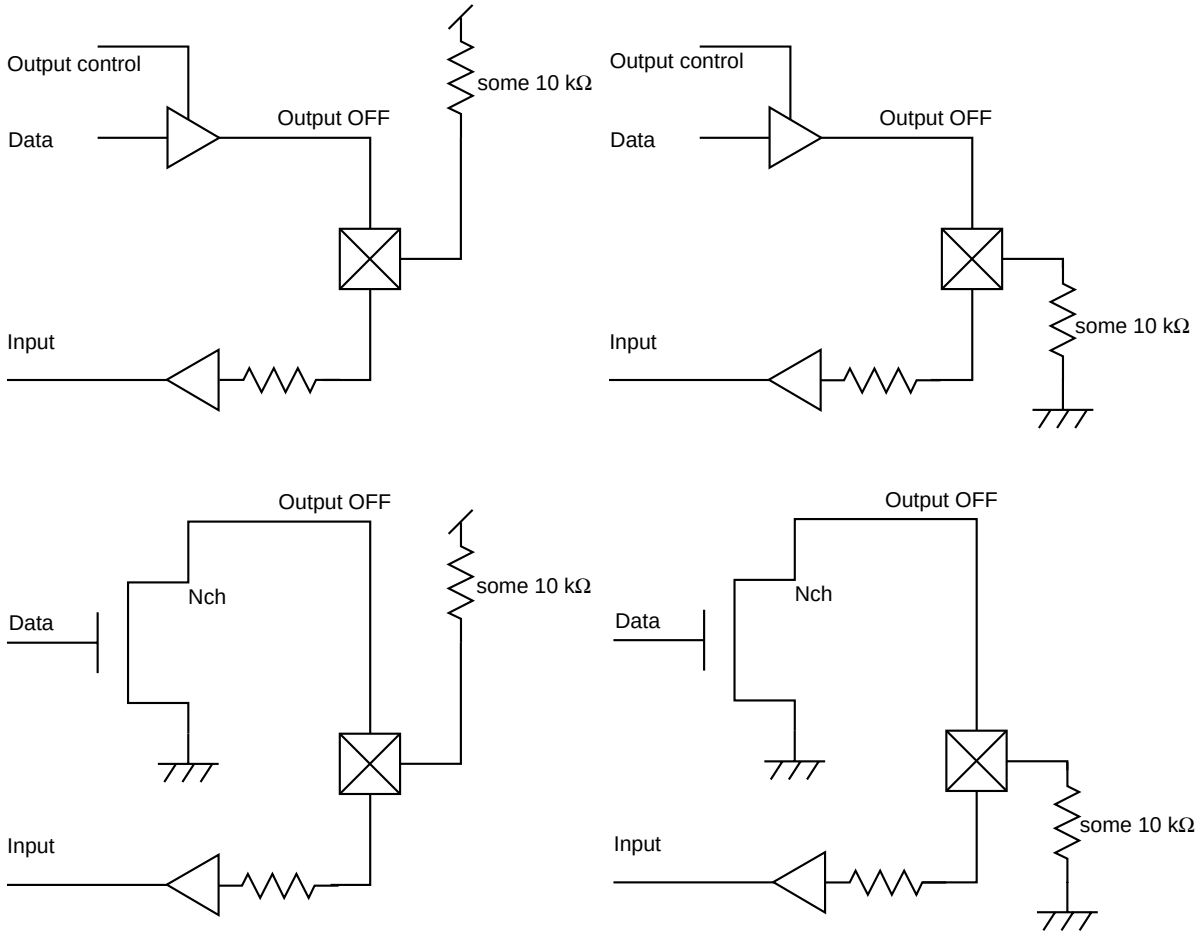


Figure 1-6-4 Unused I/O pins (high impedance output at reset)

1-6-3 Power Supply

■The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If the input voltage supplies before V_{DD} is on, a latch up occurs and causes the destruction of micro controller by a large current flow.

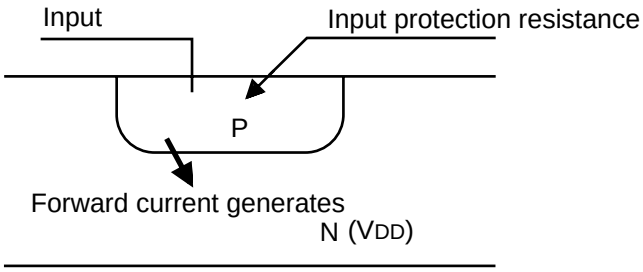


Figure 1-6-5 V_{DD} and Input Pin Voltage

■The Relation between V_{DD} and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising , in order to be recognized as a reset signal.

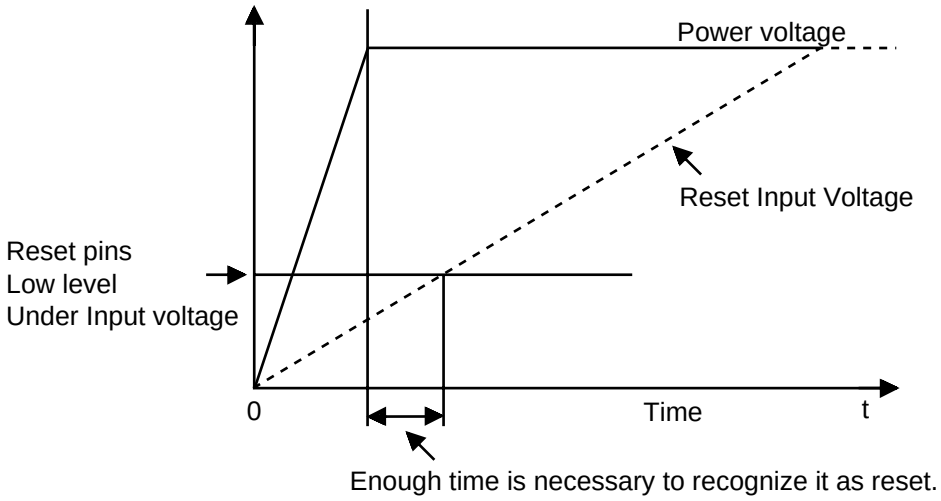


Figure 1-6-6 Power Supply and Reset Input Voltage

1-6-4 Power Supply Circuit

■Cautions for Setting Circuits with VDD

The MOS logic such a microcomputer is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver. Figure 1-6-6 shows an example for a circuit with VDD (Emitter follower type).

■An Example for a Circuit of VDD Supply Employing Emitter Follower Type

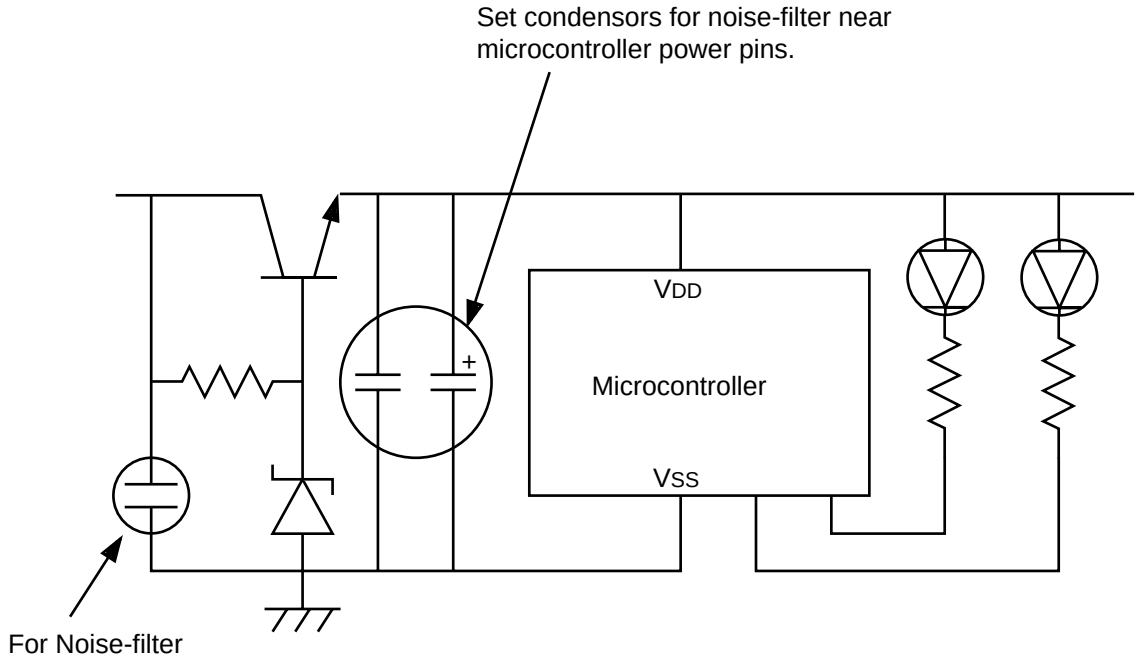


Figure 1-6-7 An Example for a Circuit of VDD Supply (Emitter follower type)

1-6-5 Oscillators

This LSI's oscillation clock can be used with a ceramic and crystal Oscillator.

■Recomended Oscillators

Figure 1-6-8 shows basic configuration connected with a ceramic Oscillator and table 1-6-1 shows recommended Oscillators and the circuit constant.

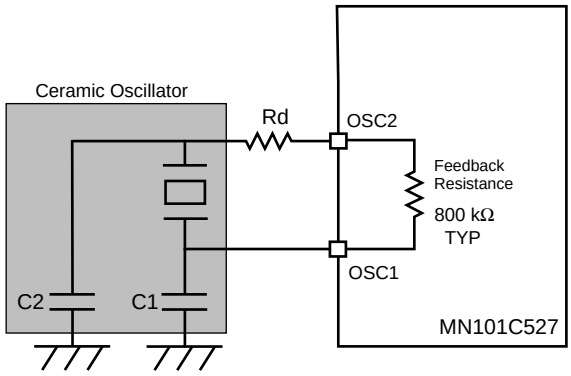


Figure 1-6-8 Basic Configuration Connected with a Ceramic Oscillator

Table 1-6-1 Recommended Ceramic Oscillator and the Circuit Cosntant

Manufacturer	Frequency	Part Number	Recommended circuit constant			
			Load Capacity		Dumping Resistance Rd (Ω)	Feedback Resistance Rd (Ω)
			C1[pF]	C2[pF]		
Matsushita Electronic Components Co., Ltd.	2 MHz	EFOMC2004A4	33	33	3.3 k	-
	4 MHz	EFOMC4004A4	33	33	1.0 k	-
	8 MHz	EFOMC8004A4	33	33	560	-
	16 MHz	EFOMC1605A4	33	33	0	-
	20 MHz	EFOMC2005A4	33	33	0	-
Murata Manufacturing Company, Ltd.	2 MHz	CSTLS2M00G56-B0	47	47	Open	470
		CSTCC2.00MG0H6	47	47	Open	470
	4 MHz	CSTS0400MG06	47	47	Open	-
		CSTCR4M00G55-R0	39	39	Open	-
	8 MHz	CSTS0800MG06	47	47	Open	-
		CSTCC8.00MG0H6	47	47	Open	-
	16 MHz	CSALS16M0X55-B0	7 *1	7 *1	Open	-
		CSTCV16.00MXJ0C1	5	5	Open	-
	20 MHz	CSTLS20M0X51-B0	5	5	33 k	-
		CSTCV20.00MXJ0H1	5	5	15 k	-

Above recommended ranges are result obtained from unit oscillating evaluation of this LSI.
After evaluate the actual oscillating on the target board, dumping resistance may be set, if necessary.

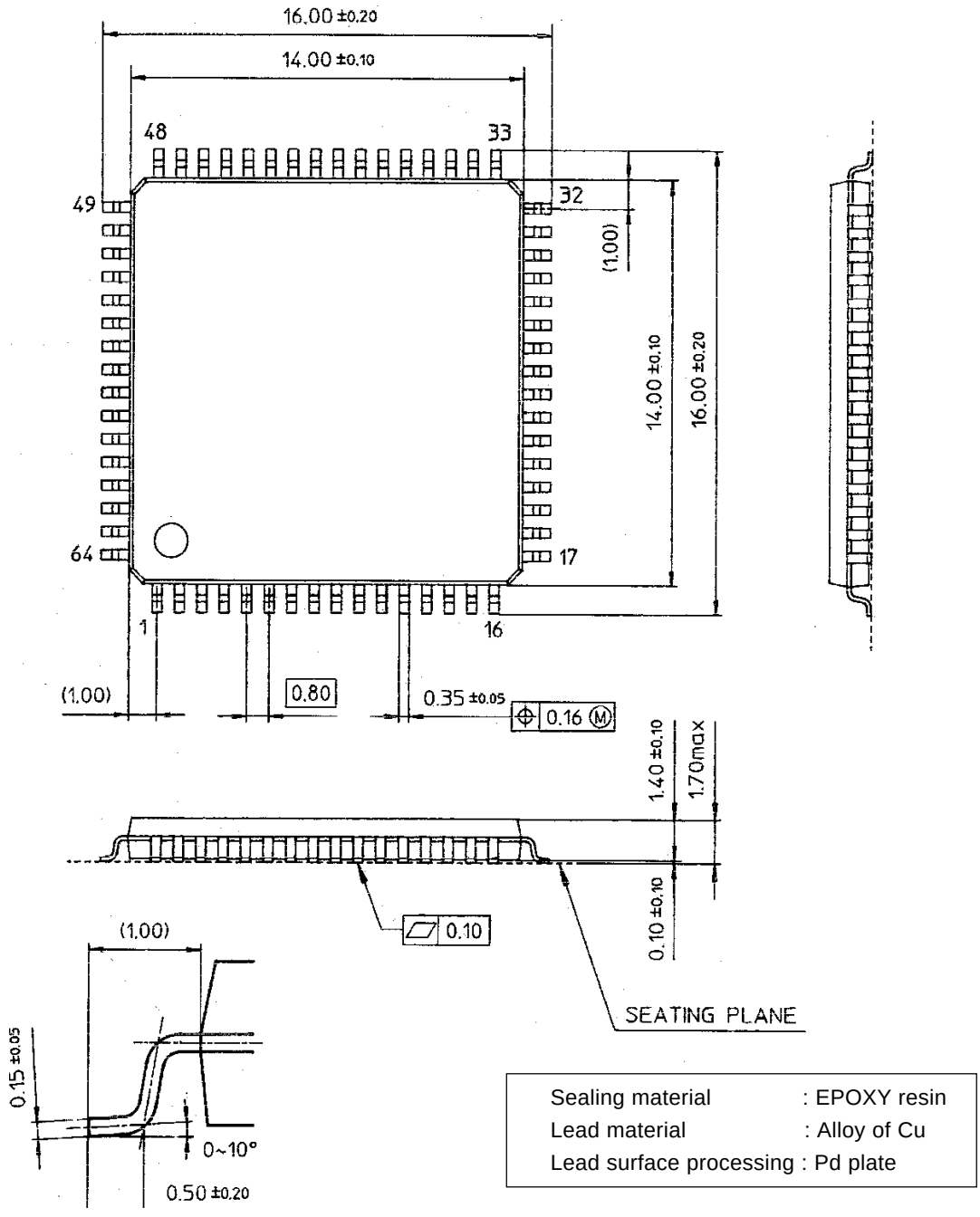
We do not evaluate oscillating of crystal Oscillator on this LSI. Set the circuit constant as is recommendation of the Oscillator manufacturer.

Circuit constant of each ceramic or crystal Oscillator, which is connected to OSC1/OSC2 or XI/XO, differs depending on stray capacitance of the oscillator or on the mounting circuit. So consult the Oscillator manufacturer for the appropreate circuit constant.

1-7 Package Dimension

Package Code: LQFP064-P-1414

Units : mm



Sealing material	: EPOXY resin
Lead material	: Alloy of Cu
Lead surface processing	: Pd plate

Figure 1-7-1 64-Pin LQFP

The package dimension is subjected to change. Before using this product, please obtain product specifications from the sales office.

1-8 Operation Mode Check List

Date:

SE No.

Model Name	MN101C527	Customer		Counter-sign	

1. Supply voltage operating range

CPU Operation	Used	Unused	Supply Voltage during Operation
Atr High Speed OSC1 Operation			V to V
At Low Speed XI Operation			V to V
At HALT0			V to V
At HALT1			V to V
At STOP			V to V

2. Type and frequency of oscillation input

Type	System Clock OSC1 Input	Timer Clock XI Input
External Clock		
Crystal		
Ceramic		
Frequency	MHz	kHz
Unused		

3. System operating clock

OSC1 Only	
Switching OSC1 and XI	

4. Setting of oscillation divider

Normal mode		Slow mode	
2 divide		2 divide	
4 divide		8 divide	
8 divide		32 divide	
16 divide			
32 divide			
64 divide			

5. LCD display mode

LCD unused	
Static	
1/2 duty, 1/2bias	
1/3 duty, 1/3 bias	
1/4 duty, 1/3 bias	

6. LCD power supply

LCD active	Voltage booster circuit active	At 2 times, 3 times boost		V_{LC3}= V
		At 2/3 times, 1/2 times boost		V_{LC2}= V
		At 2 times boost		V_{LC2}=V_{LC3}= V
		Unused		
	Internal voltage divider active			V_{LC1}= V
	External voltage divider active	R= kΩ		V_{LC1}= V
LCD unused				

When placing an order for masks, please present this document.

Chapter 2 Basic CPU

2-1 Overview

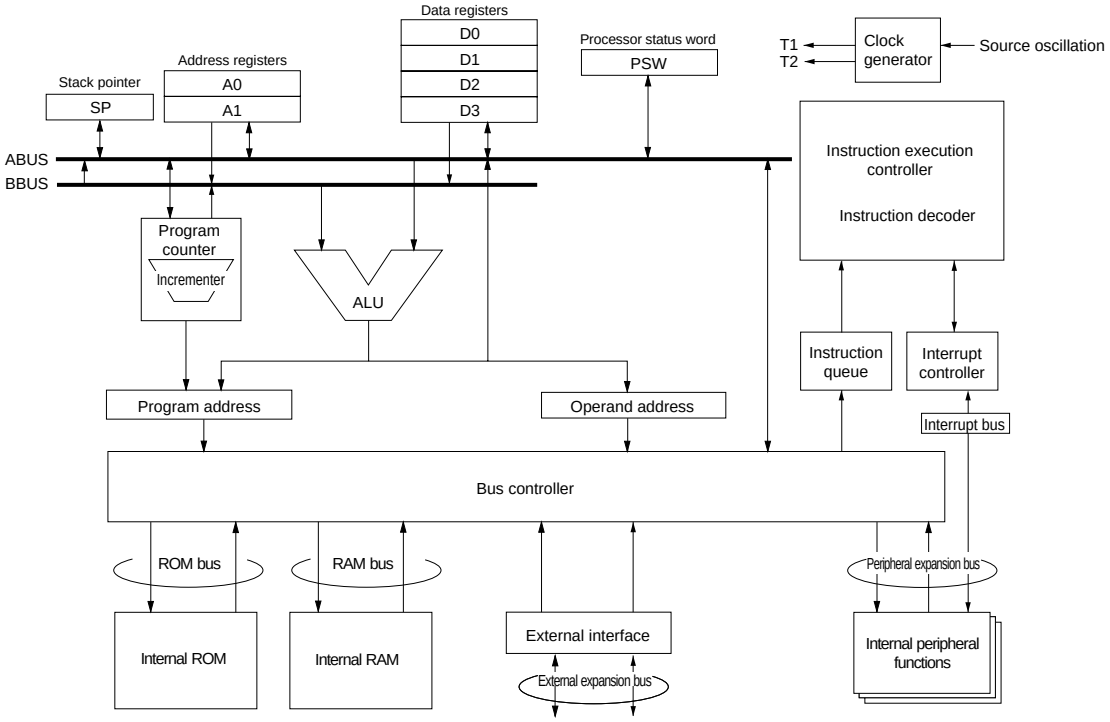
The MN101C series has a flexible optimized hardware configuration as an embedded microcomputer and a simple, efficient instruction set for both economy and speed. Specific features are as follows:

1. Minimized code sizes with instruction lengths based on 4-bit increments
   The series keeps code sizes down by adopting a basic instruction length of one byte and variable word lengths based on 4-bit increments. As a result, the series minimizes code sizes in spite of its simple instruction set limiting data transfers to and from memory to load/store operations.
2. Minimum instruction execution time of one cycle in this LSI is 100 ns .
3. Minimized register set that simplifies the architecture and supports C language
   The instruction set has been determined, depending on the size and capacity of hardware, after an analysis of embedded application programing code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler. [☞ MN101C LSI User's Manual" (Architecture Instructions)]

Table 2-1-1 Basic Specifications

Structure	Load / store architecture	
	Six registers	Data : 8-bit x 4 Address : 16-bit x 2
	Other	PC : 19-bit PSW : 8-bit SP : 16-bit
Instructions	Number of instructions	37
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte x n (0≤n≤9)
Basic performance	Internal operating frequency (max)	10 MHz
	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycles
	Load / store	Min. 2 cycles
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	256 KB (max. 64 KB for data)	
	Instruction / data common space	
External bus	Address	18-bit (max.)
	Data	8-bit
	Minimum bus cycle	1 clock (100 ns)
Interrupt	Vector interrupt	3 interrupt levels
Low-power dissipation mode	STOP mode	
	HALT mode	

2-1-1 Block Diagram



Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic oscillator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, D/A converter, etc.). Peripheral functions vary with model.

Figure 2-1-1 Block Diagram and Function

2-1-2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (x'03F00' to x'03FFF') with memory-mapped I/O. CPU control registers are also located in this memory space.

Table 2-1-2 CPU Control Registers

Address	Registers	R/W	Function
X'3F00'	CPUM	R/W*1	CPU mode control register
X'3F01'	MEMCTR	R/W	Memory control register
X'3F0A'	Reserved		
X'3F0B'	Reserved		
X'3F0D'	Reserved		
X'3FE0'	Reserved (for debugger)		
X'3FE1'	NMICR	R/W	Non maskable interrupt control register [☞ Chapter 3]
X'3FE2' to X'3FFE'	xxxICR	R/W	Mascable interrupt control register [☞ Chapter 3]
X'3FFF'	Reserved (For reading out interrupt vector data in interrupt process)		

* Part of the register is only readable

2-1-3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

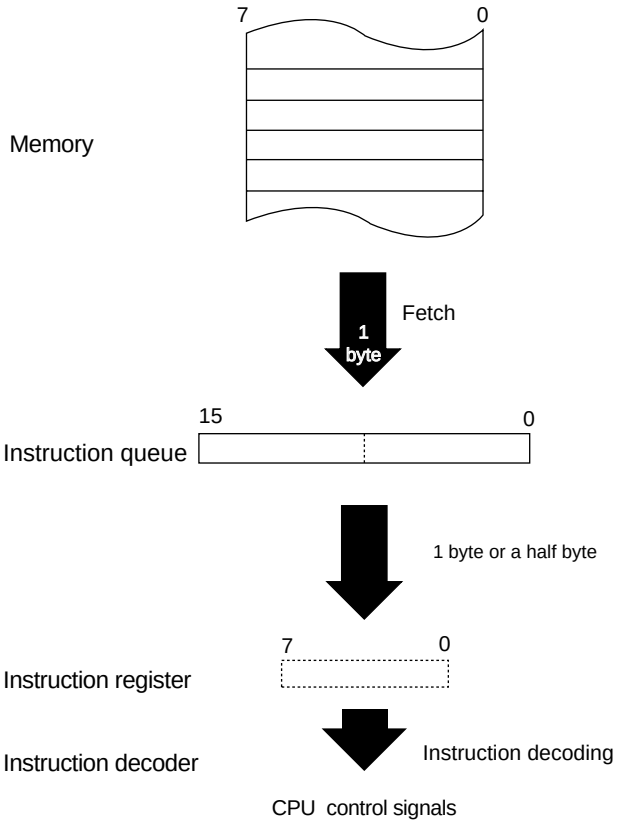


Figure 2-1-2 Instruction Execution Controller Configuration

2-1-4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, which are given nonstop. Pipeline process realizes speedy processing of consective instructions/ executions. This process is executed with instruction queue and instruction decoder.

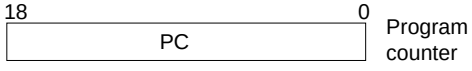
Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate (imm) are needed at the first cycle of the next instruction execution. But on some other instruction such a branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

Instruction queue is controlled automatically by hardware so that there is no need to control by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2-1-5 Registers for Address

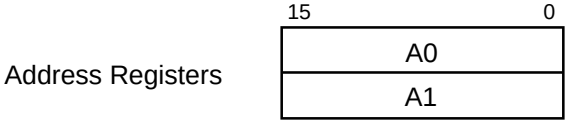
Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP).

■Program Counter (PC)
This register gives the address of the currently executing instruction. It is 19 bits wide to provide access to a 256 KB address space in half byte(4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 4000.



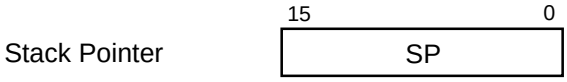
■Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2-byte data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.



■Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. Ar reset, the value of SP is undefined.



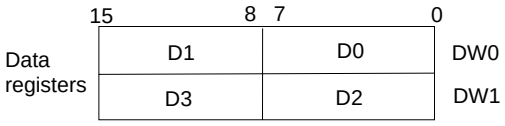
2-1-6 Registers for Operation

Registers for operation include four data registers (D0, D1, D2, D3).

■Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory.

The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.



2-1-7 Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when the interrupt service routine returns.

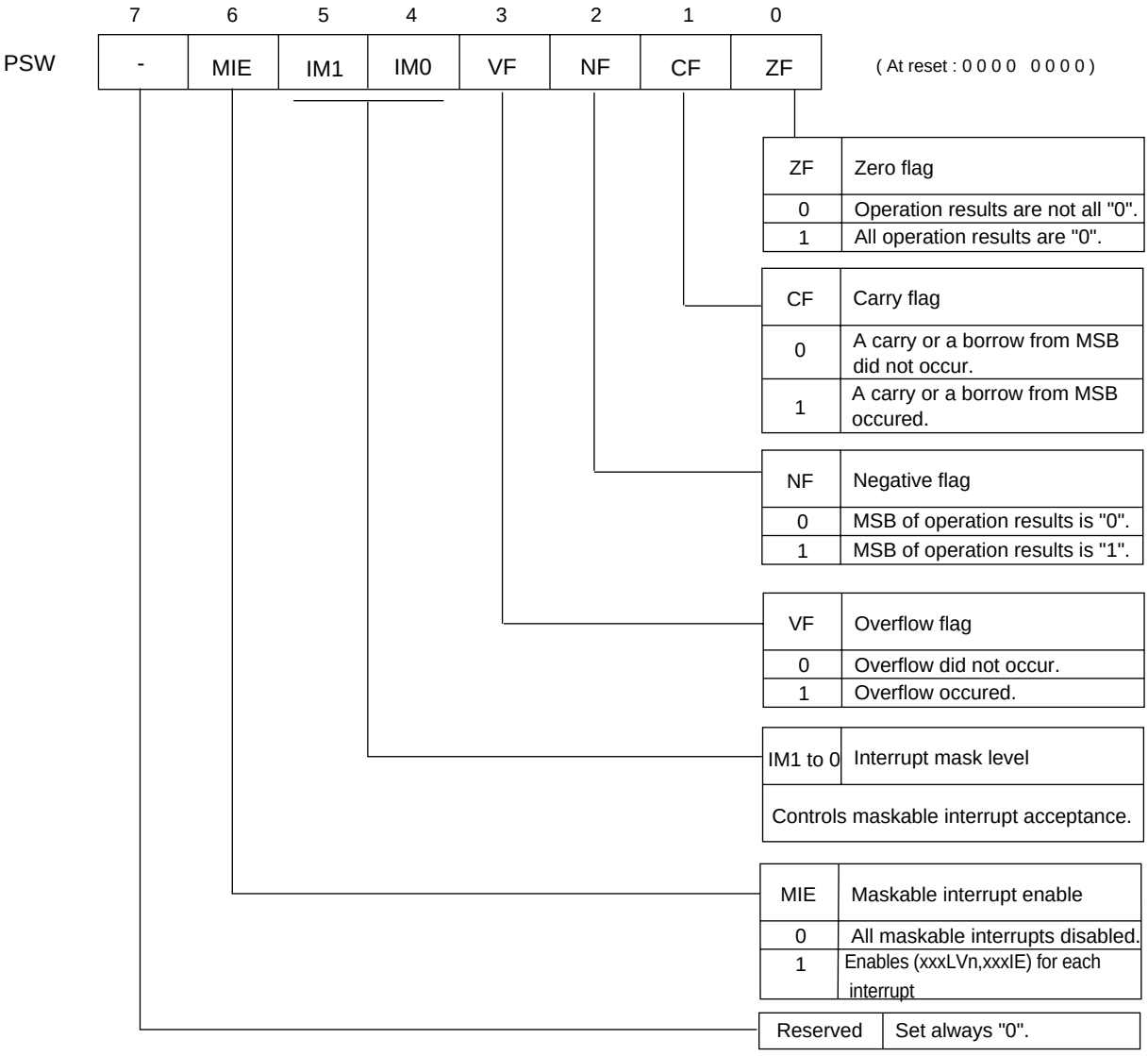

7 6 5 4 3 2 1 0
PSW
- MIE IM1 IM0 VF NF CF ZF
(At reset : 0 0 0 0 0 0 0 0)
ZF Zero flag
0 Operation results are not all "0".
1 All operation results are "0".
CF Carry flag
0 A carry or a borrow from MSB did not occur.
1 A carry or a borrow from MSB occured.
NF Negative flag
0 MSB of operation results is "0".
1 MSB of operation results is "1".
VF Overflow flag
0 Overflow did not occur.
1 Overflow occured.
IM1 to 0 Interrupt mask level
Controls maskable interrupt acceptance.
MIE Maskable interrupt enable
0 All maskable interrupts disabled.
1 Enables (xxxLVn,xxxIE) for each interrupt
Reserved Set always "0".

Figure 2-1-3 Processor Status Word(PSW)

■Zero Flag (ZF)
Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■Carry Flag (CF)
Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■Negative Flag (NF)
Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■Overflow Flag (VF)
Overflow flag (VF) is set to "1", when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0".
Overflow flag is used to handle a signed value.

■Interrupt Mask Level (IM1 and IM0)
Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The two-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLVn) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the level is reset to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table 2-1-3 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt levels
	IM1	IM0		
Mask level 0	0	0	High	Non-maskable interrupt (NMI) only
Mask level 1	0	1	.	NMI, Level 0
Mask level 2	1	0	.	NMI, Level 0 to 1
Mask level 3	1	1	Low	NMI, Level 0 to 2

■Maskable Interrupt Enable (MIE)
Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. A '1' enables maskable interrupts; a '0' disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW.
This flag is not changed by interrupts.

2-1-8 Addressing Modes

This LSI supports the nine addressing modes.

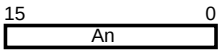
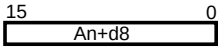
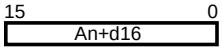
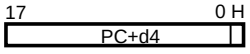
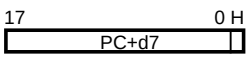
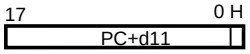
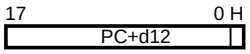
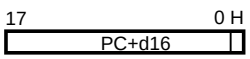
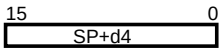
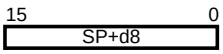
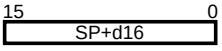
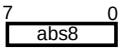
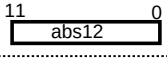
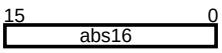
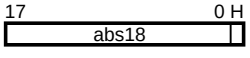
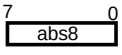
Each instruction uses a combination of the following addressing modes.

1) Register direct
2) Immediate
3) Register indirect
4) Register relative indirect
5) Stack relative indirect
6) Absolute
7) RAM short
8) I/O short
9) Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combining handy addresssing with absolute addressing reduces code size. For transfer data between memory, 7 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101C series.

This LSI is designed for 8-bit data access. It is possible to tranfer data in 16-bit increments by specifying either all odd or all even addresses.

Table 2-1-4 Addressing Modes

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	-	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	-	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)		Specifies the address using an address register.
Register relative indirect	(d8, An)		Specifies the address using an address register with 8-bit displacement.
	(d16, An)		Specifies the address using an address register with 16-bit displacement.
	(d4, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4, SP)		Specifies the address using the stack pointer with 4-bit displacement.
	(d8, SP)		Specifies the address using the stack pointer with 8-bit displacement.
	(d16, SP)		Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)		Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)		
	(abs16)		
	(abs18) (branch instructions only)	 * 1	
RAM short	(abs8)		Specifies an 8-bit offset from the address x'00000'.
I/O short	(io8)		Specifies an 8-bit offset from the top address (x'03F00') of the special function register area.
Handy	(HA)	-	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

* 1 H: half-byte bit

2-2 Memory Space

2-2-1 Memory Mode

ROM is the read only area and RAM is the memory area which contains readable/writable data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101C52 series supports one memory mode (single chip mode) in its memory model.

Table 2-2-1 Memory Mode Setup

Memory mode	MMOD pin	EXMEM flag in (MEMCTR register)
Single chip mode	L	0

Set the MMOD pin always to "L" level.

2-2-2 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory model and allows construction of systems with the highest performance.

The single-chip mode uses only internal ROM and internal RAM. The MN101C series devices offer up to 12 KB of RAM and up to 240 KB of ROM. This LSI offers 1536 bytes of RAM and 16 KB of ROM.

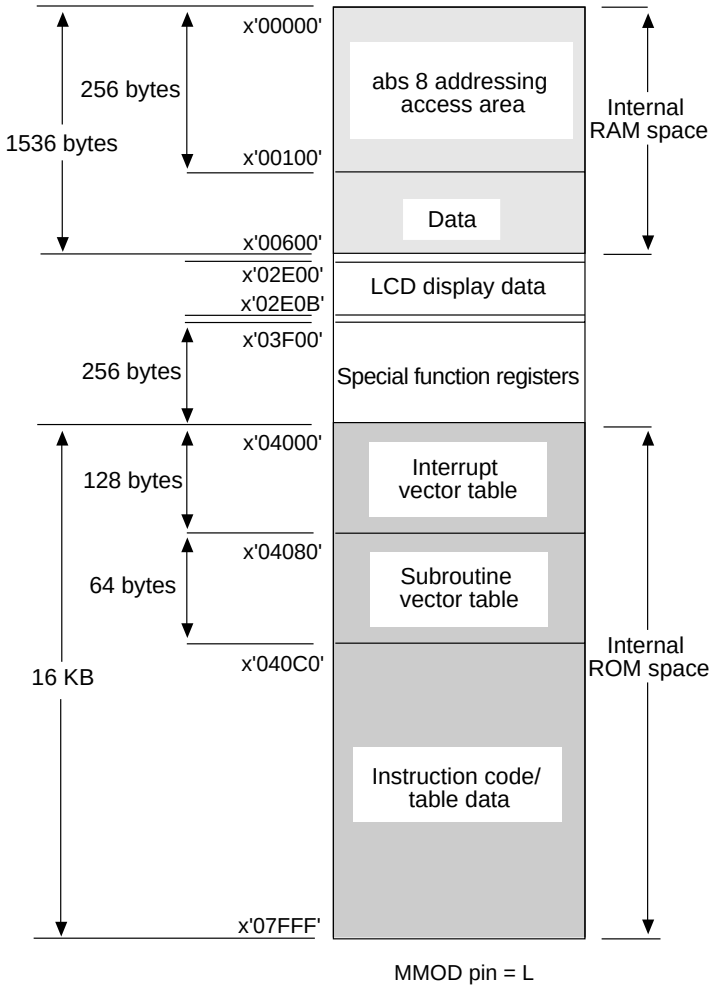


Figure 2-2-1 Single-chip Mode

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before it is used.

2-2-3 Special Function Registers

The MN101C series locates the special registers (I/O spaces) at the address x'03F00' to x'03FFF' in memory space. The special function registers of this LSI are located as shown below.

Table 2-2-3 Register Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
03F0X	CPUM	MEMCTR	WDCTR	DLYCTR	Reserved		Reserved			Reserved	Reserved	Reserved			CPU mode,memory control	
03F1X	P0OUT	P1OUT	P2OUT	P3OUT		P5OUT	P6OUT	P7OUT	P8OUT		PAOUT				PORT output	P1OMD
03F2X	P0IN	P1IN	P2IN	P3IN		P5IN	P6IN	P7IN	P8IN		PAIN				PORT input	P5OMD
03F3X	P0DIR	P1DIR		P3DIR		P5DIR	P6DIR	P7DIR	P8DIR		PAIMD	PADIR			I/O mode control	P6IMD
03F4X	P0PLU	P1PLU	P2PLU	P3PLU		P5PLU	P6PLUD	P7PLUD	P8PLU		PAPLUD				Registor control	
03F5X	TM0BC	TM1BC	TM0OC	TM1OC	TM0MD	TM1MD	CK0MD	CK1MD	TM2BC	TM3BC	TM2OC	TM3OC	TM2MD	TM3MD	CK2MD	CK3MD
03F6X									TM6BC	TM6OC	TM6MD	TBCLR	TM7MD3	TM8MD3	RMCTR	PSCMD
03F7X	TM7BCL	TM7BCH	TM7OC1L	TM7OC1H	TM7PR1L	TM7PR1H	TM7ICL	TM7ICH	TM7MD1	TM7MD2	TM7OC2L	TM7OC2H	TM7PR2L	TM7PR2H		
03F8X	TM8BCL	TM8BCH	TM8OC1L	TM8OC1H	TM8PR1L	TM8PR1H	TM8ICL	TM8ICH	TM8MD1	TM8MD2					NFCTR	EDGDT
03F9X	SC0MD0	SC0MD1	SC0MD2	SC0MD3	RXBUF0	TXBUF0	SC0ODC	SC0CKS								
03FAX																
03FBX	ANCTR0	ANCTR1	ANCTR2	ANBUF0	ANBUF1											
03FCX																
03FDX										LCDMD1	LCDMD2	LCCTR1	LCCTR2			
03FEX		NMICR	IRQ0ICR	IRQ1ICR	IRQ2ICR		IRQ4ICR			TM0ICR	TM1ICR	TM2ICR	TM3ICR			TM6ICR
03FFX	TBICR	TM7ICR	TM7OC2 ICR	TM8ICR		SC0RICR	SC0TICR				ADICR					

2-3 Bus Interface

2-3-1 Bus Controller

The MN101C series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads and thus realize faster operation.

There are four such buses: ROM bus, RAM bus, and peripheral expansion bus (I/O bus). They are connected to the internal ROM, internal RAM, internal peripheral circuits, and external interfaces respectively. The bus control block controls the parallel operation of instruction read and data access, the access speed adjustment for low-speed external devices, and arbitration of bus access when using master devices on the external bus lines. A functional block diagram of the bus controller is given below.

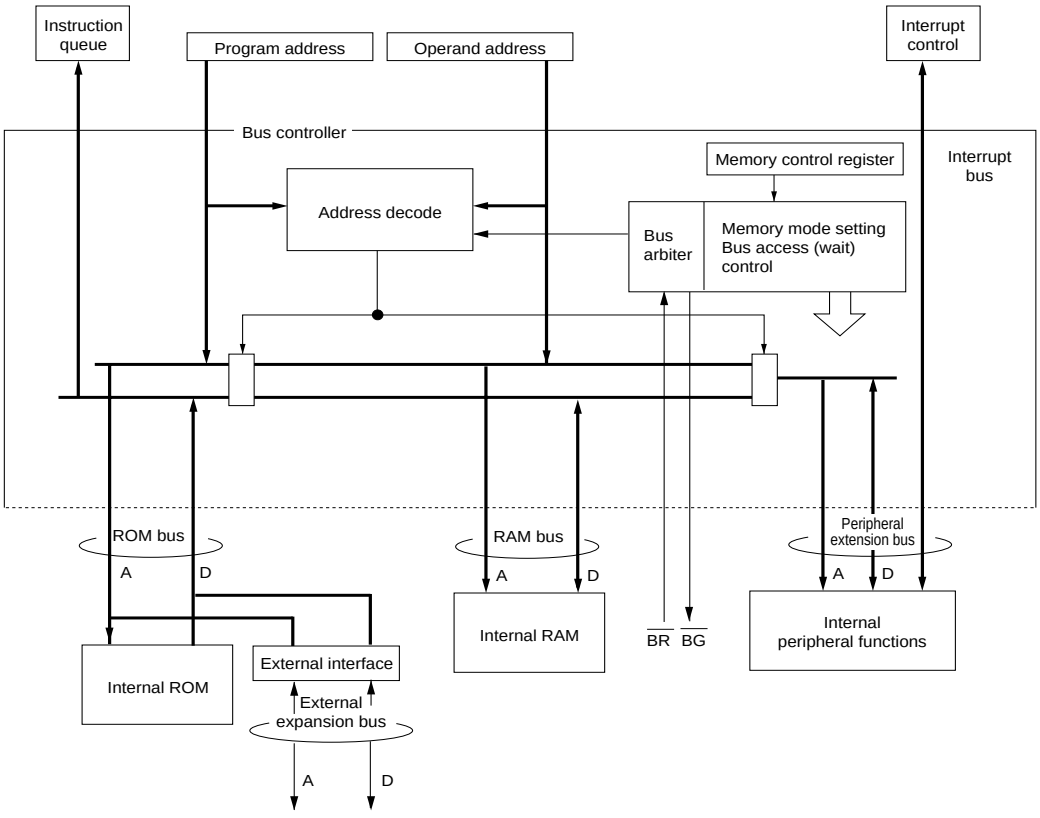


Figure 2-3-1 Functional Block Diagram of the Bus Controller

2-3-2 Control Registers

Bus interface is controlled by two registers : the memory control register (MEMCTR) and the expansion address register (EXADV).

■Memory Control Register (MEMCTR)

	7	6	5	4	3	2	1	0	
MEMCTR	IOW1	IOW0	IVBM	EXMEM	RESERVED	IRWE	EXW1	EXW0	(At reset : 1 1 0 0 1 0 1 1)

RESERVED	Set always "11".

IRWE	Set software write for interrupt request flag
0	Writing software is forbidden When data is written to each interrupt control register (xxxICR), the state of the interrupt request flag (xxxIR) will not change.
1	Software write enable

RESERVED	Set always "1".

EXMEM	Set always "0".

IVBM	Base address setting for interrupt vector table
0	Interrupt vector base = x'04000'
1	Interrupt vector base = x'00100'

IOW1 to 0	Set number of wait cycles when accessing special register area	Bus cycle at 20 MHz oscillation
0 0	No wait cycles	100 ns
0 1	1 wait cycle	150 ns
1 0	2 wait cycles	200 ns
1 1	3 wait cycles	250 ns

Figure 2-3-2 Memory Control Register (MEMCTR: x'3F01' R/W)

The IOW1-IOW0 wait settings affect accesses to the special registers located at the addresses x'3F00'-x'3FFF'. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" for high performance system construction.

2-4 Standby Function

2-4-1 Outline

This LSI has two sets of system clock oscillator pins (high- and low-frequency) for two CPU operating modes (NORMAL and SLOW), each with two standby modes (HALT and STOP).

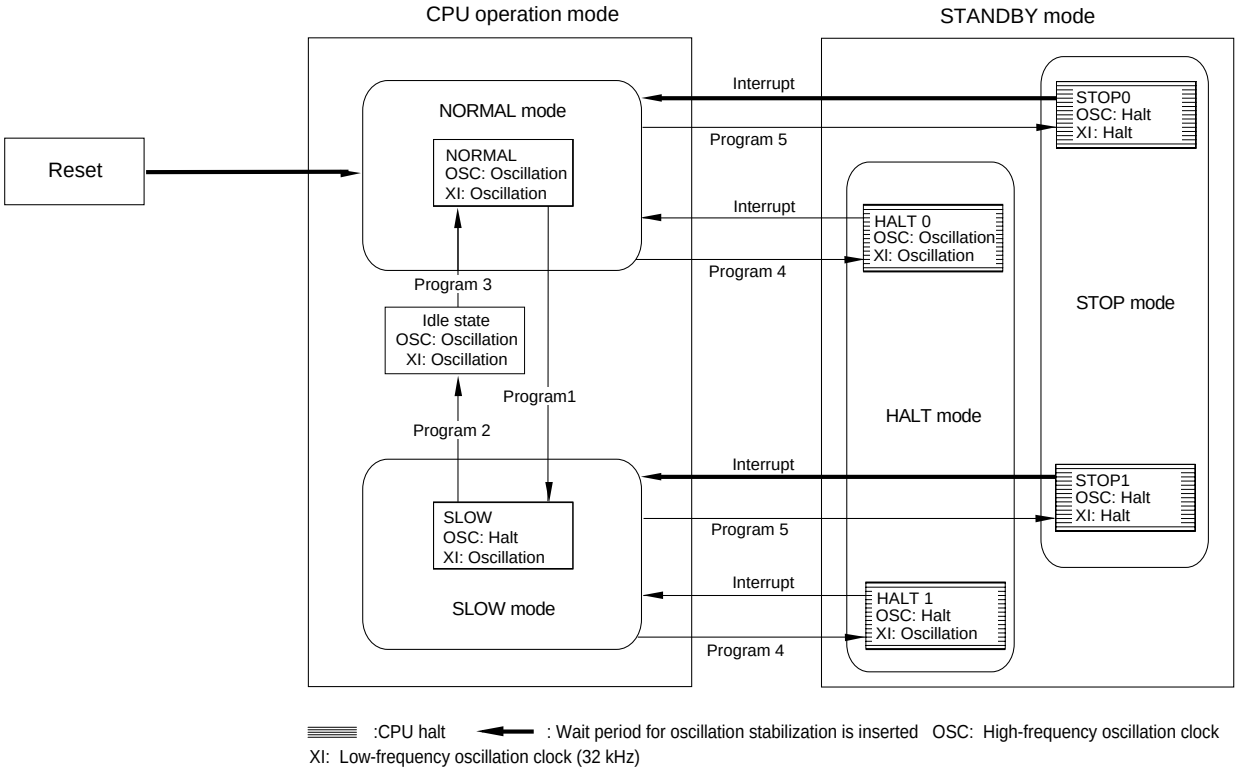


Figure 2-4-1 Transition Between Operation Modes

■HALT Modes (HALT0, HALT1)

– The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1.
– An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1.

■STOP Modes (STOP0, STOP1)

– The CPU and both of the oscillators stop operating.
– An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■SLOW Mode

– This mode executes the software programs using the low-frequency clock. Since the high-frequency oscillator is turned off, the device consumes less power while executing the software.

■IDLE Mode

– This mode allows time for the high-frequency oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

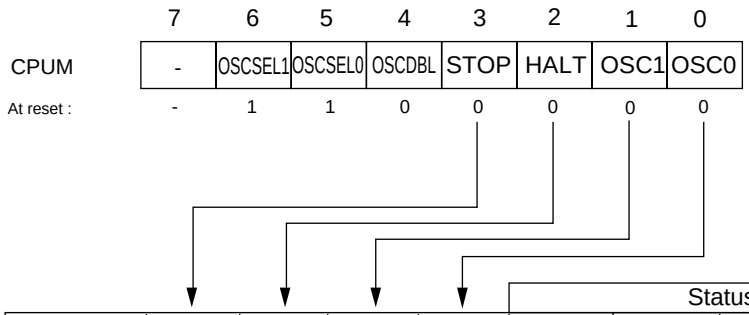
To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.

This LSI has two system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

To stabilize the synchronization at the moment of switching clock speed between high-frequency and low-frequency, high-frequency oscillation frequency (fosc) should be set to 2.5 times or higher frequency than the low-frequency oscillation frequency (fx).

2-4-2 CPU Mode Control Register

Transition to other modes is controlled by operating the related flags in the CPU mode control register (CPUM).



Operation mode	STOP	HALT	OSC1	OSC0	Status: OSCI /OSCO	Status: XI/XO	Status: System clock	Status: CPU
NORMAL	0	0	0	0	Oscillation	Oscillation	OSCI	Operating
IDLE	0	0	0	1	Oscillation	Oscillation	XI	Operating
SLOW	0	0	1	1	Halt	Oscillation	XI	Operating
HALT0	0	1	0	0	Oscillation	Oscillation	OSCI	Halt
HALT1	0	1	1	1	Halt	Oscillation	XI	Halt
STOP0	1	0	0	0	Halt	Halt	Halt	Halt
STOP1	1	0	1	1	Halt	Halt	Halt	Halt

Figure 2-4-2 Operating Mode Control and Clock Oscillation On/Off (CPUM : x'3F00', R/W)

The procedure for transition from NORMAL to HALT or STOP mode is shown below.

(1) If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.
(2) Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR) , set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.
(3) Set CPUM to HALT or STOP mode.

IRWE flag of Memory control (MEMCTR) should be set for interrupt request flag to be cleared by software.

System clock (fs) is changed depending on CPU operation mode.
In NORMAL mode, HALT0 mode, fs is based on fosc (high speed oscillation). In SLOW mode, IDLE mode, HALT1 mode, fs is based on fx (low speed oscillation). [☞ Chapter 2 2-5 Clock Switching]

2-4-3 Transition between SLOW and NORMAL

This LSI has two CPU operating modes, NORMAL and SLOW. Transition from SLOW to NORMAL requires passing through an idle state.

A sample program for transition from NORMAL to SLOW mode is shown below.

```
Program 1
        MOV   x'3', D0          ; Set SLOW mode.
        MOV   D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through the idle state is not necessary.
For transition from the SLOW to NORMAL mode, the program must maintain the idle state until high-frequency clock oscillation is fully stable. In the idle state, the CPU operates on the low-frequency clock.

This stabilization time is the same as that required after a reset, but here the program must do the counting.
We recommend selecting the oscillation stabilization interval after consulting with the oscillator manufacturer.

Sample program for transition from SLOW to NORMAL mode is shown below.

```
Program 2
                MOV         x'01', D0           ; Set IDLE mode.
                MOV         D0, (CPUM)
```

```
Program 3
        MOV     x'0B', D0       ; A loop to keep approx. 6.7 ms with low-frequency clock (32 kHz)
LOOP    ADD     -1, D0          ; operation when changed to high-frequency clock (20 MHz).
        BNE     LOOP            ;
        SUB     D0, D0          ;
        MOV     D0, (CPUM)      ;  Set NORMAL mode.
```

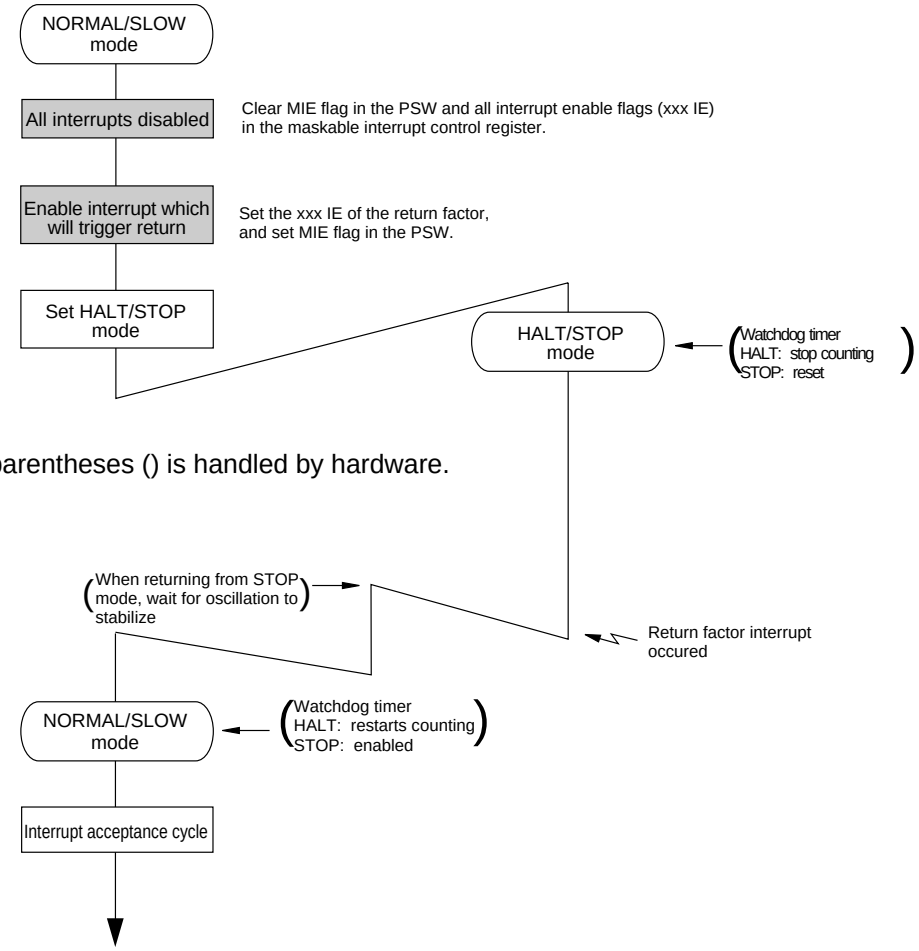
2-4-4 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return.

To initiating a transition to a STANDBY mode, the program requires in advance to,

(1) Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.

(2) Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.


NORMAL/SLOW mode
All interrupts disabled
Clear MIE flag in the PSW and all interrupt enable flags (xxx IE) in the maskable interrupt control register.
Enable interrupt which will trigger return
Set the xxx IE of the return factor, and set MIE flag in the PSW.
Set HALT/STOP mode
HALT/STOP mode
(Watchdog timer HALT: stop counting STOP: reset)
(When returning from STOP mode, wait for oscillation to stabilize)
Return factor interrupt occured
NORMAL/SLOW mode
(Watchdog timer HALT: restarts counting STOP: enabled)
Interrupt acceptance cycle

Processing inside parentheses () is handled by hardware.

Figure 2-4-3 Transition to/from STANDBY Mode

If the interrupt is enabled and interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.

■Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

Program 4

```
        MOV     x'4',  D0      ; Set HALT mode.
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

■Transition to STOP mode

The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

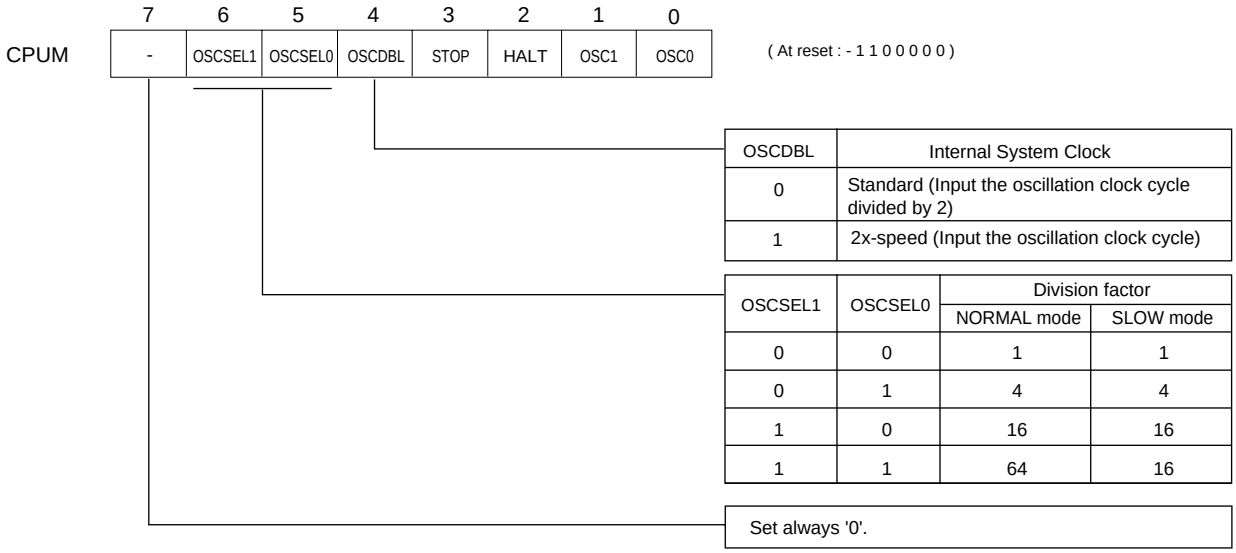
Program 5

```
        MOV     x'8',  D0      ; Set STOP mode
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

Insert three nop instructions right after the instruction of transition to HALT, SLOW modes.

2-5 Clock Switching

This LSI can select the best operation clock for system by switching clock cycle division rate through program. Division rate is determined by both flags of the CPU mode control register (CPUM). At the highest-frequency, CPU can be operated in the same clock cycle to the external clock hence providing a wider operating frequency range.



OSCDBL	Internal System Clock
0	Standard (Input the oscillation clock cycle divided by 2)
1	2x-speed (Input the oscillation clock cycle)

OSCSEL1	OSCSEL0	Division factor	
		NORMAL mode	SLOW mode
0	0	1	1
0	1	4	4
1	0	16	16
1	1	64	16

Figure 2-5-1 CPU Mode Control Register (CPUM : x'03F00', R/W)

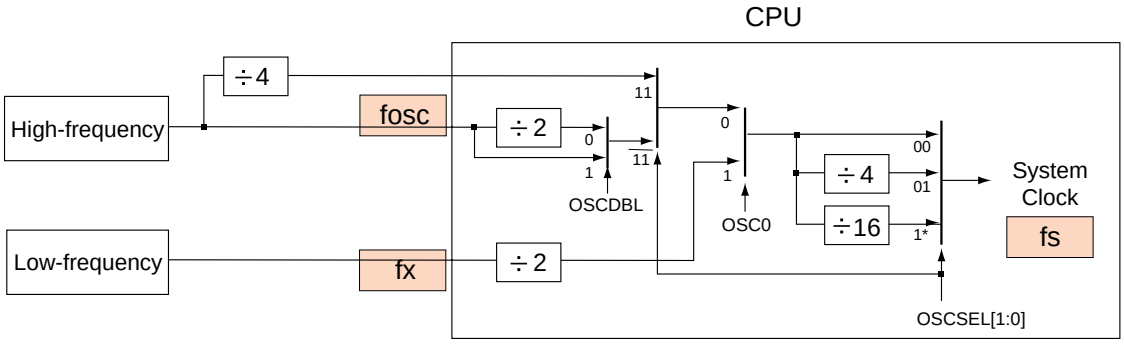


Figure 2-5-2 Clock Switching Circuit

OSCSEL1	OSCSEL0	OSCDBL	Division factor for High-frequency (OSC) Input (NORMAL mode)
0	0	0	2
0	0	1	Forbidden
0	1	0	8
0	1	1	4
1	0	0	32
1	0	1	16
1	1	0	64
1	1	1	64

Figure 2-5-3 Setting Division Rate at NORMAL mode by combination of OSCSEL and OSCDBL

OSCSEL1	OSCSEL0	Division factor for Low-frequency(XI/XO) Input (SLOW mode)
0	0	2
0	1	8
1	0	32
1	1	32

Figure 2-5-4 Setting Division Rate at SLOW mode by combination of OSCSEL

On clock switching, set each flag of OSCDBL, OSCSEL, and OSC0, individualy. Even if those flags are mapped on the same special functions register, set three times.

2-6 Reset

2-6-1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin (P27) is pulled to low.

■Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the NRST pin low for at least four clock cycles.
NRST pin should be holded "low" for more than 4 clock cycles (200 ns at a 20 MHz).

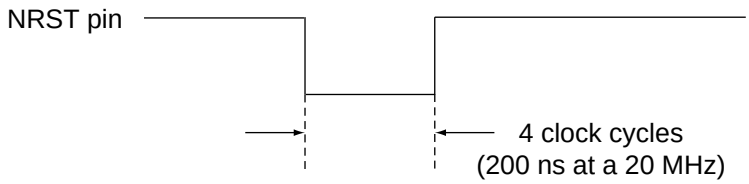


Figure 2-6-1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.

[☞ Chapter 4. 4-4-2 Registers]

This LSI's starting mode is NORMAL mode in which high oscillation is the base clock.

If the low power voltage detection circuit is connected to NRST pin, design the circuit to supply enough low level time pulse at sudden disconnect. Also beware of noise as reset could be generated even with the low level time pulse of less than 4 OSC clock cycle.

■Sequence at Reset

(1) When reset pin comes to high level from low level, system closk starts count operation by the internal 10-bit counter (watchdog timer dual function). The period from starting its count from its overflow is called oscillation stabilization wait time.

(2) During reset, internal register and special function register are initiated.

(3) After oscillation stabilization wait time is finished, internal reset is released and program is started from the address written on x'04000' of vector table.

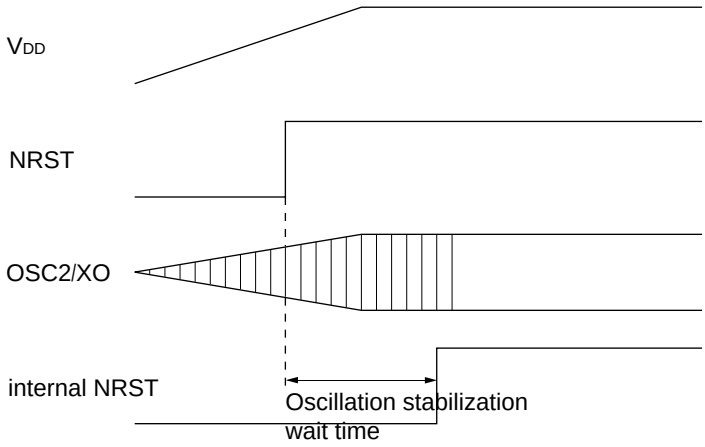


Figure 2-6-2 Reset Released Sequence

2-6-2 Oscillation Stabilization Wait time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stablization for oscillation. Oscillaion stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.

The timer that counts oscillation stabilization wait time is also used as a watchdog timer. That is used as a runaway detective timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (x'0000') when system clock (fs) is as clock source. After oscillation stabilization wait time is finished, it continues counting as a watchdog timer. [☞ Chapter 9 Watchdog timer]

■Block Diagram of Oscillation Stabilization Wait Time Function (watchdog timer)

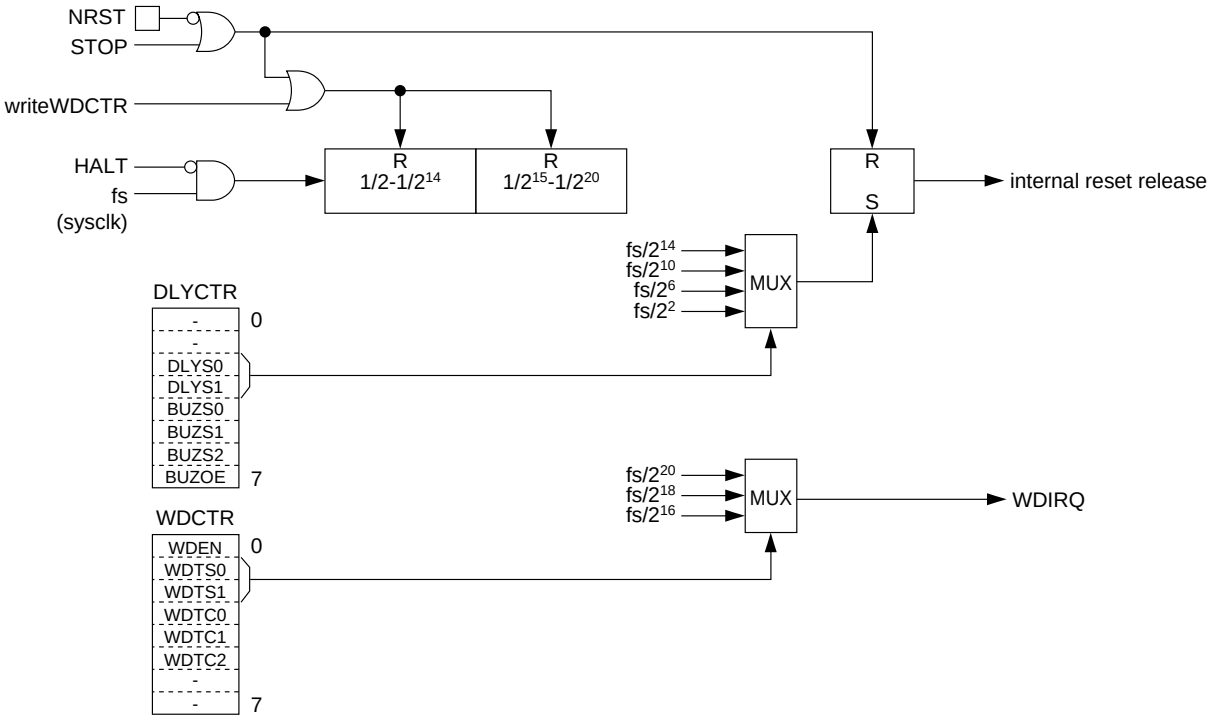
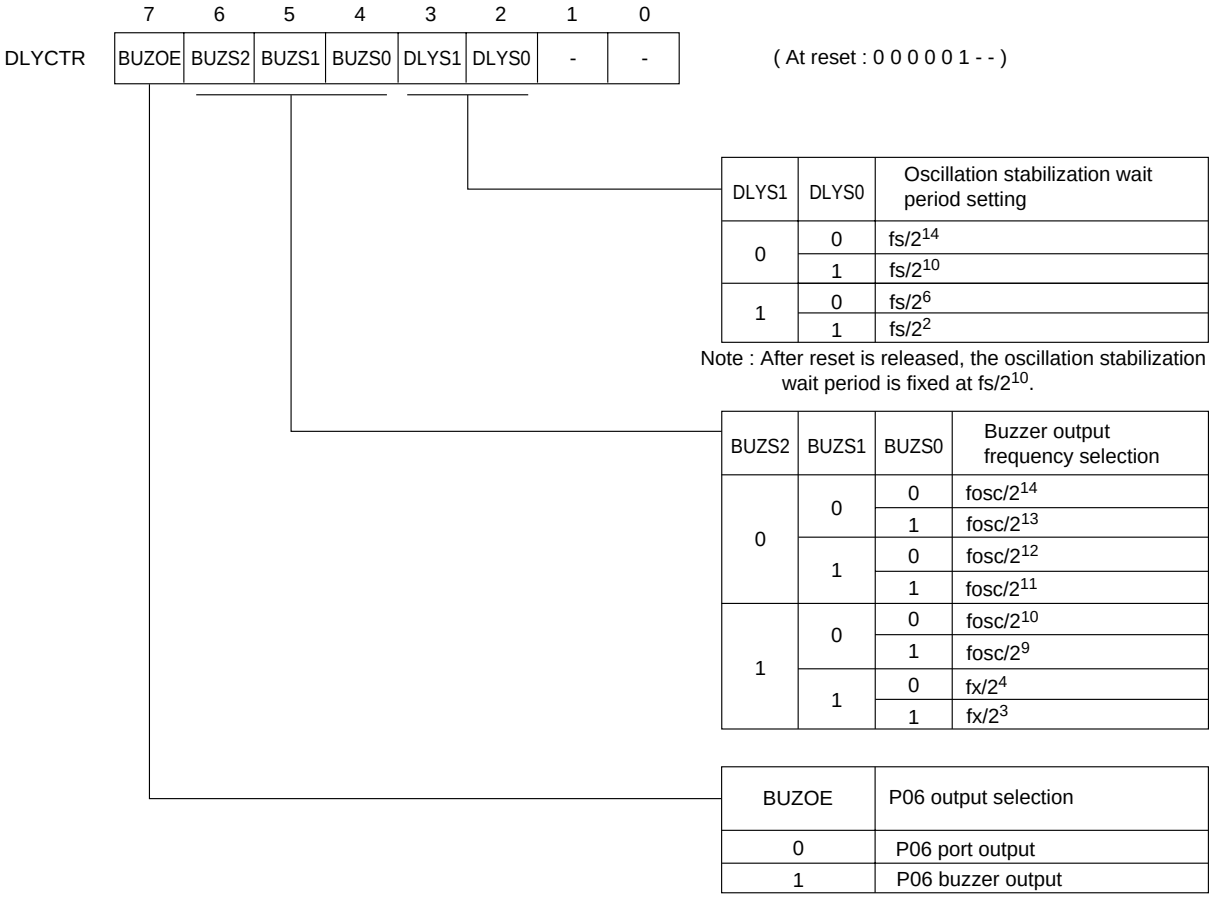


Figure 2-6-3 Block Diagram of Osillation Stabilization Wait Time Function (watchdog timer)

■Oscillation Stabilization Wait Time Control Register



DLYS1	DLYS0	Oscillation stabilization wait period setting
0	0	$fs/2^{14}$
	1	$fs/2^{10}$
1	0	$fs/2^{6}$
	1	$fs/2^{2}$

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{10}$.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	P06 port output
1	P06 buzzer output

Figure 2-6-4 Osillation stabilization wait time control register (DLYCTR : x'03F03', R/W)

■Control the Osillation Stabilization Wait Time

At recovering from STOP mode, the bit 3-2 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 2^{14}, 2^{10}, 2^{6}, 2^{2} x system clock. The DLYCTR register is also used for controlling of buzzer functions.

[☞ Chapter 10 Buzzer]

At releasing from reset, the oscillation stabilization wait time is fixed to "2^{10} x system clock". System clock is controlled through the CPU mode control register (CPUM).

Table 2-6-1 Oscillation Stabilization Wait Tim

DLYS1	DLYS0	Oscillation stabilization wait time
0	0	2^{14} x Systemclock
0	1	2^{10}x Systemclock
1	0	2^{6} x Systemclock
1	1	2^{2} x Systemclock

Chapter 3 Interrupts

3

3-1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table : reset, non-maskable interrupts (NMI), 9 maskable peripheral interrupts, and 14 internal interrupts.

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. And an interrupts handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Max.12 machine cycles before execution, and max 11 machine cycles after execution.

Each interrupt has a interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1-0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupt enable flag is set in maskable interrupt. Interrupt enable flag of maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is "1".

Maskable interrupts have had vector numbers by hardware, but their priority can be changed by setting interrupts level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1-0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3-1-1 Functions

Table 3-1-1 Interrupt Functions

Interrupt type	Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number	0	1	2 to 30
Table address	x'04000'	x'04004'	x'04008' to x'04078'
'Starting address	Address specified by vector table		
Interrupt level	-	-	Can be set to levels 0 to 2 by software
Interrupt factor	External NRST pin input	Errors detection, PI interrupt	External pin input Internal peripheral function
Generated operation	Direct input to CPU core	Input to CPU core from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxLVn) of maskable interrupt control register (xxxICR) to CPU core.
Accept operation	Always accepts	Always accepts	Accepted only by the interrupt control of the register (xxxICR) and the interrupt mask level in PSW.
Machine cycles till acceptance	12	12	12
PSW status after acceptance	All flags are cleared to "0".	The interrupt mask level flag in PSW is cleared to "00".	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority).

3-1-2 Block Diagram

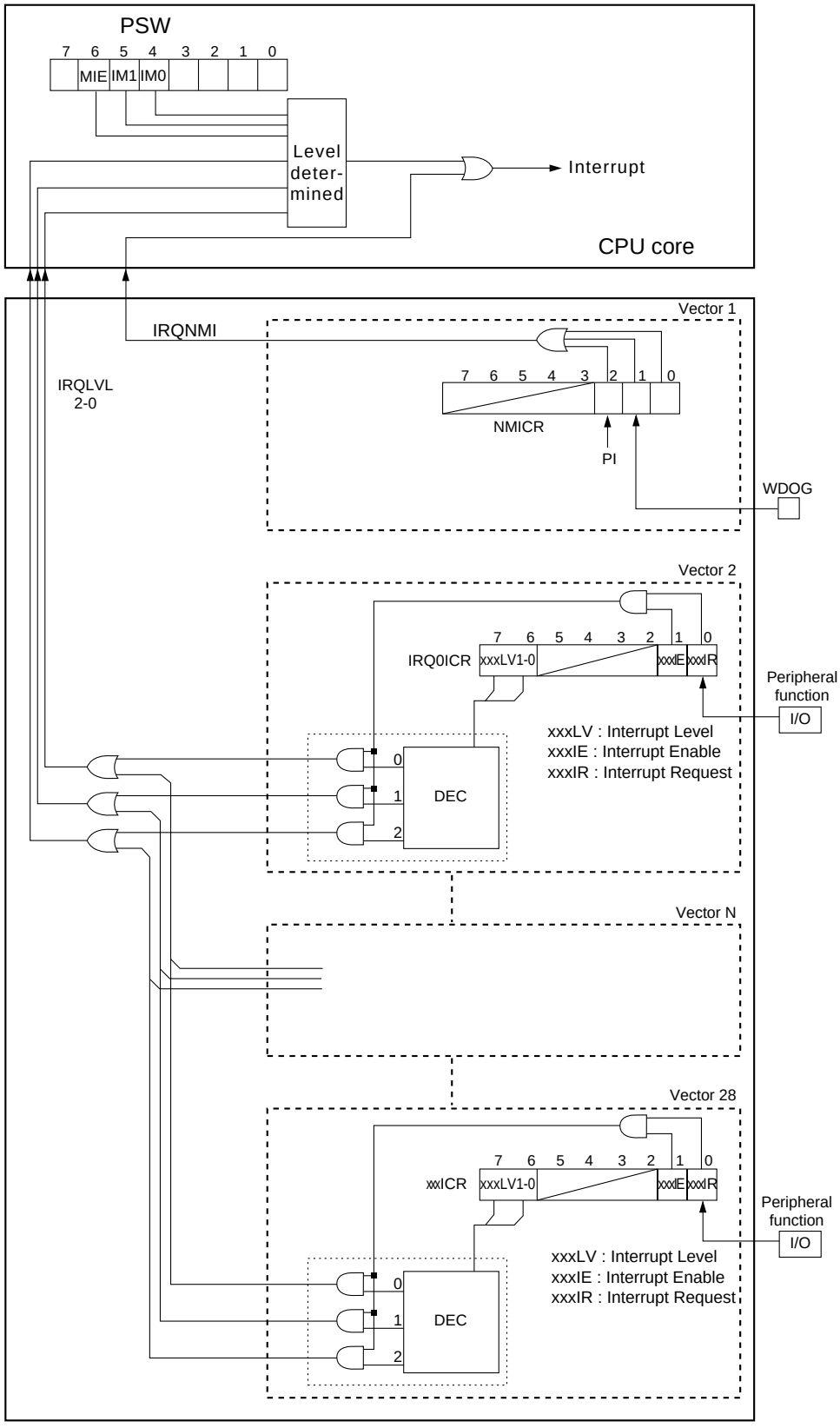


Figure 3-1-1 Interrupt Block Diagram

3-1-3 Operation

■Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. The program counter (PC) and processor status word (PSW) and hard addressing data (HA) are saved onto the stack, and program is branched to the address specified by the corresponding interrupt vector.

An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

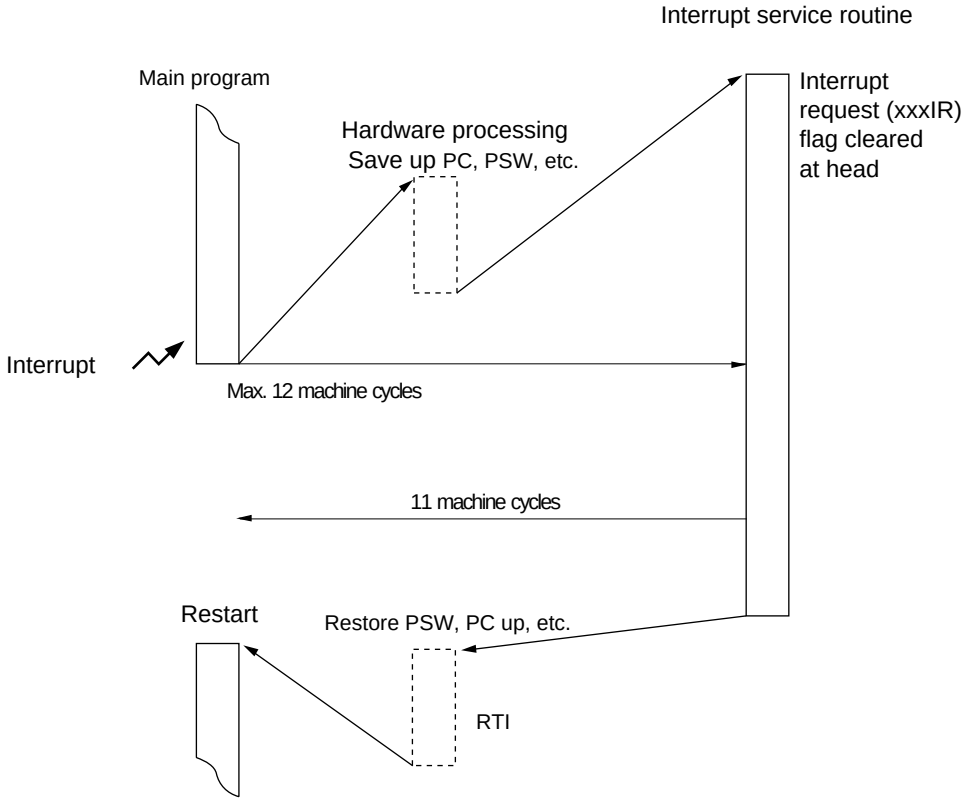


Figure 3-1-2 Interrupt Processing Sequence (maskable interrupts)

■Interrupt Group and Vector Addresses

Here is the list of interrupt vector address and interrupt group.

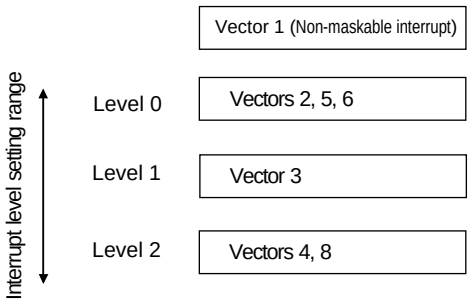
Table 3-1-2 Interrupt Vector Address and Interrupt Group

Vector Number	Vector Address	Interrupt group (Interrupt source)		Control Register (address)	
0	x'04000'	Reset	-	-	-
1	x'04004'	Non-maskable interrupt	NMI	NMICR	x'03FE1'
2	x'04008'	External interrupt 0	IRQ0	IRQ0ICR	x'03FE2'
3	x'0400C'	External interrupt 1	IRQ1	IRQ1ICR	x'03FE3'
4	x'04010'	External interrupt 2	IRQ2	IRQ2ICR	x'03FE4'
5	x'04014'	Reserved	-	-	-
6	x'04018'	External interrupt 4	IRQ4	IRQ4ICR	x'03FE6'
7	x'0401C'	Reserved	-	-	-
8	x'04020'	Reserved	-	-	-
9	x'04024'	Timer 0 interrupt	TM0IRQ	TM0ICR	x'03FE9'
10	x'04028'	Timer 1 interrupt	TM1IRQ	TM1ICR	x'03FEA'
11	x'0402C'	Timer 2 interrupt	TM2IRQ	TM2ICR	x'03FEB'
12	x'04030'	Timer 3 interrupt	TM3IRQ	TM3ICR	x'03FEC'
13	x'04034'	Reserved	-	-	-
14	x'04038'	Reserved	-	-	-
15	x'0403C'	Timer 6 interrupt	TM6IRQ	TM6ICR	x'03FEF'
16	x'04040'	Time base interrupt	TBIRQ	TBICR	x'03FF0'
17	x'04044'	Timer 7 interrupt	TM7IRQ	TM7ICR	x'03FF1'
18	x'04048'	Timer 7 compare2-match	T7OC2IRQ	T7OC2ICR	x'03FF2'
19	x'0404C'	Timer 8 interrupt	TM8IRQ	TM8ICR	x'03FF3'
20	x'04050'	Reserved	-	-	-
21	x'04054'	Serial 0 interrupt 1	SC0RIRQ	SC0RICR	x'03FF5'
22	x'04058'	Serial 0 interrupt 2	SC0TIRQ	SC0TICR	x'03FF6'
23	x'0405C'	Reserved	-	-	-
24	x'04060'	Reserved	-	-	-
25	x'04064'	Reserved	-	-	-
26	x'04068'	A/D conversion interrupt	ADIRQ	ADICR	x'03FFA'
27	x'0406C'	Reserved	-	-	-
28	x'04070'	Reserved	-	-	-
29	x'04074'	Reserved	-	-	-
30	x'04078'	Reserved	-	-	-

Write an address to which the RTI instruction is written to memory space of the vector addresss of reserved or unused interrupt.

■Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupts simultaneously, vector 3 will be accepted.



Priority	Interrupt vector No.
1	Vector 1
2	Vector 2
3	Vector 5
4	Vector 6
5	Vector 3
6	Vector 4
7	Vector 8

Figure 3-1-3 Interrupt Priority Outline

■Determination of Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

(1) The interrupt request flag (xxxIR) in the corresponding external interrupt control register(IRQnICR) and internal interrupt control register (xxxICR) are set to '1'.

(2) An interrupt request is input to the CPU. (If the interrupt enable flag (xxxIE) of the same register is '1'.)

(3) The interrupt request signal is set for each interrupt. The interrupt level (IL) is input to the CPU.

(4) The interrupt request is accepted. (If IL has higher priority than IM and MIE is '1'.)

(5) After the interrupt is accepted, the hardware resets the interrupt request flag (xxxIR) in the interrupt control register (xxxICR) to '0'.

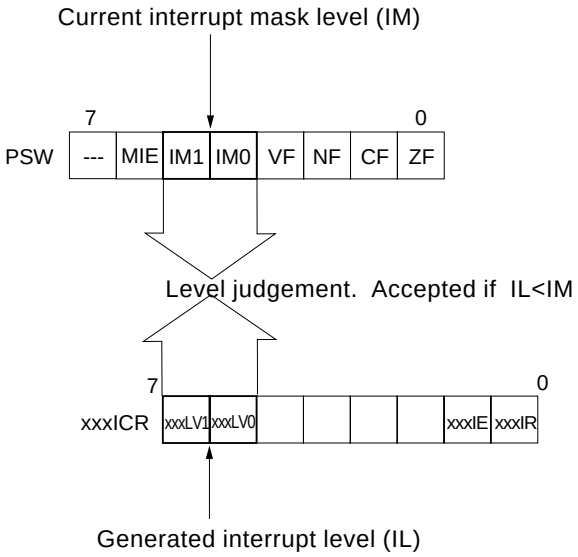


Figure 3-1-4 Determination of Interrupt Acceptance

Acceptance of an interrupt does not reset the corresponding interrupt enable flag (xxxIE) to "0".

When set as xxxLV1=1, xxxLV0=1, the set interrupt is disabled regardless of the values of xxxIE, XXXIR.

MIE='0' and interrupts are disabled when:

- MIE in the PSW is reset to '0' by a program
- Reset is detected

MIE='1' and interrupts are enabled when:

- MIE in the PSW is set to '1' by a program

The interrupt mask level (IM=IM1 - IM0) in the processor status word (PSW) changes when:

- The program alters it directly,
- A reset initializes it to 0 (00b),
- Maskable interrupt is accepted (the interrupt level becomes the interrupt mask level).
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.

The MN101C series does not reset the maskable interrupt enable (MIE) flag of the processor status word (PSW) to "0" when accepting interrupts.

Non-maskable interrupts have priority over maskable ones.

■Interrupt Acceptance Operation

When accepting an interrupt, hardware of this LSI saves the handy address register, the return address from the program counter, and the processor status word (PSW) to the stack and branches program to the interrupt handler using the starting address in the vector table.

The following is the hardware processing sequence invoked by interrupt acceptance.

1. The stack pointer (SP) is updated.
   (SP-6 → SP)
2. The contents of the handy address register (HA) are saved to the stack.
   Upper half of HA → (SP+5)
   Lower half of HA → (SP+4)
3. The contents of the program counter (PC) -i.e., the return address- are saved to the stack.
   PC bits 18, 17, and 0 → (SP+3)
   PC bits 16-9 → (SP+2)
   PC bits 8-1 → (SP+1)
4. The contents of the PSW are saved to the stack.
   PSW → (SP)
5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask (IMn) in the PSW.
   Interrupt level (xxxLVn) → IMn
6. The hardware branches program to the address in the vector table.

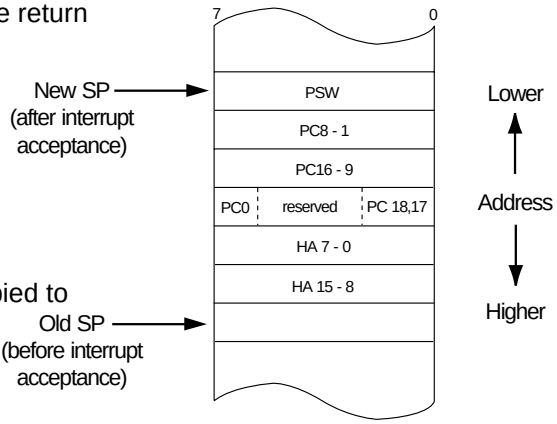


Figure 3-1-5 Stack Operation during interrupt acceptance

■Interrupt Return Operation

An interrupt handler ends by restoring the contents of any registers saved to the stack during processing by the POP instruction and other means, and the RTI instruction restores the program to the point at execution was interrupted.

The following is the processing sequence invoked by the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC) - i.e., the return address- are restored from the stack. (SP+1 to SP+3)
3. The contents of the handy address register (HA) are restored from the stack. (SP+4, SP+5)
4. The stack pointer is updated. (SP+6 → SP)
5. Execution branches program to the address in the program counter.

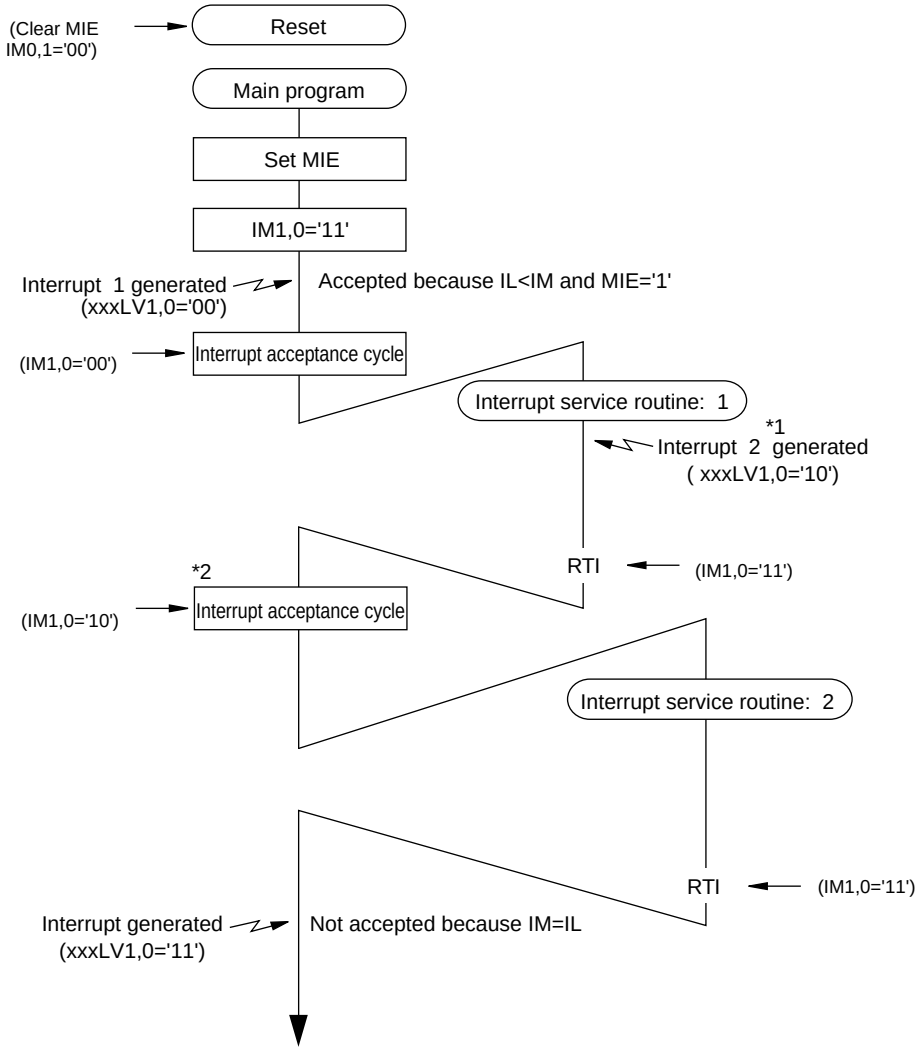
The handy address register is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.

Registers such as data register, or address register are not saved, so that PUSH instruction from program should be used to save them onto the stack, if necessary.

The address bp6 to bp2, when program counter (PC) are saved to the stack, are reserved. Do not change it by program.

■Maskable Interrupt

Figure 3-1-6 shows the processing flow when a second interrupt with a lower priority level (xxxLV1-xxxLV0='10') arrives during the processing of one with a higher priority level (xxxLV1-xxxLV0='00').



Parentheses ( ) indicate hardware processing.

*1 If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If IL ≥ IM, however, the interrupt is not accepted.

*2 The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure 3-1-6 Processing Sequence for Maskable Interrupts

■Multiplex Interrupt

When an MN101C527 series device accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

1. To disable interrupt nesting
   - Reset the MIE bit in the PSW to "0".
   - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
   - Lower the priority level of the interrupt mask (IM) in the PSW.

Multiplex interrupts are only enabled for interrupts with levels higher than the PSW interrupt mask level (IM).

It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but be careful of stack overflow.

Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag.

Figure 3-1-7 shows the processing flow for multiple interrupts (interrupt 1: xxxLV1-xxxLV0='10', and interrupt 2: xxxLV1-xxxLV0='00').

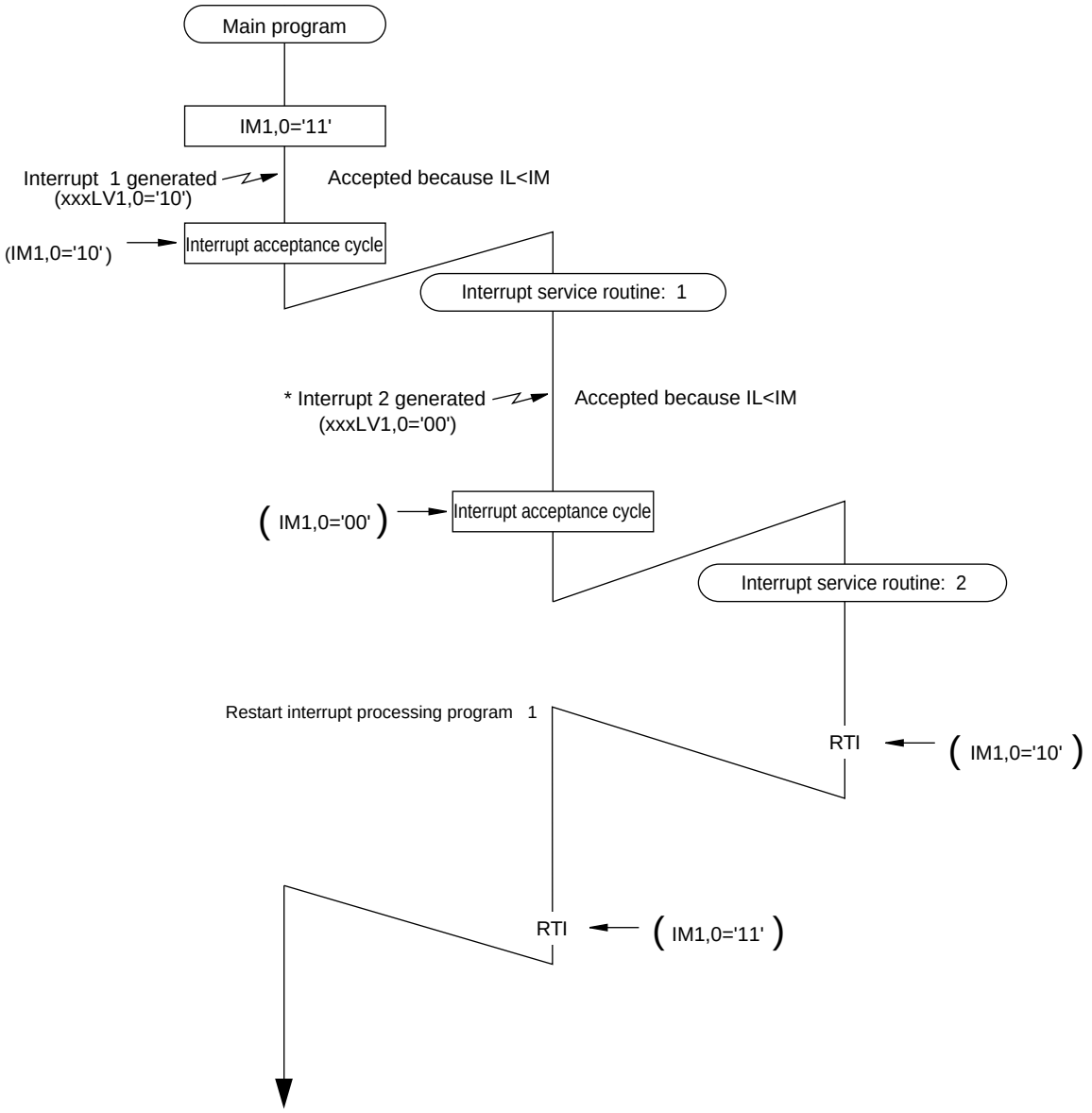


Figure 3-1-7 Processing Sequence with Multiple Interrupts Enabled

3-1-4 Interrupt Flag Setup

■ Interrupt request flag (IR) setup by the software

The interrupt request flag is operated by the hardware. That is set to "1" when any interrupt factor is generated, and cleared to "0" when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to "1".

■ Interrupt flag setup procedure

A setup procedure of the interrupt request flag set by the hardware and the software shows as follows ;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6 : MIE = 0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Select the interrupt factor.	(2) Select the interrupt factor such as interrupt edge selection, or timer interrupt cycle change.
(3) Enable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 1	(3) Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4) Rewrite the interrupt request flag. xxxICR bp0 : xxxIR	(4) Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR).
(5) Disable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 0	(5) Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6) Set the interrupt level. xxxICR bp7-6 : xxxLV1-0 PSW bp5-4 : IM1-0	(6) Set the interrupt level by the xxxLV1-0 flag of the interrupt control register (xxxICR). Set the IM1-0 flag of PSW when the interrupt acceptance level of CPU should be changed.
(7) Enable the interrupt. xxxICR bp1 : xxxIE = 1	(7) Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8) Enable all maskable interrupts. PSW bp6 : MIE = 1	(8) Set the MIE flag of PSW to enable maskable interrupts.

3-2 Control Registers

3-2-1 Registers List

Table 3-2-1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	x'03FE1'	R/W	Non-maskable interrupt control register	III - 16
IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III - 18
IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III - 19
IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	III - 20
IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	III - 21
TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register (Timer 0 compare-match)	III - 22
TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register (Timer 1 compare-match)	III - 23
TM2ICR	x'03FEB'	R/W	Timer 2 interrupt control register (Timer 2 compare-match)	III - 24
TM3ICR	x'03FEC'	R/W	Timer 3 interrupt control register (Timer 3 compare-match)	III - 25
TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register (Timer 6 compare-match)	III - 26
TBICR	x'03FF0'	R/W	Time base interrupt control register (Time base period)	III - 27
TM7ICR	x'03FF1'	R/W	Timer 7 interrupt control register (Timer 7 compare-match)	III - 28
T7OC2ICR	x'03FF2'	R/W	Timer 7 compare register 2-match interrupt control register	III - 29
TM8ICR	x'03FF3'	R/W	Timer 8 interrupt control register (Timer 8 compare-match)	III - 30
SC0RICR	x'03FF5'	R/W	Serial 0 nterrupt control register 1	III - 31
SC0TICR	x'03FF6'	R/W	Serial 0 interrupt control register 2	III - 32
ADICR	x'03FFA'	R/W	A/D conversion interrupt control register (A/D conversion complete)	III - 33

Writing to the interrupt control register should be done after that all maskable interrupts are set to be disable by the MIE flag of the PSW register.

If the interrupt level flag (xxxLVn) is set to "level 3", its vector is disabled, regardless of interrupt enable flag and interrupt request flag.

3-2-2 Interrupt Control Registers

The interrupt control registers include the non-maskable interrupt control register (NMICR), the external interrupt control register and the internal interrupt control registers (xxxICR).

■Non-Maskable Interrupt Control Register (NMICR address: x'3FE1')

The non-maskable interrupt control register (NMICR) is stored the non maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches program to the address stored at location x'4004' in the interrupt vector table. The watchdog timer overflow interrupt request flag (WDIR) is set to "1" when the watchdog timer overflows. The program interrupt request flag (PIR) is set to "1" when the undefined instruction is executed.
Setting PIR or WDIR flag to be "1" enable non-maskable interrupt request to be set compulsory.

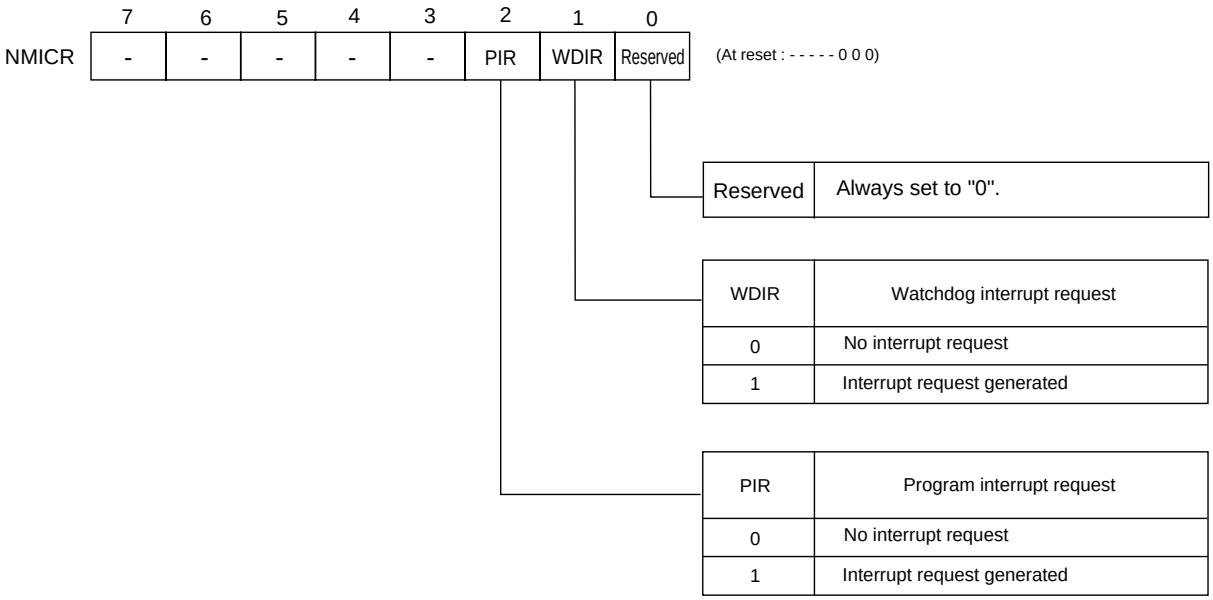


Figure 3-2-1 Non-Maskable Interrupt Control Register (NMICR:x'03FE1', R/W)

This LSI generates non-maskable interrupt and sets the program interrupt request flag (PIR) at the same time before undefined instruction is exected.
If setting of the PIR flag is detected in the non-maskable interrupt service routine, use the software reset which outputs "0" to the reset pin (P27).

Once a non-maskable interrupt is generated and the value of the WDIR changes to "1", the value does not return to "0" unless it is cleared by program.

Faulty interrupt that does not occur under normal conditions could be occurred with certain combinations of instruction codes. In programming, please follow the instructions shown below.

Faulty interrupt could be occurred independently of issue of a branch instruction if the instruction code right after the one of the following 19 branch instructions in a program is "2FD", "3DA", or "3DB", which is identical to relevant unspecified instructions.
The relevant 19 branch instructions are ; BEQ, BNE, BGE, BCC, BCS, BLT, BLE, BGT, BHI, BLS, BNC, BNS, BVC, BVS, BRA, CBEQ, CBNE, TBZ, TBNZ.
This faulty interrupt halts the ICE operation with "Illegal instruction break", and also causes a non-maskable interrupt on Mask ROM, EEPROM and Flash ROM products.

The cause is a design error in the hardware circuits.

Example :
When a branch instruction is placed right in front of a ROM data and if the instruction right behind a branch instruction (code "89") is "2FD", above faulty interrupt is occurred.

Addr	Code	Nmonic	
04100	AA	mov	(A0),D0
04100	89D7	bra	+7D
04102	2F	dc	F2
04103	D0	dc	0D

The instruction code (ROM data) right behind the branch instruction (code "89") is "2FD"

We are providing a software diagnostic tool.
Please refer to the documents attached to the diagnotic tool for how to use it
If above problem is identified with the diagnostic tool, insert a "nop" instruction to avoid the above relevant condition to be fulfilled.

Example :

Addr	Code	Nmonic		
04100	AA	mov	(A0),D0	
04100	89F7	bra	+7F	If above problem is identified with the diagnostic
04102	00	nop		tool, insert a "nop" instruction to avoid the
04103	2F	dc	F2	above relevant condition to be fulfilled.
04104	D0	dc	0D	

The diagnostic tool can be downloaded from our Web site of TECHNICAL REPORT.

■External Interrupt 0 Control Register (IRQ0ICR)

The external interrupt 0 control register (IRQ0ICR) controls interrupt level of the external interrupt 0, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

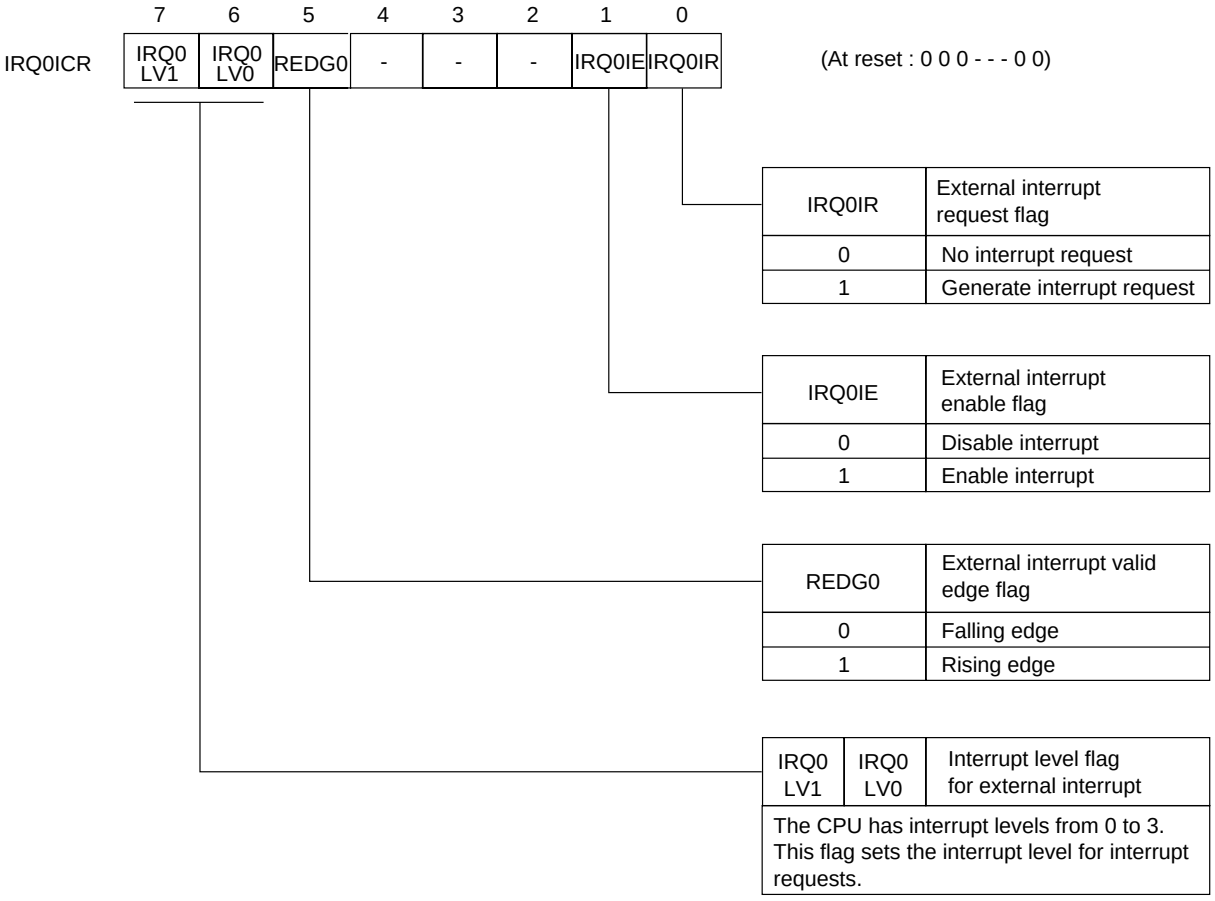


Figure 3-2-2 External Interrupt 0 Control Register (IRQ0ICR : x'03FE2', R/W)

■External Interrupt 1 Control Register (IRQ1ICR)

The external interrupt 1 control register (IRQ1ICR) controls interrupt level of external interrupt 1, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

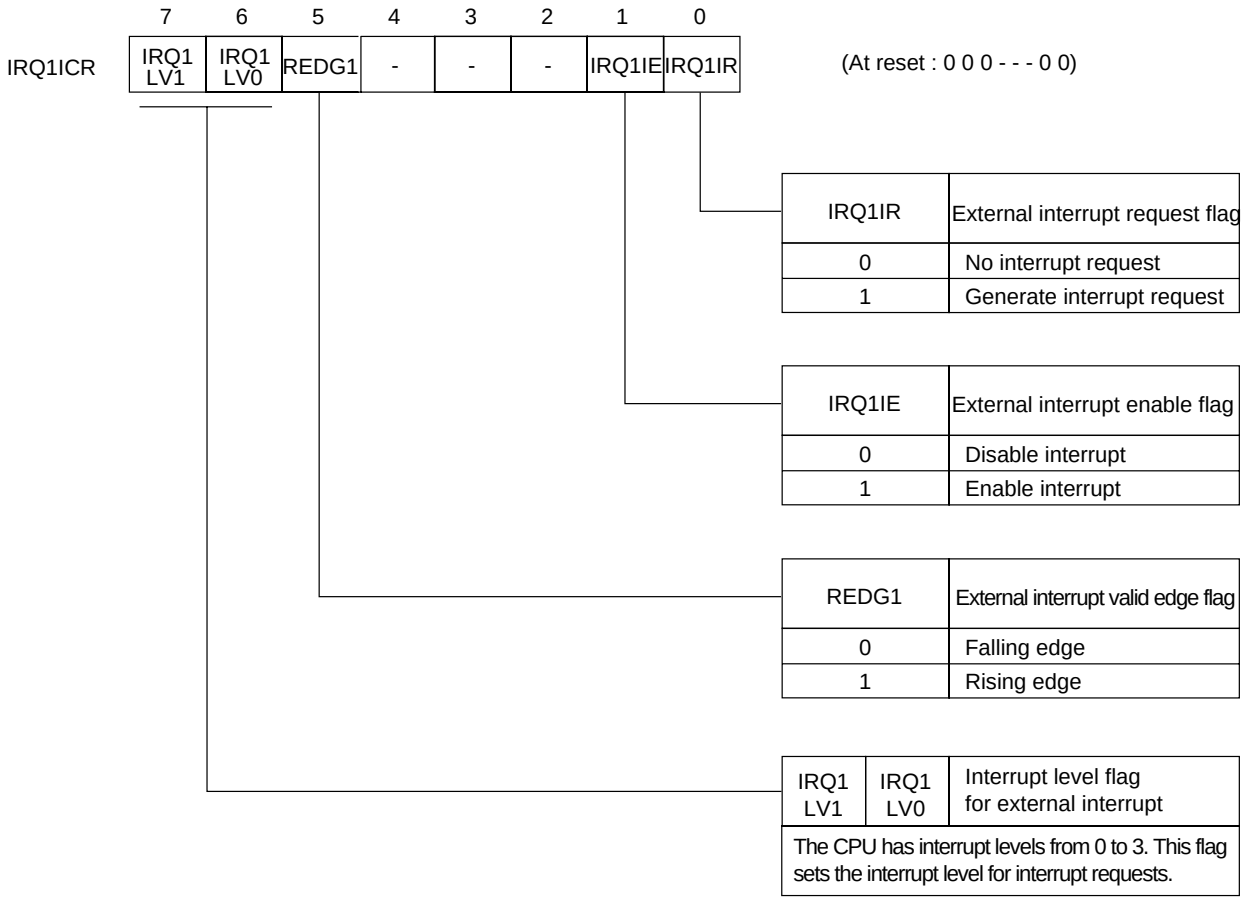


Figure 3-2-3 External Interrupt 1 Control Register (IRQ1ICR : x'03FE3', R/W)

■External Interrupt 2 Control Register (IRQ2ICR)

The external interrupt 2 control register (IRQ2ICR) controls interrupt level of external interrupt 2, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

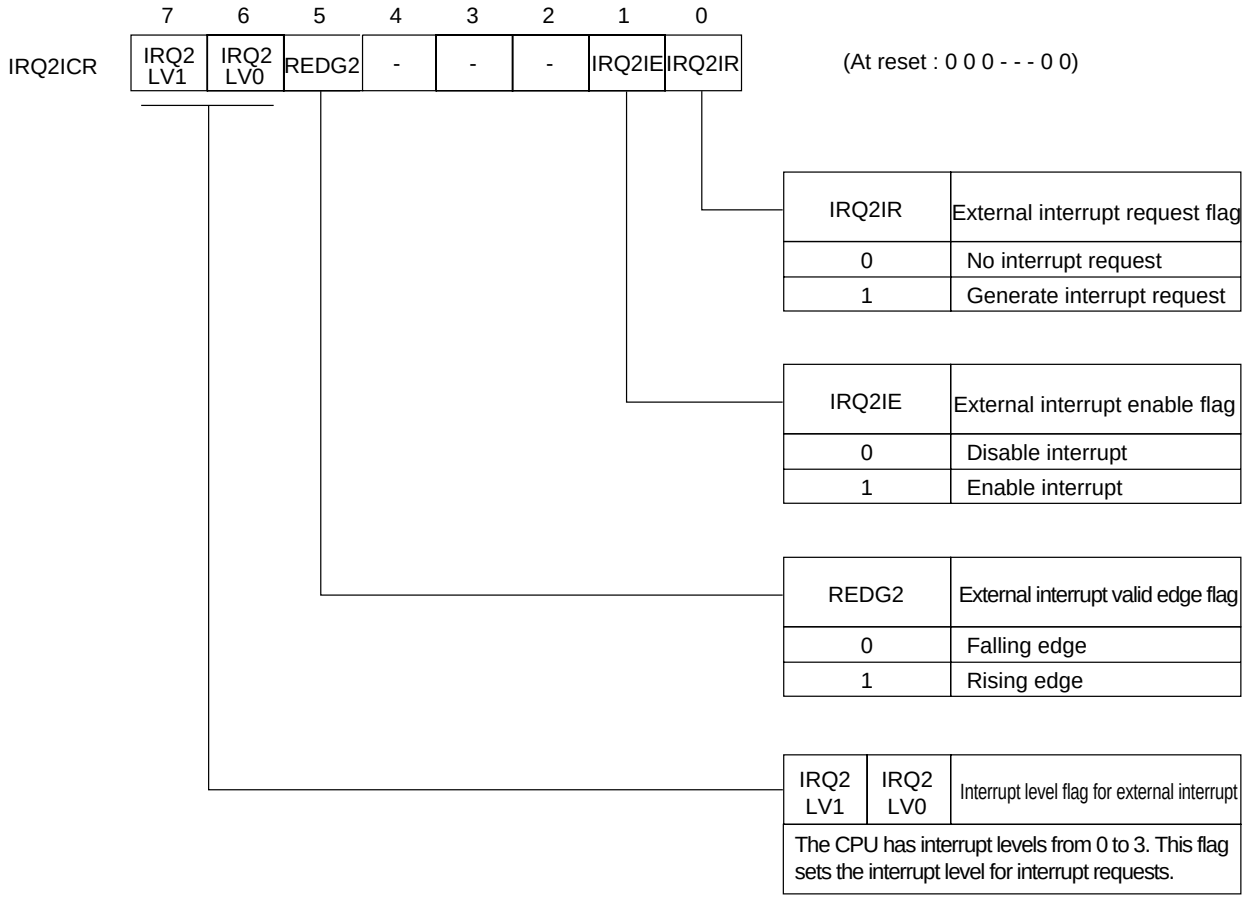


Figure 3-2-4 External Interrupt 2 Control Register (IRQ2ICR : x'03FE4', R/W)

■External Interrupt 4 Control Register (IRQ4ICR)

The external interrupt 4 control register (IRQ4ICR) controls interrupt level of external interrupt 4, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

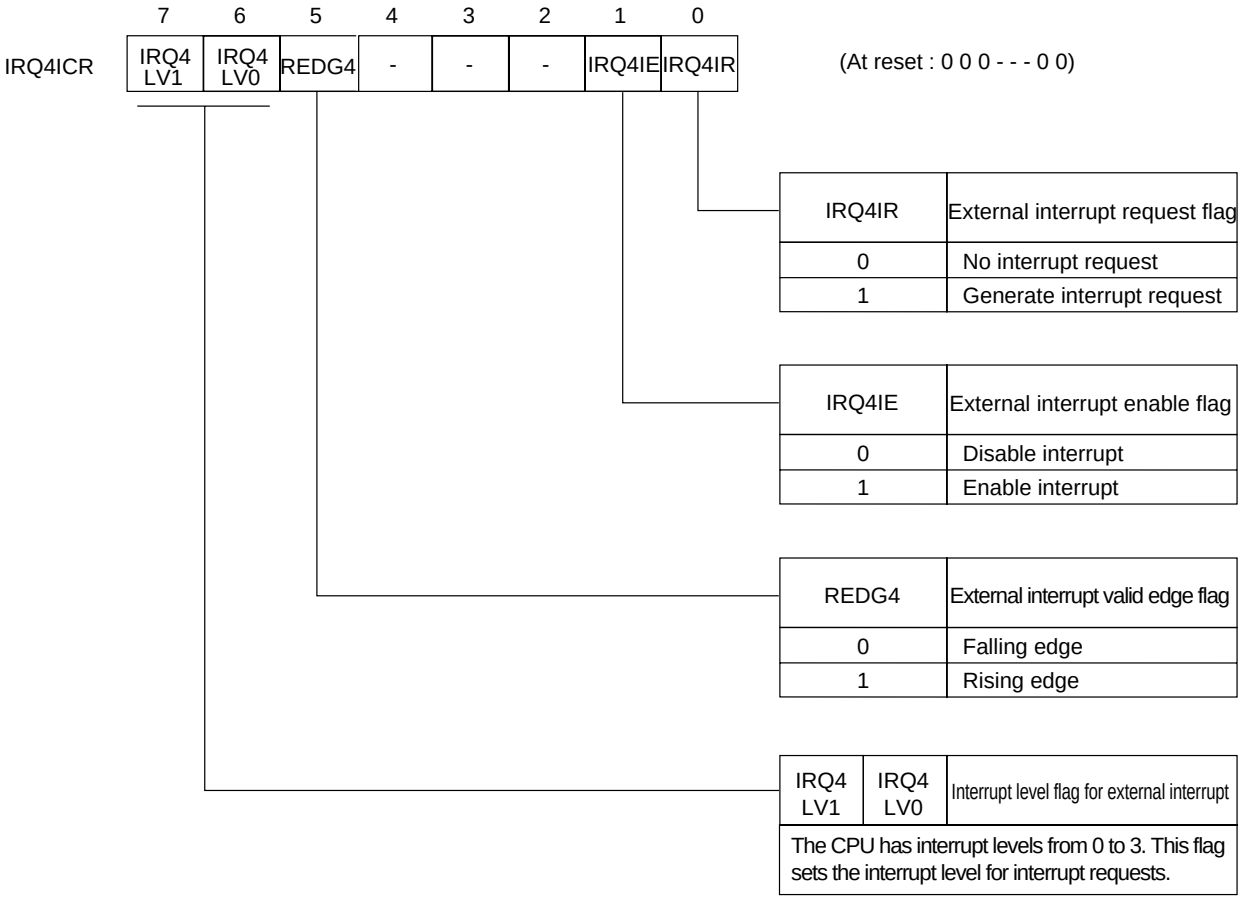


Figure 3-2-5 External Interrupt 4 Control Register (IRQ4ICR : x'03FE6', R/W)

■Timer 0 Interrupt Control Register (TM0ICR)

The timer 0 interrupt control register (TM0ICR) controls interrupt level of timer 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

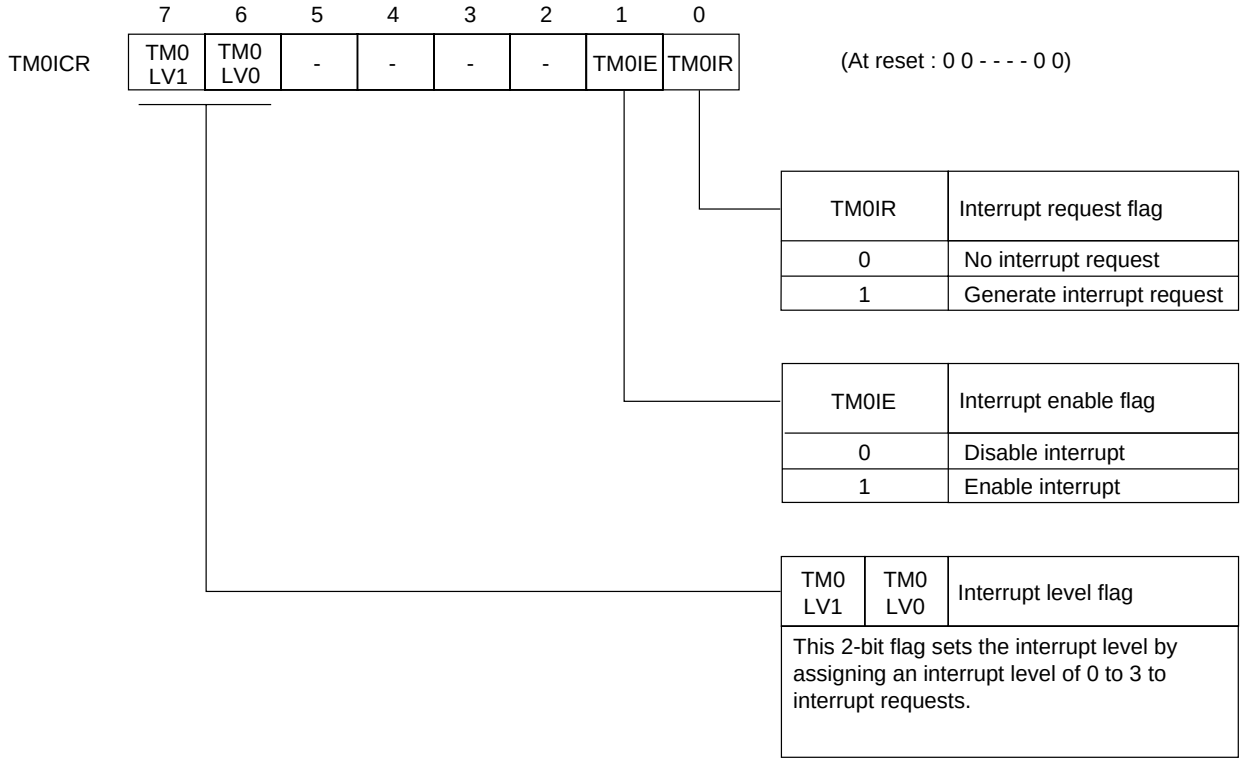


Figure 3-2-6 Timer 0 Interrupt Control Register (TM0ICR : x'03FE9', R/W)

■Timer 1 Interrupt Control Register (TM1ICR)

The timer 1 interrupt control register (TM1ICR) controls interrupt level of timer 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

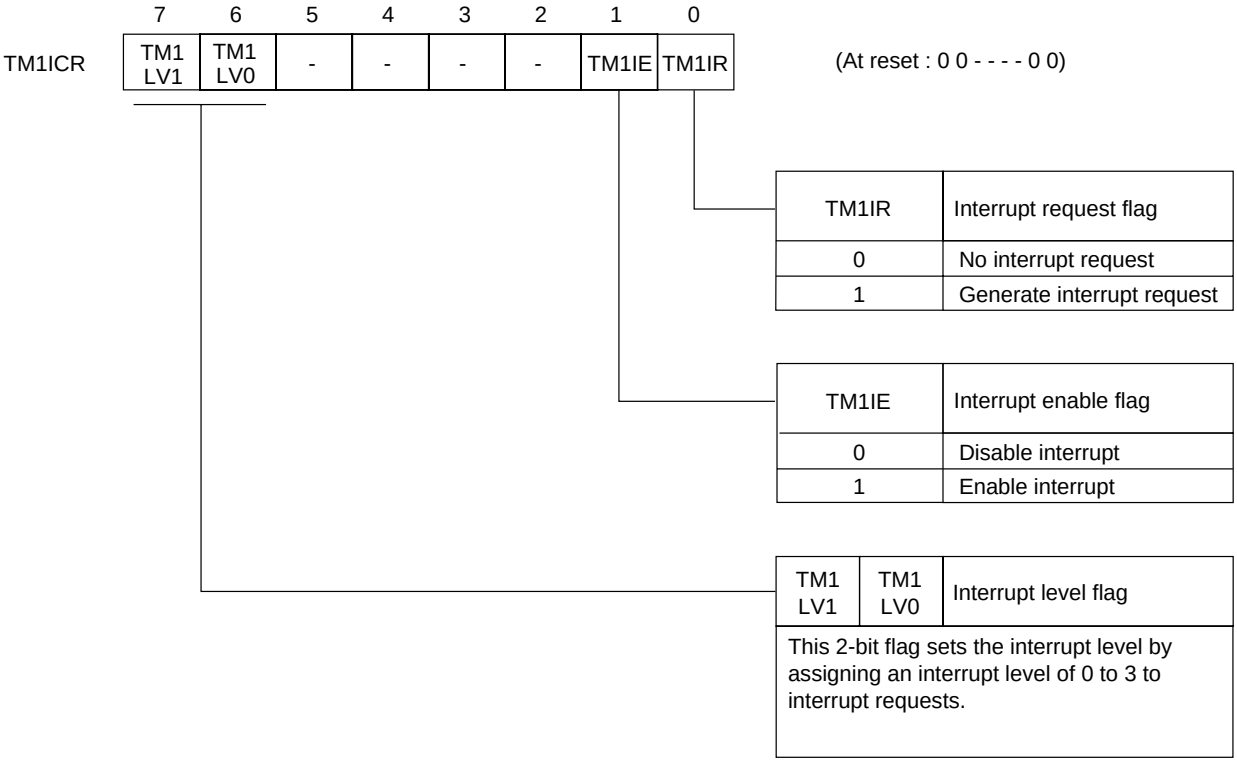


Figure 3-2-7 Timer 1 Interrupt Control Register (TM1ICR : x'03FEA', R/W)

■Timer 2 Interrupt Control Register (TM2ICR)

The timer 2 interrupt control register (TM2ICR) controls interrupt level of timer 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

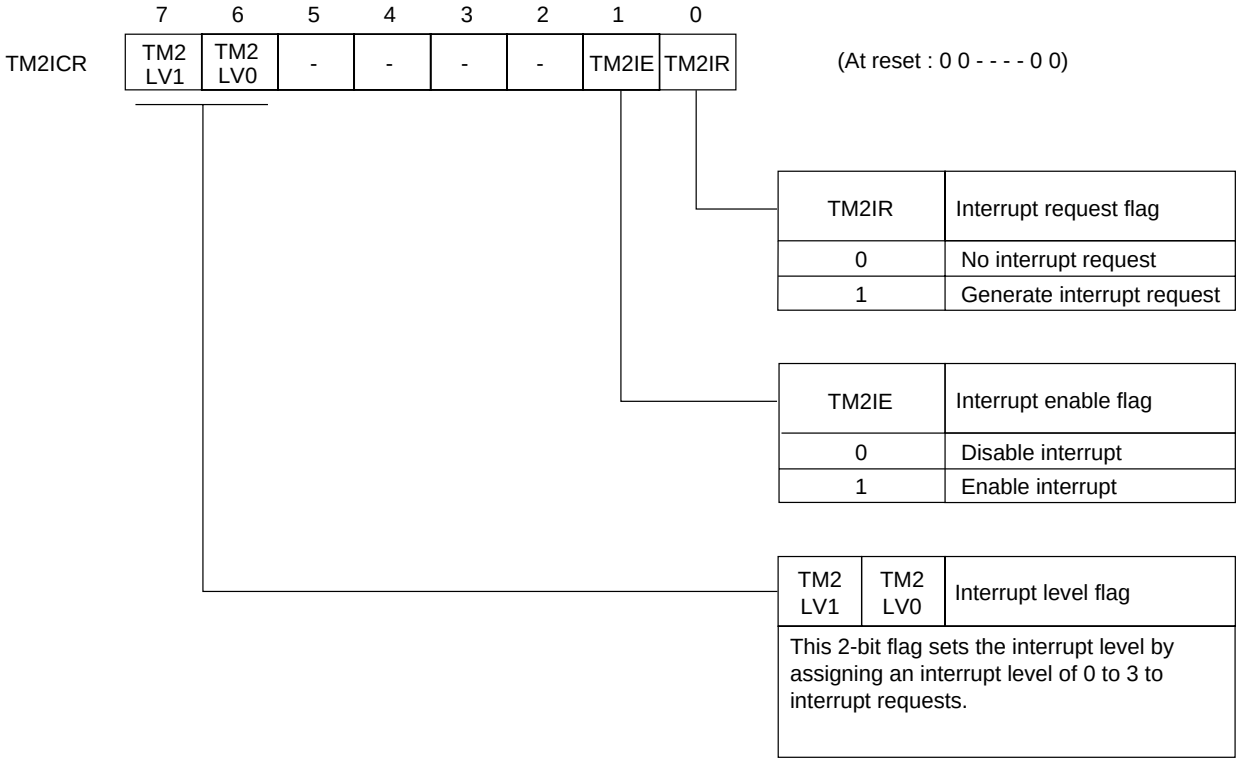


Figure 3-2-8 Timer 2 Interrupt Control Register (TM2ICR : x'03FEB', R/W)

■Timer 3 Interrupt Control Register (TM3ICR)

The timer 3 interrupt control register (TM3ICR) controls interrupt level of timer 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

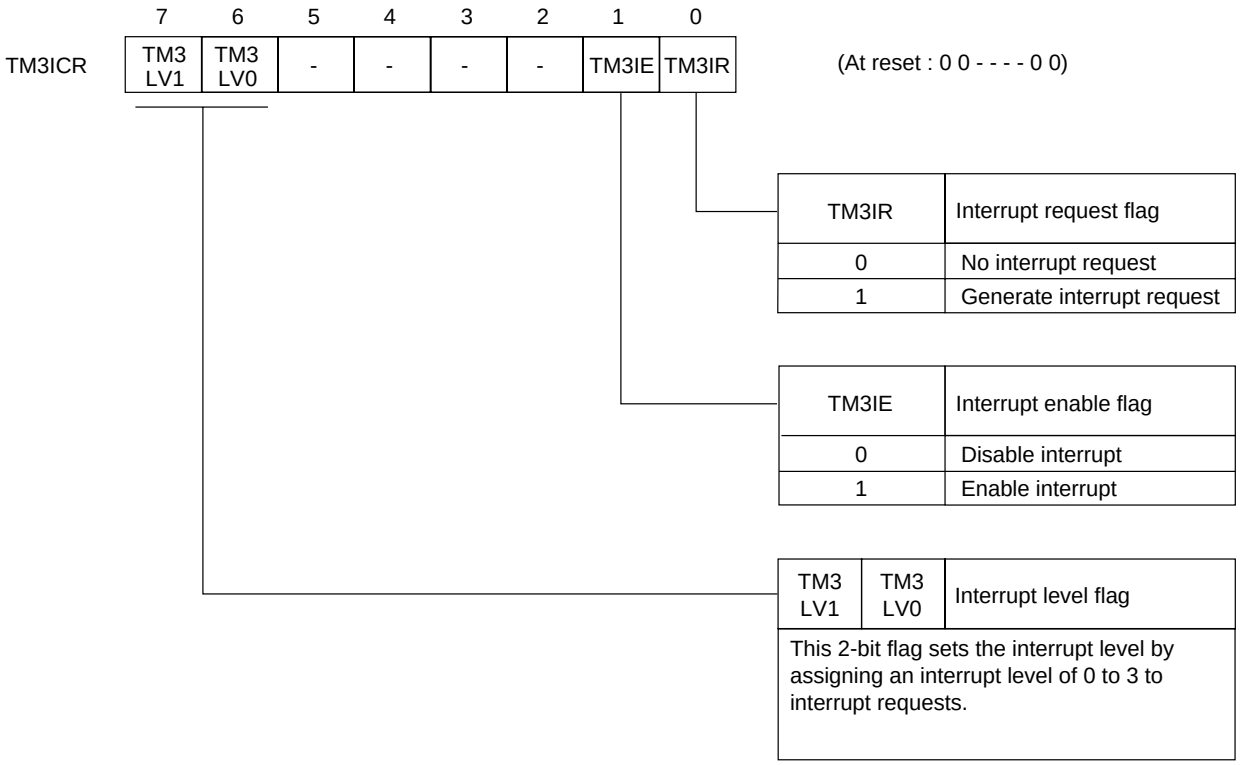


Figure 3-2-9 Timer 3 Interrupt Control Register (TM3ICR : x'03FEC', R/W)

■Timer 6 Interrupt Control Register (TM6ICR)

The timer 6 interrupt control register (TM6ICR) controls interrupt level of timer 6 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

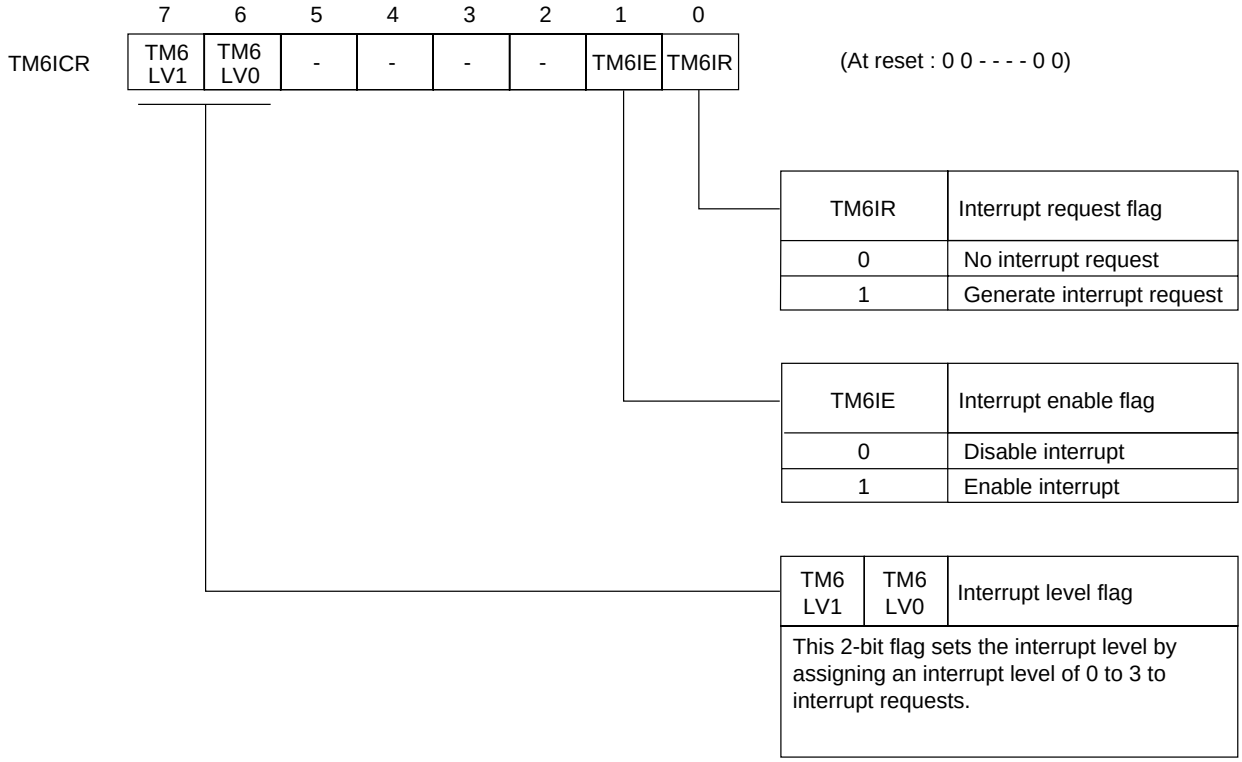


Figure 3-2-10 Timer 6 Interrupt Control Register (TM6ICR : x'03FEF', R/W)

■Time Base Interrupt Control Register (TBICR)

The time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

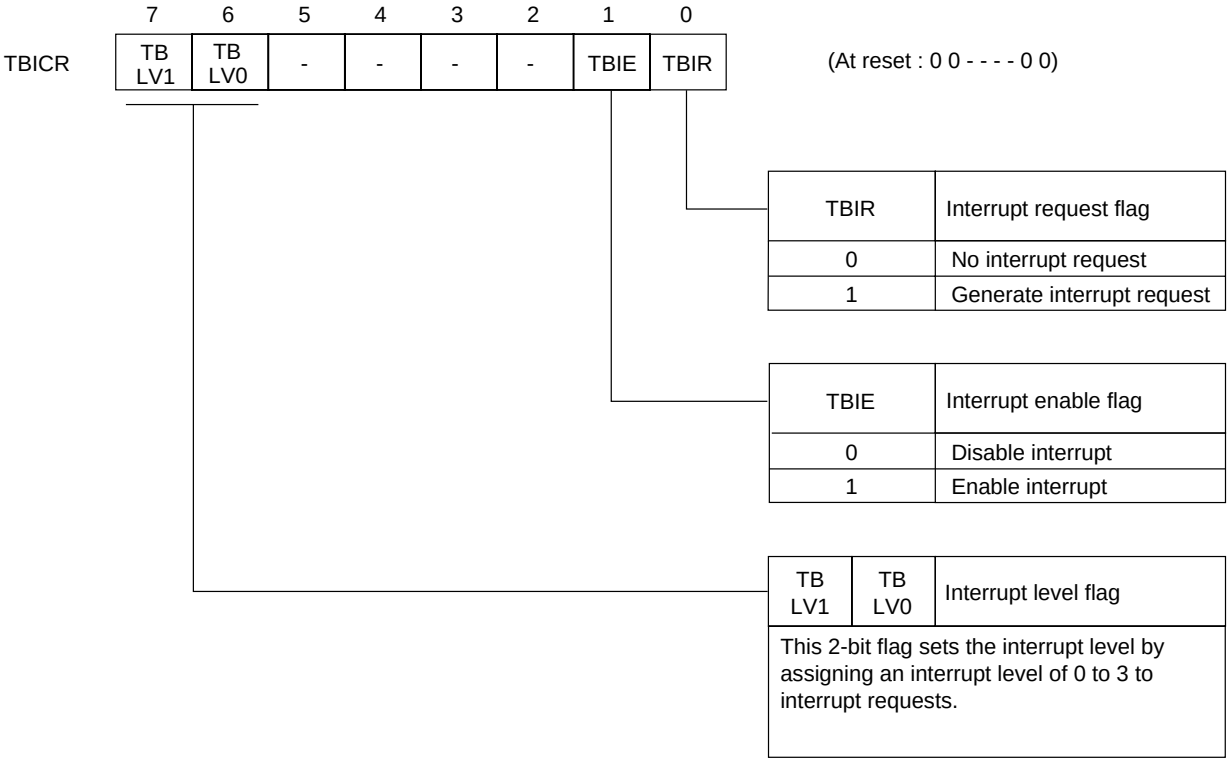


Figure 3-2-11 Time Base Interrupt Control Register (TBICR : x'03FF0', R/W)

■Timer 7 Interrupt Control Register (TM7ICR)

The timer 7 interrupt control register (TM7ICR) controls interrupt level of timer 7 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

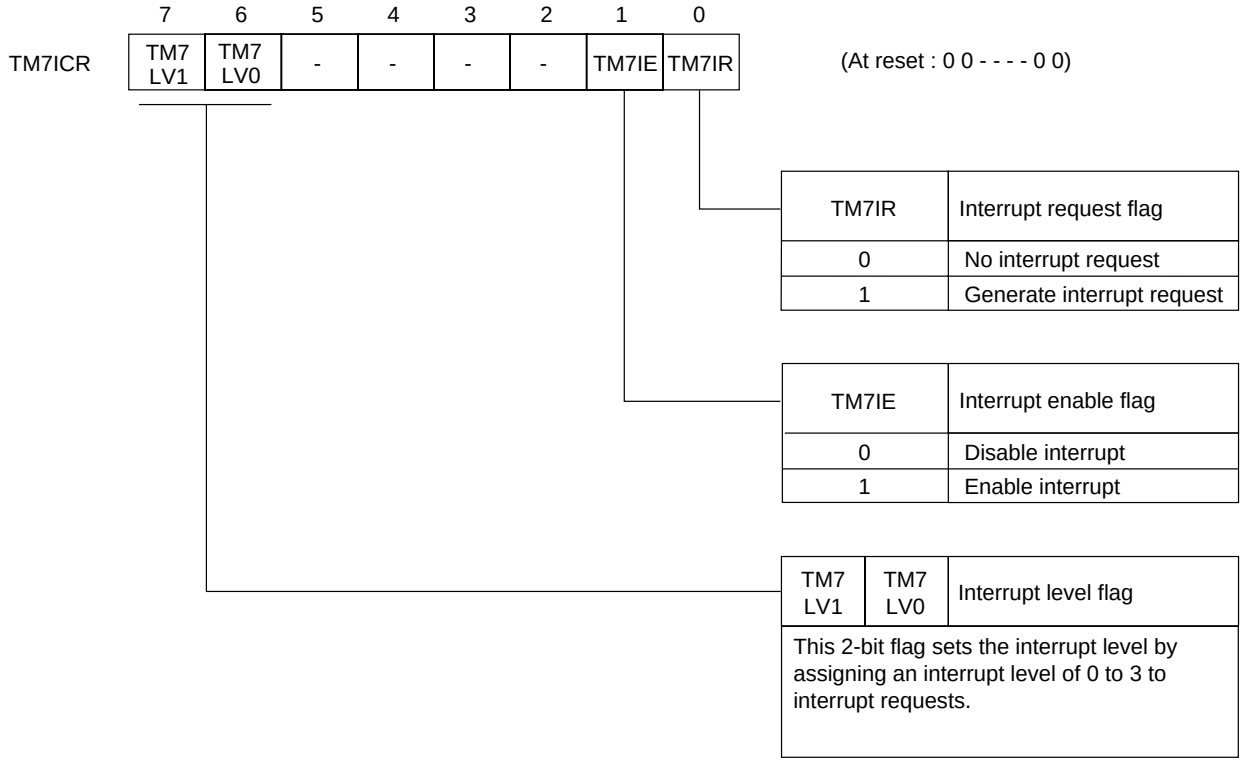


Figure 3-2-12 Timer 7 Interrupt Control Register (TM7ICR : x'03FF1', R/W)

■Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR)

The timer 7 compare register 2-match interrupt control register (T7OC2ICR) controls interrupt level of timer 7 compare register 2-match interrupt , interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

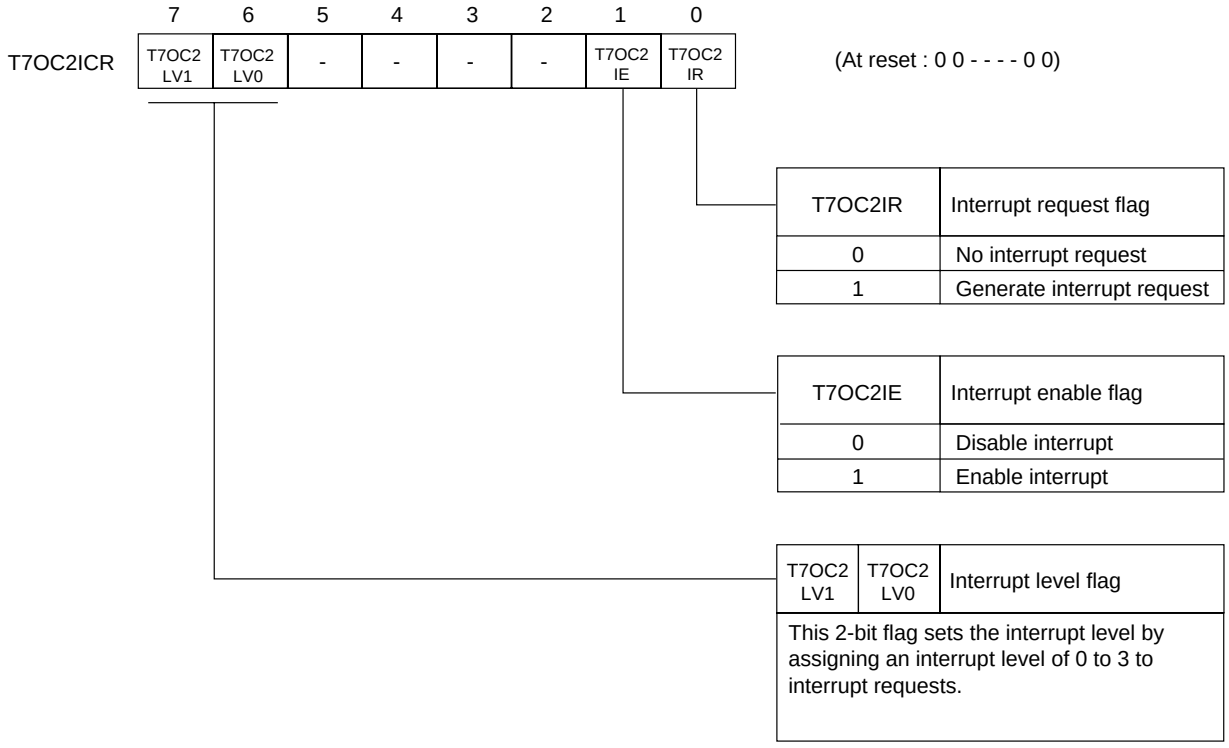


Figure 3-2-13 Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR : x'03FF2', R/W)

■Timer 8 Interrupt Control Register (TM8ICR)

The timer 8 interrupt control register (TM8ICR) controls interrupt level of timer 8 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

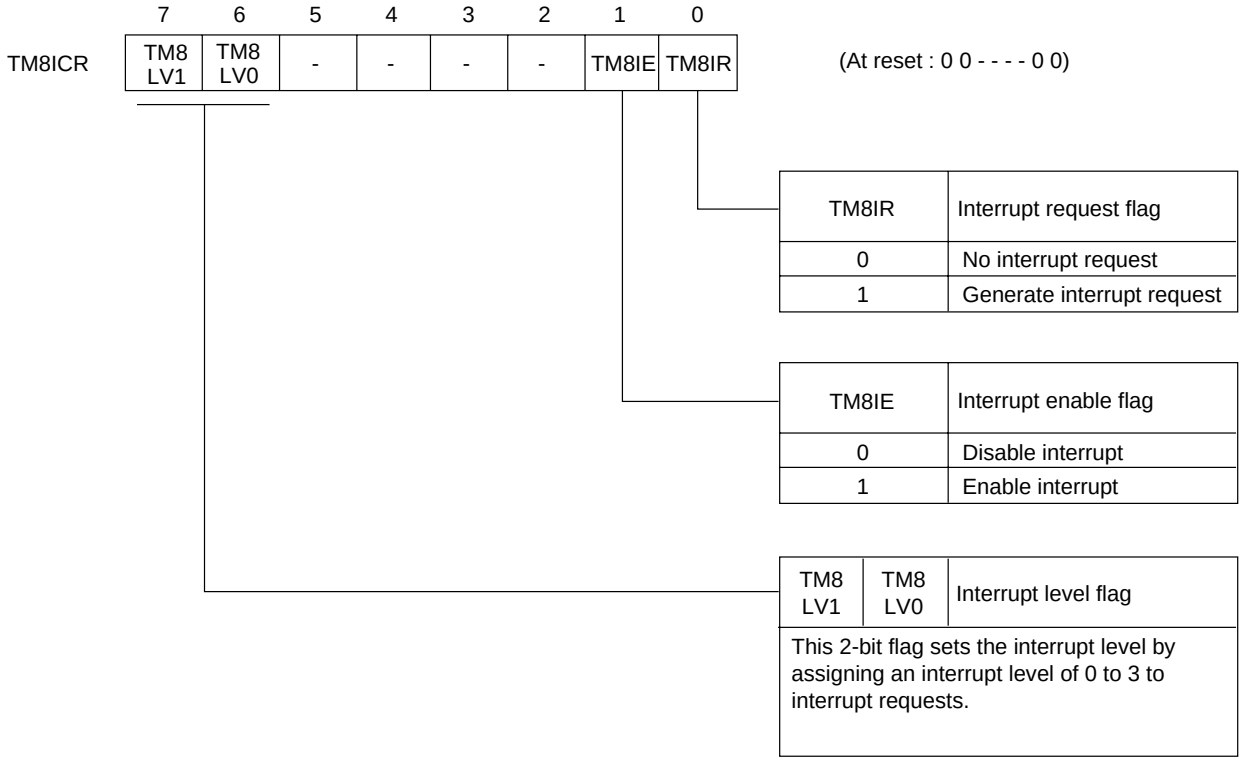


Figure 3-2-14 Timer 8 Interrupt Control Register (TM8ICR : x'03FF3', R/W)

■Serial 0 Interrupt Control Register 1 (SC0RICR)

The serial 0 interrupt control register 1 (SC0RICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

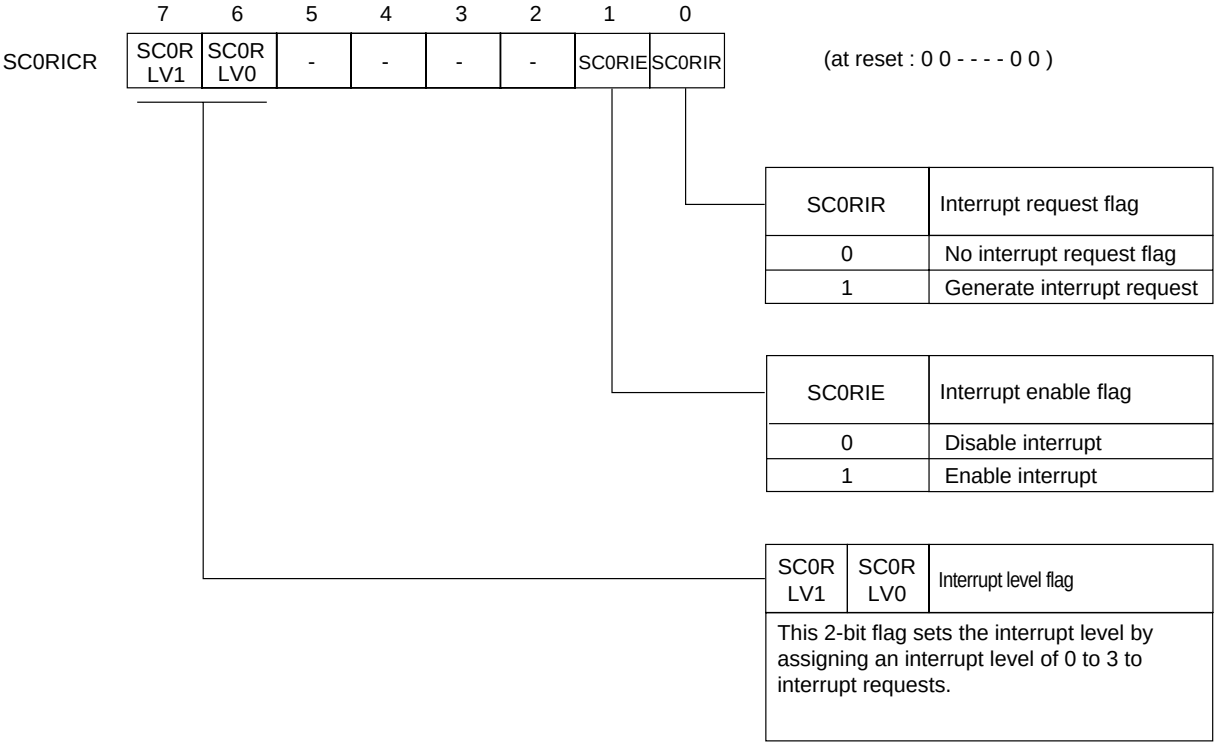


Figure 3-2-15 Serial 0 Interrupt Control Register 1 (SC0RICR : x'03FF5', R/W)

■Serial 0 Interrupt Control Register 2 (SC0TICR)

The serial 0 interrupt control register 2 (SC0TICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

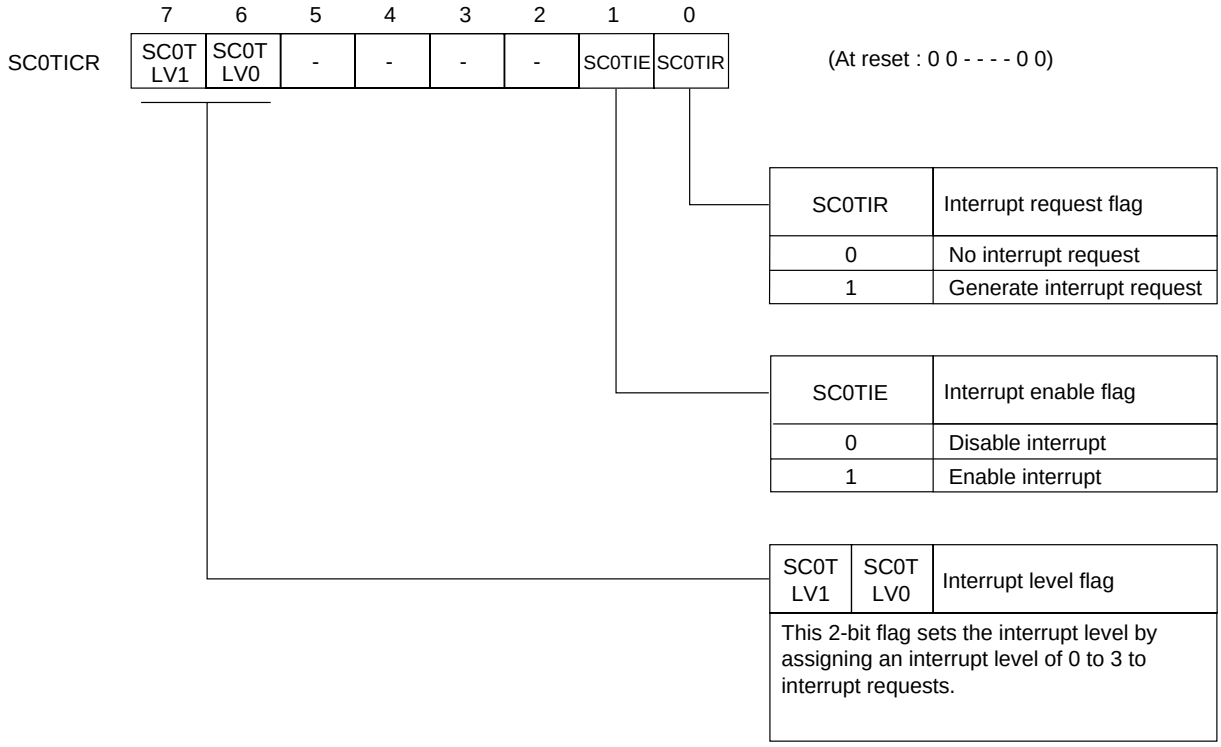


Figure 3-2-16 Serial 0 Interrupt Control Register 2 (SC0TICR : x'03FF6', R/W)

■A/D Conversion Interrupt Control Register (ADICR)

The A/D conversion interrupt control register (ADICR) controls interrupt level of A/D conversion interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

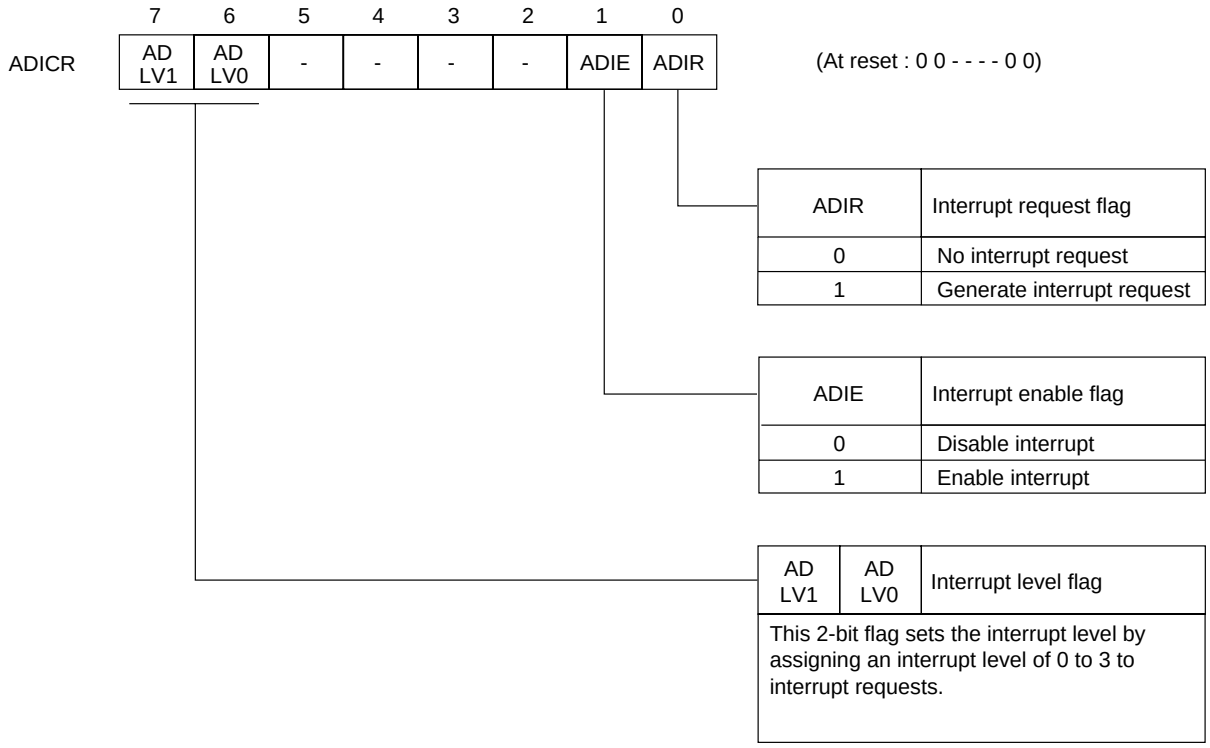


Figure 3-2-17 A/D Conversion Interrupt Control Register (ADICR : x'03FFA', R/W)

3-3 External Interrupts

There are 4 external interrupts in this LSI. The circuit (external interrupt interface), operates the external interrupt input signal, is built-in between the external interrupt input pin and the external interrupt block. This external interrupt interface can manage to do with any kind of external interrupts.

3-3-1 Overview

Table 3-3-1 shows the list of functions which external interrupts 0 to 2 and 4 are used.

Table 3-3-1 External Interrupt Functions

	External interrupt 0 (IRQ0)	External interrupt 1 (IRQ1)	External interrupt 2 (IRQ2)	External interrupt 4 (IRQ4)
External interrupt input pin	P20	P21	P22	KEY Interrupts Only
Programmable active edge interrupt	√	√	√	-
Both edges interrupt	-	-	√	-
Key input interrupt	-	-	-	√ (P60-P67)
Noise filter built-in	√	√	-	-
AC zero cross detection	-	√	-	-

3-3-2 Block Diagram

■External Interrupt 0 Interface, External Interrupt 1 Interface, Block Diagram

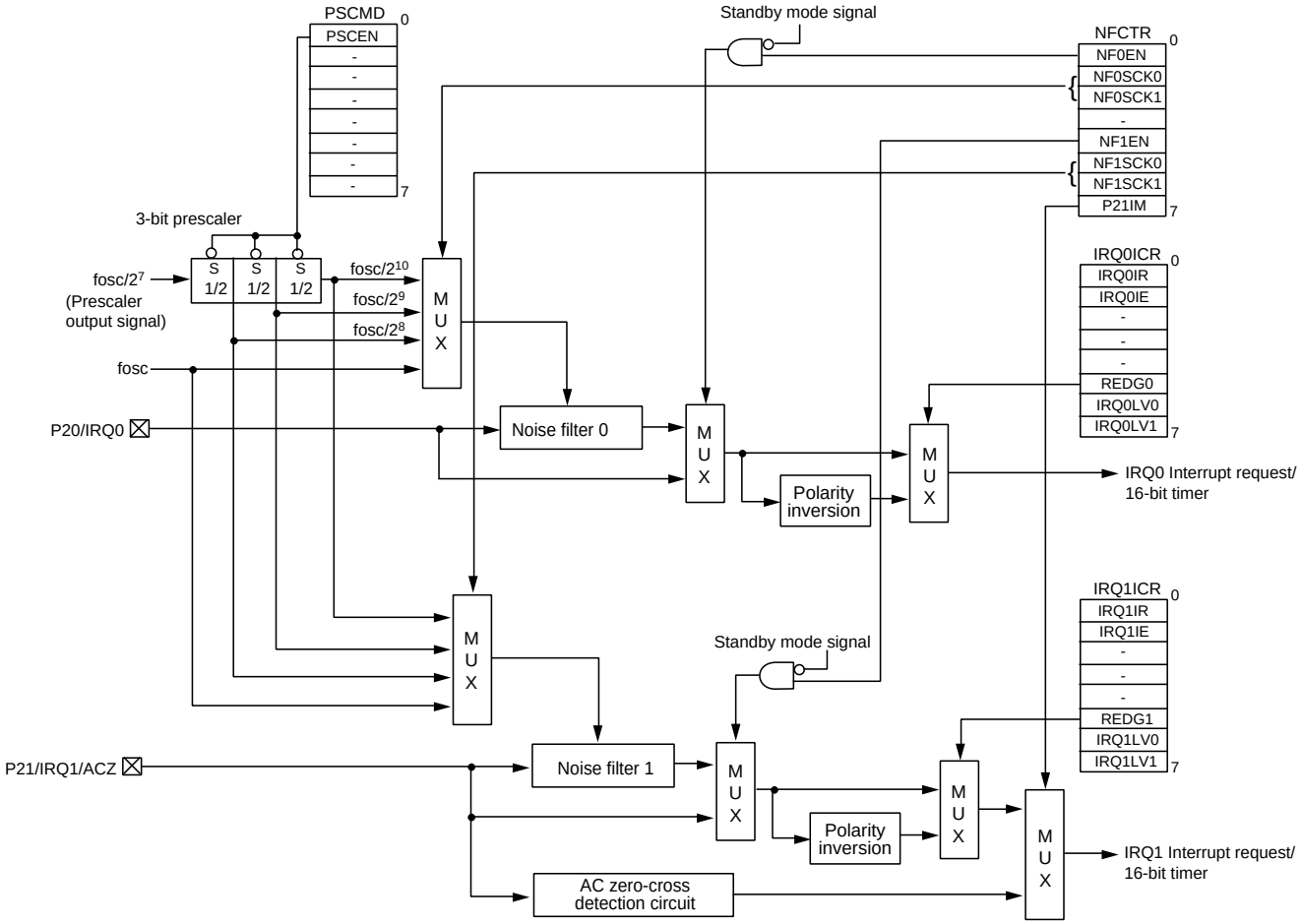


Figure 3-3-1 External Interrupt 0 Interface and External Interrupt 1 Interface, Block Diagram

■External Interrupt 2 Interface Block Diagram

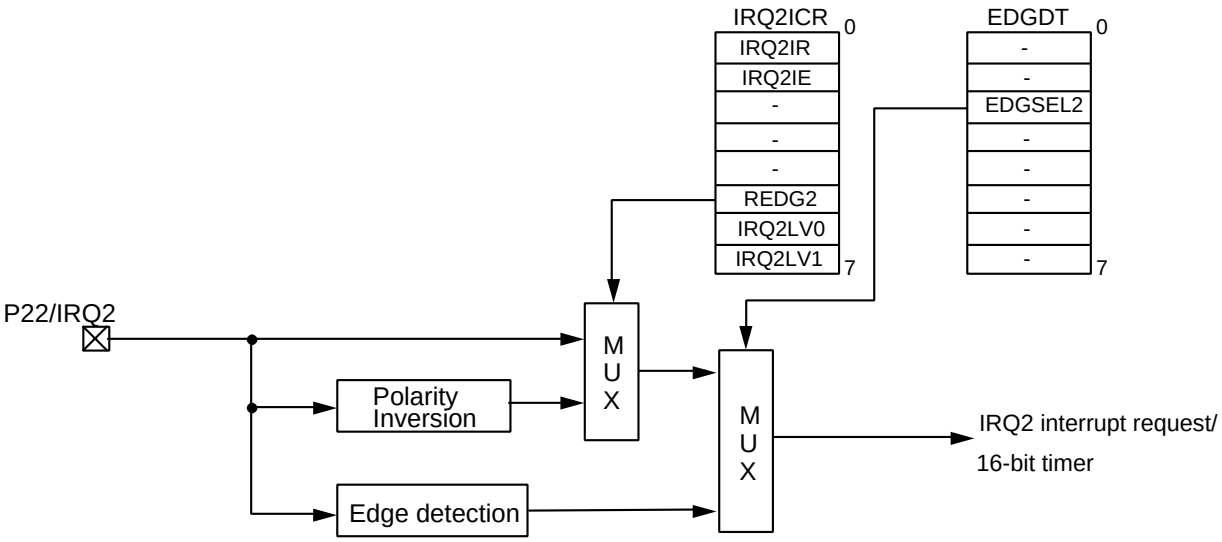


Figure 3-3-2 External Interrupt 2 Interface Block Diagram

■External Interrupt 4 Interface, Block Diagram

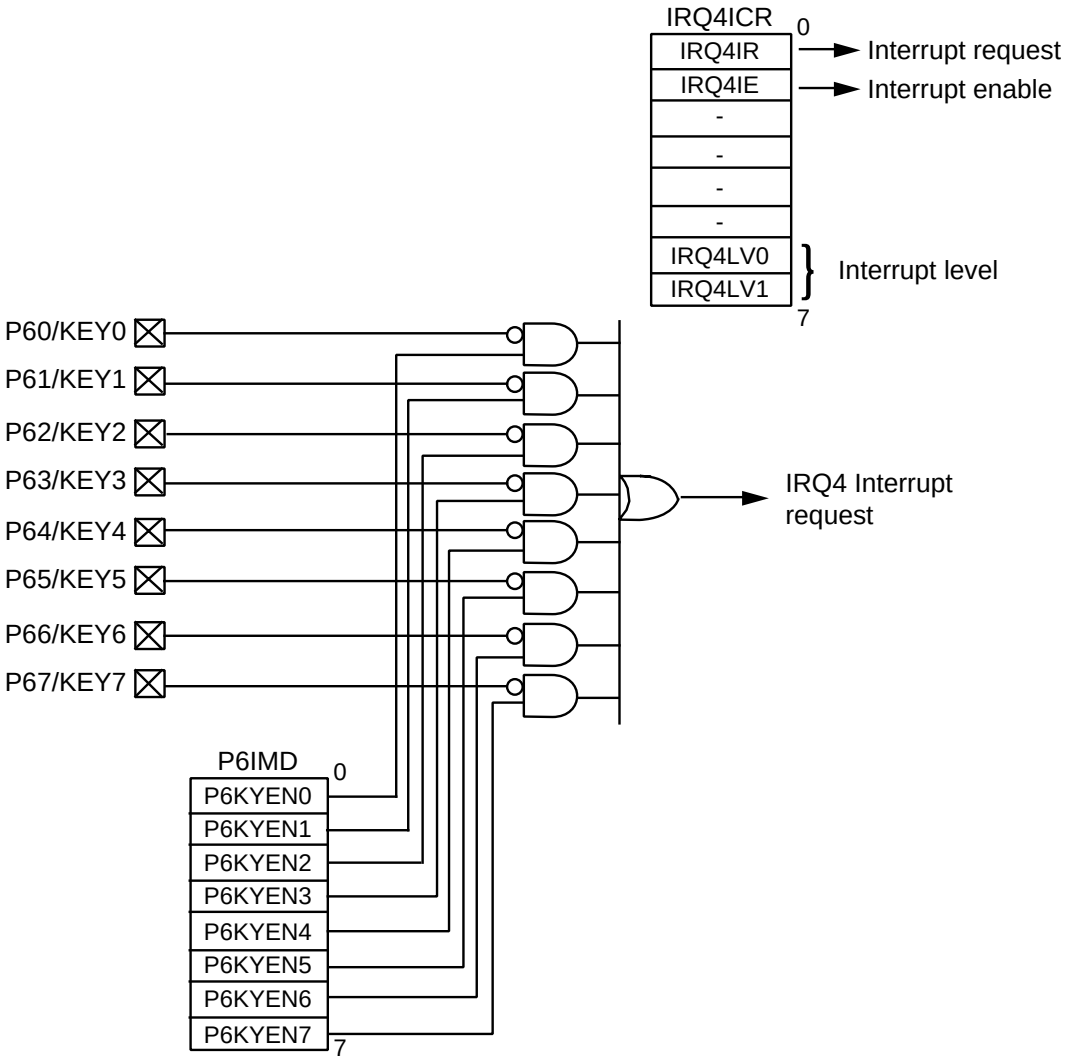


Figure 3-3-3 External Interrupt 4 Interface, Block Diagram

3-3-3 Control Registers

The external Interrupt input signals, which passed through each external interrupt interface 0 to 2 and 4 generate interrupt requests.

External interrupt 0 to 2 and 4 interface are controlled by the external interrupt control register (IRQnICR). External interrupt interface 0 to 1 are controlled by the noise filter control register (NFCTR), external interrupt interface 2 is controlled by the both edges interrupt control register (EDGDT), and external interrupt interface 4 is controlled by the port 6 key interrupt control register (P6IMD).

Table 3-3-2 shows the list of registers, which control external interrupt 0 to 2 and 3.

Table 3-3-2 External Interrupt Control Register

External Interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III -18
	NFCTR	x'03F8E'	R/W	Noise filter control register	III -39
External interrupt 1	IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III -19
	NFCTR	x'03F8E'	R/W	Noise filter control register	III -39
External interrupt 2	IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	III -20
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -40
External interrupt 4	IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	III -21
	P6IMD	x'03F3E'	R/W	Port 6 key interrupt control register	III -41

R/W : Readable / Writable.

■Noise Filter Control Register (NFCTR)

The noise filter control register (NFCTR) set the noise remove function to IQR0 and IRQ1 and also selects the sampling cycle of noise remove function. And this register also set the AC zero cross detection function to IRQ1.

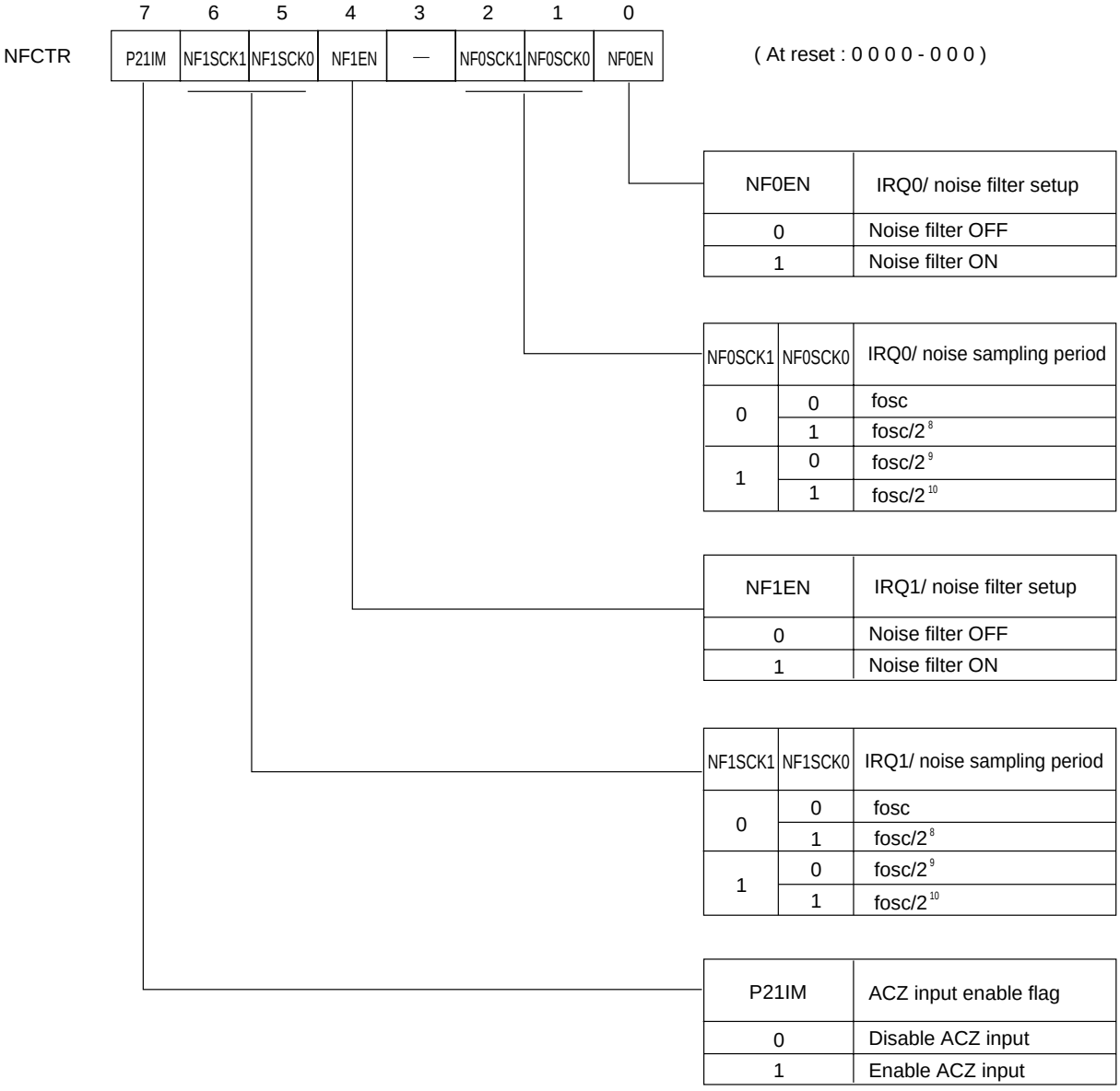

7 6 5 4 3 2 1 0
NFCTR
P21IM NF1SCK1 NF1SCK0 NF1EN — NF0SCK1 NF0SCK0 NF0EN
(At reset : 0 0 0 0 - 0 0 0)
NF0EN IRQ0/ noise filter setup
0 Noise filter OFF
1 Noise filter ON
NF0SCK1 NF0SCK0 IRQ0/ noise sampling period
0 0 fosc
1 fosc/2^8
1 0 fosc/2^9
1 fosc/2^10
NF1EN IRQ1/ noise filter setup
0 Noise filter OFF
1 Noise filter ON
NF1SCK1 NF1SCK0 IRQ1/ noise sampling period
0 0 fosc
1 fosc/2^8
1 0 fosc/2^9
1 fosc/2^10
P21IM ACZ input enable flag
0 Disable ACZ input
1 Enable ACZ input

Figure 3-3-4 Noise Filter Control Register (NFCTR : x'03F8E', R/W)

■Both Edges Interrupt Control Register (EDGDT)

The both edges interrupt control register (EDGDT) selects interrupt edges of IRQ2. Interrupts are generated at both edges, or at single edge. The external interrupt control register (IRQ2ICR) specifies whether interrupts are generated.

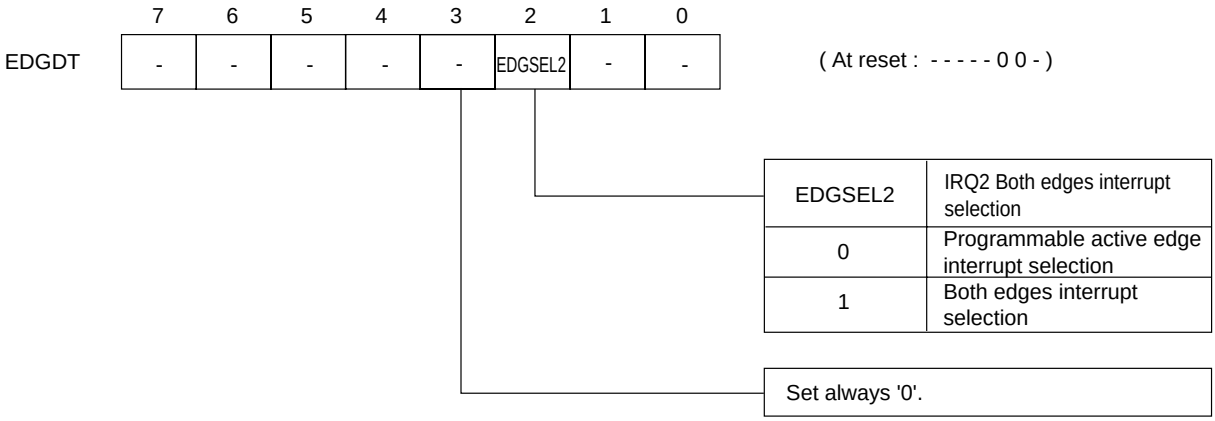

7 6 5 4 3 2 1 0
EDGDT
- - - - - EDGSEL2 - -
(At reset : - - - - - 0 0 -)
EDGSEL2
IRQ2 Both edges interrupt selection
0
Programmable active edge interrupt selection
1
Both edges interrupt selection
Set always '0'.

Figure 3-3-5 Both Edges Interrupt Control Register (EDGDT : x'03F8F', R/W)

■Port 6 Key Interrupt Control Register (P6IMD)

The port 6 key interrupt control register (P6IMD) selects if key interrupt is accepted. Also, this register assigns port6 pin to key interrupt in 1-bit unit.

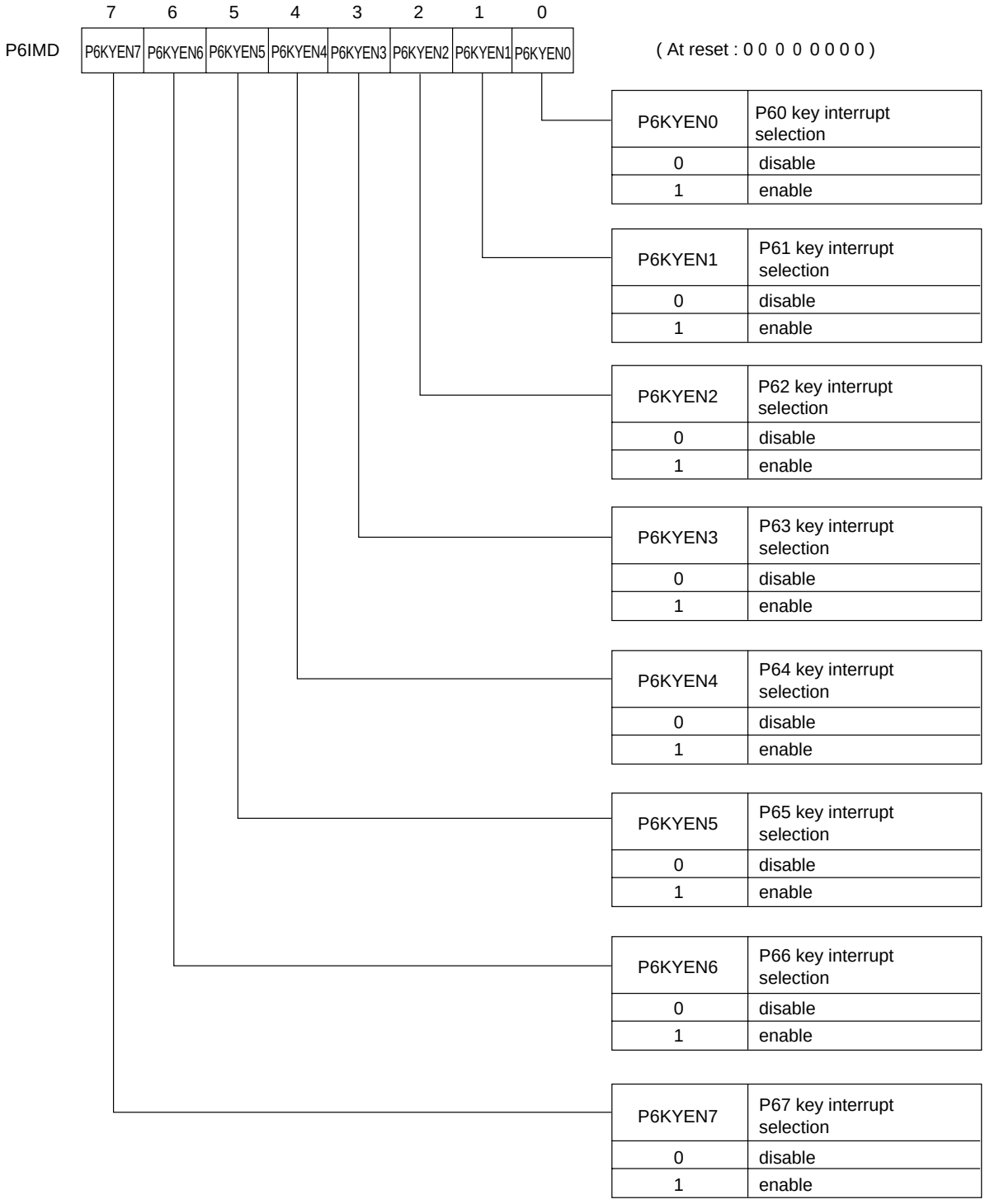


Figure 3-3-6 Port 6 Key Interrupt Control Register (P6IMD : x'03F3E', R/W)

3-3-4 Programmable Active Edge Interrupt

■Programmable Active Edge Interrupts (External interrupts 0 to 2)
Through register settings, external interrupts 0 to 2 are generated at either the rising or falling edge of the IRQ input signal. And this function can generate interrupt at the selected edge.

■Programmable Active Edge Interrupt Setup Example (External interrupt 0 to 2)
External interrupt 0 (IRQ0) is generated at the rising edge of the input signal from P20.
The table below provides a setup example for IRQ0.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the rising edge as the active edge for interrupts.
(2) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(2) Set the interrupt priority level in the IRQ0LV1-0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [☞ Chapter 3. 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(3) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

External interrupt 0 is generated at the rising edge of the input signal from P20.

The Interrupt request flag can be set at switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.

The external interrupt pin is recommended to be pull-up in advance.

When the programmable active edge interrupt is specified for external interrupt 2 (IRQ2), set the EDGSELn flag of the both edge interrupt control register (EDGDT) to "0".

3-3-5 Both Edges Interrupt

■Both Edges Interrupt (External interrupts 2)
Both edges interrupt can generate interrupt at both the falling edge and the rising edge by the input signal from external input pins. CPU also can be returned from standby mode.

■Both Edges Interrupt Setup Example (External interrupts 2)
External interrupt 2 (IRQ2) is generated at the both edges of the input signal from P22 pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the both edges interrupt. EDGDT (x'3F8F') bp2 : EDGSEL2 = 1	(1) Set the EDGSEL2 flag of the both edges interrupt control register (EDGDT) to "1" to select the both edges interrupt.
(2) Set the interrupt level. IRQ2ICR (x'3FE4') bp7-6 : IRQ2LV1- 0 = 10	(2) Set the interrupt level by the IRQ2LV1-0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). [☞ Chapter 3 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ2ICR (x'3FE4') bp1 : IRQ2IE = 1	(3) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.

At the both edge of the input signal from P22 pin, an external interrupt 2 is generated .

When the both edge interrupt is selected, the interrupt request is generated at the both edge, regardless of the REDGn flag of the external interrupt control register (IRQnICR).

The interrupt request flag may be set at switching the interrupt edge. So, clear the interrupt request flag before the interrupt acceptance. Also, select the both edge interrupt before the interrupt acceptance.

The external interrupt pin is recommended to be pull-up, in advance.

Interrupt is not accepted when the both edges interrupt is selected for external interrupt and both following conditions 1), 2) are fulfilled, and also the timings of the following two operations a), b) match.

1) The IRWE flag of the memory control register (MEMCTR) is set to "1" (Enable the interrupt request flag to be written by software)
2) Interrupt request flag (IRQnIR) of the external interrupt control register (IRQnICR) is set to "0" (no interrupt request)

a) Generation of write pulse, which rewrites "0" to the interrupt request flag (IRQnIR) of the IRQnICR.
b) Generation of interrupt request signal (interrupt edge) from external interface

When using both edges interrupt, rewrite to the interrupt request flag by software in following procedures.

(1) Disable all the maskable interrupts	MIE= 0
(2) Disable interrupt	IRQnIE= 0
(3) Select both edges interrupt	EDGSELn= 1
(4) Set the interrupt level	
(5) Enable the interrupt request flag to be written by software	IRWE= 1
(6) Set the interrupt request flag	IRQnIR= 1

Needs to be set before interrupt request flag is cleard

(7) Clear the interrupt request flag	IRQnIR= 0
(8) Disable the interrupt flag to be writen by software	IRWE= 0
(9) Enable the interrupt	IRQnIE= 1
(10) Enable all the maskable interrupt	MIE= 1

3-3-6 Key Input Interrupt

■Key Input Interrupt (External interrupt 4)

This LSI can set port 6 (P60 to P67) pin by 1 bit to key input pin. Key input interrupt can generate an interrupt at the falling edge, if at least 1 key input pin outputs low level.

Key input pin should be pull-up in advance.

■Key Input Interrupt Setup Example (External interrupt 4)

After P60 to P63 of port 6 are set to key input pins and key is input (low level), the external interrupt 4 (IRQ4) is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the key input pin to input. P6DIR (x'3F36') bp3-0 : P6DIR3-0 = 0000	(1) Set the P6DIR3-0 flag of the port 6 direction control register (P6DIR) to "0000" to set P60 to P63 pins to input pins.
(2) Set the pull-up resistance. P6PLUD (x'3F46') bp3-0 : P6PLU3-0 = 1111 FLOAT (x'3F2E') bp3 : P6RDWN = 0	(2) Set the P6PLUD3-0 flag of the port 6 pull-up/ pull down resistor control register (P6PLUD) to "1111" to add the pull-up resistors to P60 to P63 pins.
(3) Select the key input pin. P6IMD (x'3F3E') bp3-0 : P6KYEN3-0= 1111	(3) Set the P6KYEN3-0 flag of the port 6 key interrupt control register (P6IMD) to "1111" to set P60 to P63 pins to key input pins.
(4) Set the interrupt level. IRQ4ICR (x'3FE6') bp7-6 : IRQ4LV1-0= 10	(4) Set the interrupt level by the IRQ4LV1-0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ4ICR (x'3FE6') bp1 : IRQ4IE = 1	(5) Set the IRQ4IE flag of the IRQ4ICR register to "1" to enable the interrupt.

Note : Above (2) and (3) are set at the same time.

If there is at least one input signal, from the P40 to P47 pins, shows low level, the external interrupt 4 is generated at the falling edge.

The key input setings must be completed before the interrupt is accepted.

3-3-7 Noise Filter

■Noise Filter (External interrupts 0 and 1)

Noise filter reduce noise by sampling the input waveform from the external interrupt pins (IRQ0, IRQ1). Its sampling cycle can be selected from 4 types (fosc, fosc/2^8, fosc/2^9, fosc/2^{10}).

■Noise Remove Selection (External interrupts 0 and 1)

Noise remove function can be selected by setting the NFnEN flag of the noise filter control register (NFCTR) to "1".

Table 3-3-3 Addition of Noise Remove Function

NFnEN	IRQ0 input (P20)	IRQ1 input (P21)
0	IRQ0 Noise filter OFF	IRQ1 Noise filter OFF
1	IRQ0 Noise filter ON	IRQ1 Noise filter ON

■Sampling Cycle Setup (External interrupts 0 and 1)

The sampling cycle of noise remove function can be set by the NFnSCK1- 0 flag of the NFCTR register.

Table 3-3-4 Sampling Cycle / Time of Noise Remove Function

NFnCKS1	NFnCKS0	Sampling cycle	High-frequency oscillation			
			fosc=20 MHz		fosc=8 MHz	
0	0	fosc	20 MHz	50 ns	8 MHz	125 ns
	1	fosc/2^8	78.13 kHz	12.80 µs	31.25 kHz	32 µs
1	0	fosc/2^9	39.06 kHz	25.60 µs	15.62 kHz	64 µs
	1	fosc/2^{10}	19.53 kHz	51.20 µs	7.81 kHz	128 µs

When fosc/2^8, fosc/2^9 or fosc/2^{10} is selected as a sampling cycle, set the PSCEN flag of the prescaler control register (PSCMD) to "1" for the prescaler to be in operating state in advance.

■Noise Remove Function Operation (External interrupts 0 and 1)

After sampling the input signal to the external interrupt pins (IRQ0, IRQ1) with the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent. It means that only the signal with the amplitude of longer than " Sampling time X 3 sampling clock " can pass through the noise filter, and other signals with amplitude shorter than this are removed, because those are regarded as noise.

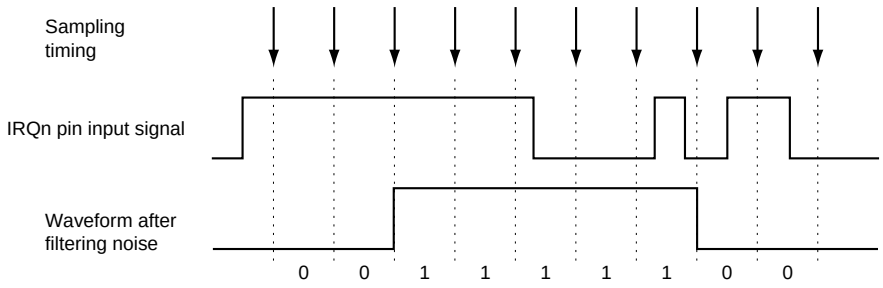


Figure 3-3-7 Noise Remove Function Operation

Noise filter can not be used at STOP mode, HALT mode and SLOW mode.

■Noise Filter Setup Example (External interrupt 0 and 1)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to fosc, and the operation state is fosc = 20 MHz. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the interrupt active edge to the rising edge.
(2) Select the sampling clock. NFCTR (x'3F8E') bp2-1 : NF0SCK1-0 = 000	(2) Select the sampling clock to fosc by the NF0SCK1-0 flag of the noise filter control register (NFCTR).
(3) Set the noise filter operation. NFCTR (x'3F8E') bp0 : NF0EN = 1	(3) Set the NF0EN flag of the NFCTR register to "1" to add the noise filter operation.
(4) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(4) Set the interrupt level by the IRQ0LV 1- 0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [☞Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(5) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

Note : Above (2) and (3) are set at the same time.

The input signal from the P20 pin generates the external interrupt 0 at the rising edge of the signal, after passing through the noise filter.

The setup of the noise filter should be done before the interrupt is enabled.

The external interrupt pins are recommended to be pull-up in advance.

3-3-8 AC Zero-Cross Detector

This LSI has AC zero-cross detector circuit. The P21 / ACZ pin is the input pin of AC zero-cross detector circuit. AC zero-cross detector circuit output the high level when the input level is at the middle, and outputs the low level at other level.

■AC Zero-Cross Detector (External interrupt 1)
AC zero-cross detector set the IRQ1 pin to the high level when the input signal (P21/ACZ pin) is at intermediate range by AC zero cross detector circuit. At the other level, IRQ1 pin is set to the low level. AC zero-cross detector is set by setting the P21IM flag of the noise filter control register (NFCTR) to "1".

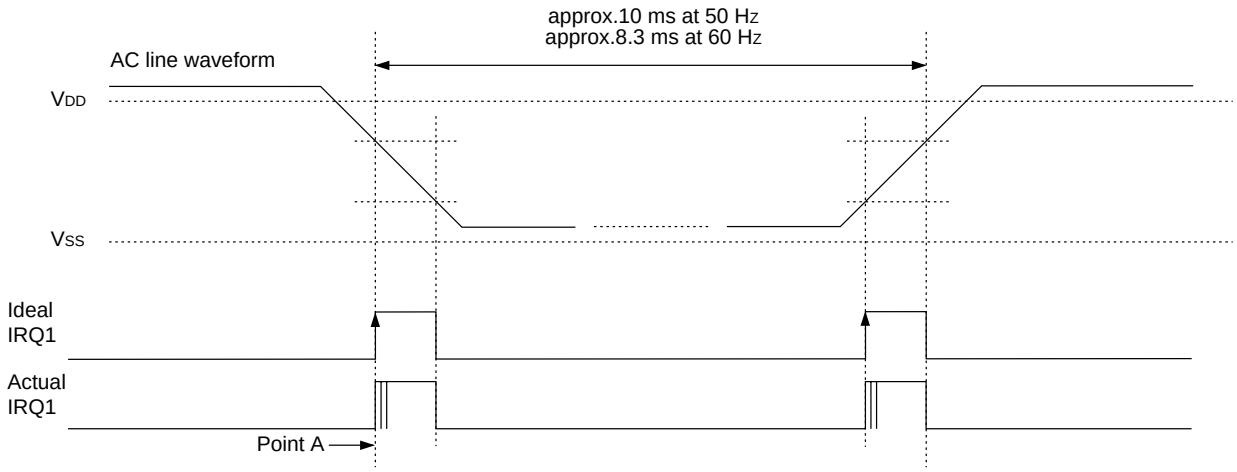


Figure 3-3-8 AC Line Waveform and IRQ1 Generation Timing

Actual IRQ1 interrupt request is generated several times at crossing the 1/2 V_{DD} of AC line waveform. So, the filtering operation by the program is needed.

The interrupt request is generated at the rising edge of the AC zero-cross detector signal.

■AC Zero-Cross Detector Setup Example (External interrupt 1)

AC zero-cross detector generates the external interrupt 1 (IRQ1) by using P21/ACZ pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the AC zero-cross detector signal. NFCTR (x'3F8E') bp7 : P21IM = 1	(1) Set the P21IM flag of the noise filter control register (NFCTR) to "1" to select the AC zero-cross detector signal as the external interrupt 1 generation factor.
(2) Set the interrupt level. IRQ1ICR (x'3FE3') bp7-6 : IRQ1LV1-0= 10	(2) Set the interrupt level by the IRQ1LV 1-0 flag of the IRQ1ICR register. If the interrupt request flag has been already set, clear the interrupt flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(3) Enable the interrupt. IRQ1ICR (x'3FE3') bp1 : IRQ1IE = 1	(3) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.

When the input level of the input signal from P21/ACZ pin cross 1/2V_{DD}, the external interrupt 1 is generated.

Chapter 4 I/O Ports

4

4-1 Overview

4-1-1 I/O Port Diagram

A total of 50 pins on this LSI, including those shared with special function pins, are allocated for the 9 I/O ports of port 0 to port 3, port 5 to port 8 and port A. Each I/O port is assigned to its corresponding special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.

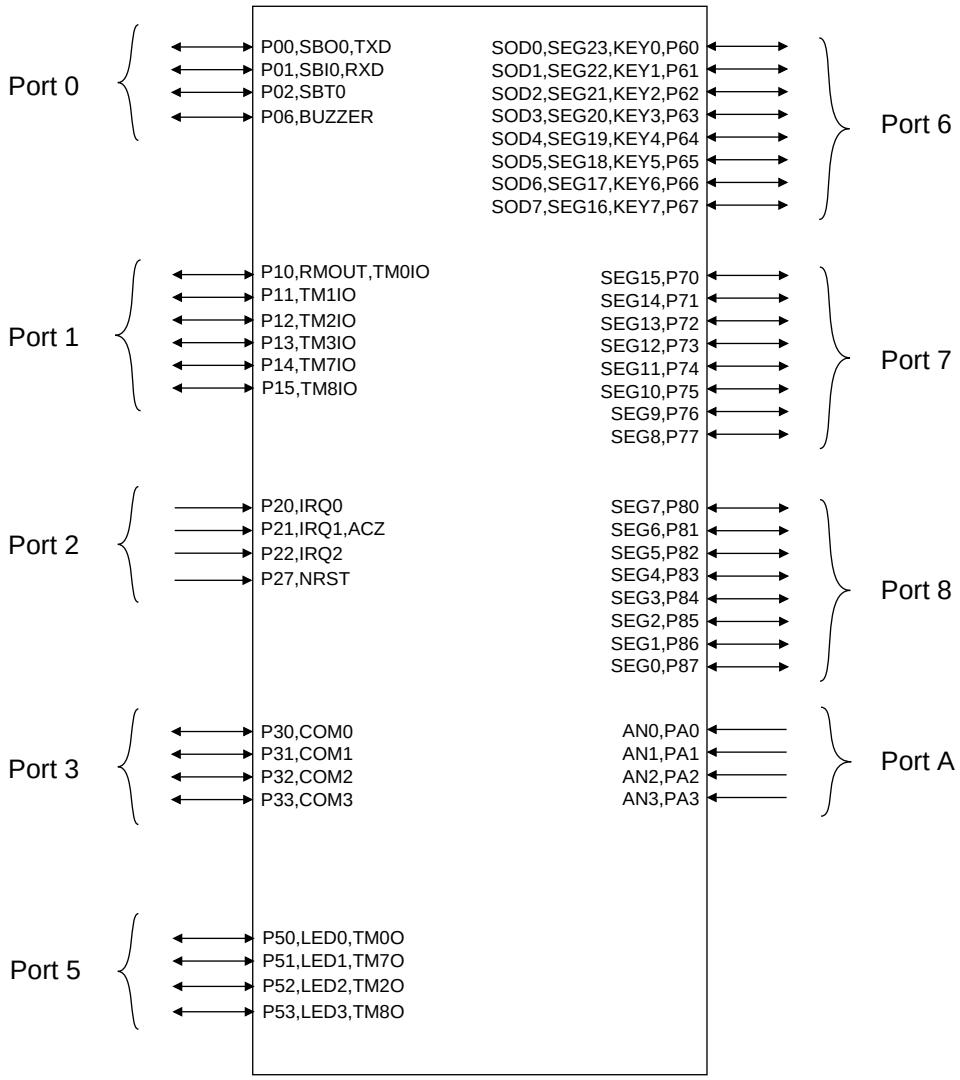


Figure 4-1-1 I/O Port Functions

4-1-2 I/O Port Status at Reset

Table 4-1-1 I/O Port Status at Reset (Single chip mode)

Port Name	I/O mode	Pull-up / Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	P27: Pull-up resistor Others : No pull-up resistor	I/O port
Port 3	Input mode	No pull-up resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up/pull-down resistor	I/O port
Port 7	Input mode	No pull-up/pull-down resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up / pull-down resistor	I/O port

The values of pull-up/pull-down resistors should be caluculated in following ways based on the electrical characteristics in LSI User's Manual of each model.

How to determine pull-up resistor value

ex) When pins maintain the low level guaranteed performance (not 0 V) as specified in the electrical characteristics,
and at V_{DD} = 5 V, V_{IN} = 1.5 V,
input current is min. = - 30 μA, typ = - 100 μA, max. = - 300 μA.
(- means current passing from microcontroller.)
When convert above values to resistor value, typ = 35 kΩ.
Note that this value varies wildely depending on the temperature.
In temperature variation from - 40 °C to 85 °C, the resistor value varies from min. = 11.7 kΩ to max. = 117 kΩ.

How to determine pull-down resistor value

ex) When pins maintain the high level guaranteed performance (not V_{DD}) as specified in the electrical characteristics,
and at V_{DD} = 5 V, V_{IN} = 3.5 V,
input current is min. = - 30 μA, typ = - 100 μA, max. = - 300 μA.
When convert these values to resistance value, typ = 35 kΩ.
Note that this value varies wildely depending on the temperature.
In temperature variation from - 40 °C to 85 °C, the resistor value varies from min. = 11.7 kΩ to max. = 117 kΩ.

4-1-3 Control Registers

Ports 0 to 3, port 5 to 8 and port A are controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) or the pull-up / pull-down resistor control resister (PnPLUD) and registers that control special function pin (P1OMD, P5OMD, PAIMD, P6IMD, P6SYO, FLOAT).

Table 4-1-2 shows the registers to control ports 0 to 3, port 5 to 8 and port A;

Table 4-1-2 I/O Port Control Registers List (1/2)

	Register	Address	R/W	Function	Page
Port 0	P0OUT	x'03F10'	R/W	Port 0 output register	IV - 7
	P0IN	x'03F20'	R	Port 0 input register	IV - 7
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLU	x'03F40'	R/W	Port 0 pull-up resistor control register	IV - 7
Port 1	P1OUT	x'03F11'	R/W	Port 1 output register	IV - 11
	P1IN	x'03F21'	R	Port 1 input register	IV - 11
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 11
	P1PLU	x'03F41'	R/W	Port 1 pull-up resistor control register	IV - 11
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 12
Port 2	P2OUT	x'03F12'	R/W	Port 2 output register	IV - 15
	P2IN	x'03F22'	R	Port 2 input register	IV - 15
	P2PLU	x'03F42'	R/W	Port 2 pull-up resistor control register	IV - 15
Port 3	P3OUT	x'03F13'	R/W	Port 3 output register	IV - 18
	P3IN	x'03F23'	R	Port 3 input register	IV - 18
	P3DIR	x'03F33'	R/W	Port 3 direction control register	IV - 18
	P3PLU	x'03F43'	R/W	Port 3 pull-up resistor control register	IV - 18

Table 4-1-3 I/O Port Control Registers List (2/2)

	Register	Address	R/W	Function	Page
Port 5	P5OUT	x'03F15'	R/W	Port 5 output register	Ⅳ - 22
	P5IN	x'03F25'	R	Port 5 input register	Ⅳ - 22
	P5DIR	x'03F35'	R/W	Port 5 direction control register	Ⅳ - 22
	P5PLU	x'03F45'	R/W	Port 5 pull-up resistor control register	Ⅳ - 22
	P5OMD	x'03F3F'	R/W	Port 5 output mode register	Ⅳ - 23
Port 6	P6OUT	x'03F16'	R/W	Port 6 output register	Ⅳ - 26
	P6IN	x'03F26'	R	Port 6 input register	Ⅳ - 26
	P6IMD	x'03F3E'	R/W	Port 6 input mode register	Ⅲ - 40
	P6DIR	x'03F36'	R/W	Port 6 direction control register	Ⅳ-26
	P6PLUD	x'03F46'	R/W	Port 6 pull-up/pull-down resistor control register	Ⅳ - 26
	P6SYO	x'03F1E'	R/W	Port 6 synchronous output control register	Ⅳ - 27
Port 7	P7OUT	x'03F17'	R/W	Port 7 output register	Ⅳ - 31
	P7IN	x'03F27'	R	Port 7 input register	Ⅳ - 31
	P7DIR	x'03F37'	R/W	Port 7 direction control register	Ⅳ - 31
	P7PLUD	x'03F47'	R/W	Port 7 pull-up/pull-down resistor control register	Ⅳ - 31
Port 8	P8OUT	x'03F18'	R/W	Port 8 output register	Ⅳ - 36
	P8IN	x'03F28'	R	Port 8 input register	Ⅳ - 36
	P8DIR	x'03F38'	R/W	Port 8 direction control register	Ⅳ - 36
	P8PLU	x'03F48'	R/W	Port 8 pull-up resistor control register	Ⅳ - 36
Port A	PAIN	x'03F2A'	R	Port A input register	Ⅳ - 40
	PAIMD	x'03F3A'	R/W	Port A input mode register	Ⅳ - 40
	PAPLUD	x'03F4A'	R/W	Port A pull-up / pull-down resistor control register	Ⅳ - 40
Pin control	FLOAT	x'03F2E'	R/W	Pull-up / Pull-down resistor selection, pin control register	Ⅳ - 27, 32, 41
LCD output control	LCDMD2	x'03FDA'	R/W	LCD mode control register 2	Ⅳ - 19, XIII - 7
	LCCTR1	x'03FDB'	R/W	LCD output control register 1	Ⅳ - 33, 37, XIII - 8
	LCCTR2	x'03FDC'	R/W	LCD output control register 2	Ⅳ - 28, XIII - 9

4-2 Port 0

4-2-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port 0 control I/O direction register (P0DIR). The control flag of the port 0 direction control register (P0DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 0 direction control register (P0DIR) to "0" and read the value of the port 0 input register (P0IN).

To output data to pin, set the control flag of the port 0 direction control register (P0DIR) to "1" and write the data to the port 0 output register (P0OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 0 pull-up resistor control register (P0PLU). Set the control flag of the port 0 pull-up resistor control register (P0PLU) to "1" to add pull-up resistor.

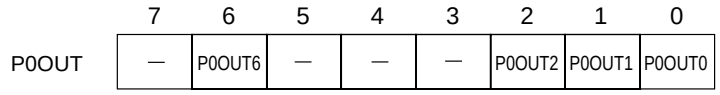
■Special Function Pin Setup

P00 to P02 are used as I/O pin for serial 0 as well. P00 is output pins of the serial 0 transmission data. When the SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P00 is serial data output pins. P01 is the input pins of the serial 0 reception data. P03 is I/O pins of the serial 0 clock. When the SC0SBTS flag of serial interface 0 mode register 1 (SC0MD1) is "1", P03 is serial clock output pins. P00 and P01 can be selected as either an push-pull output or Nch open-drain output by the serial interface 0 port control registers (SC0ODC).

[☞ Chapter 11 11-2. Control registers]

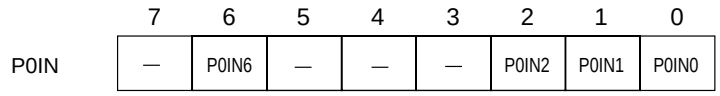
P06 is used as a buzzer output pin, as well. When the bp7 of the oscillation stabilization control register (DLYCTR) is "1", buzzer output is enabled.

4-2-2 Registers



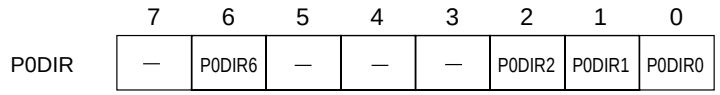
P0OUT	Output data
0	L(V_{SS} level) is output.
1	H(V_{DD} level) is output.

Port 0 output register (P0OUT : x'03F10', R/W)



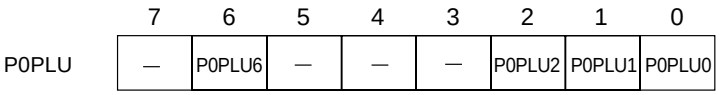
P0IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 0 input register (P0IN : x'03F20', R)



P0DIR	I/O mode selection
0	Input mode
1	Output mode

Port 0 direction control register (P0DIR : x'03F30', R/W)



P0PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 0 pull-up resistor control register (P0PLU : x'03F40', R/W)

Figure 4-2-1 Port 0 Registers (1/2)

4-2-3 Block Diagram

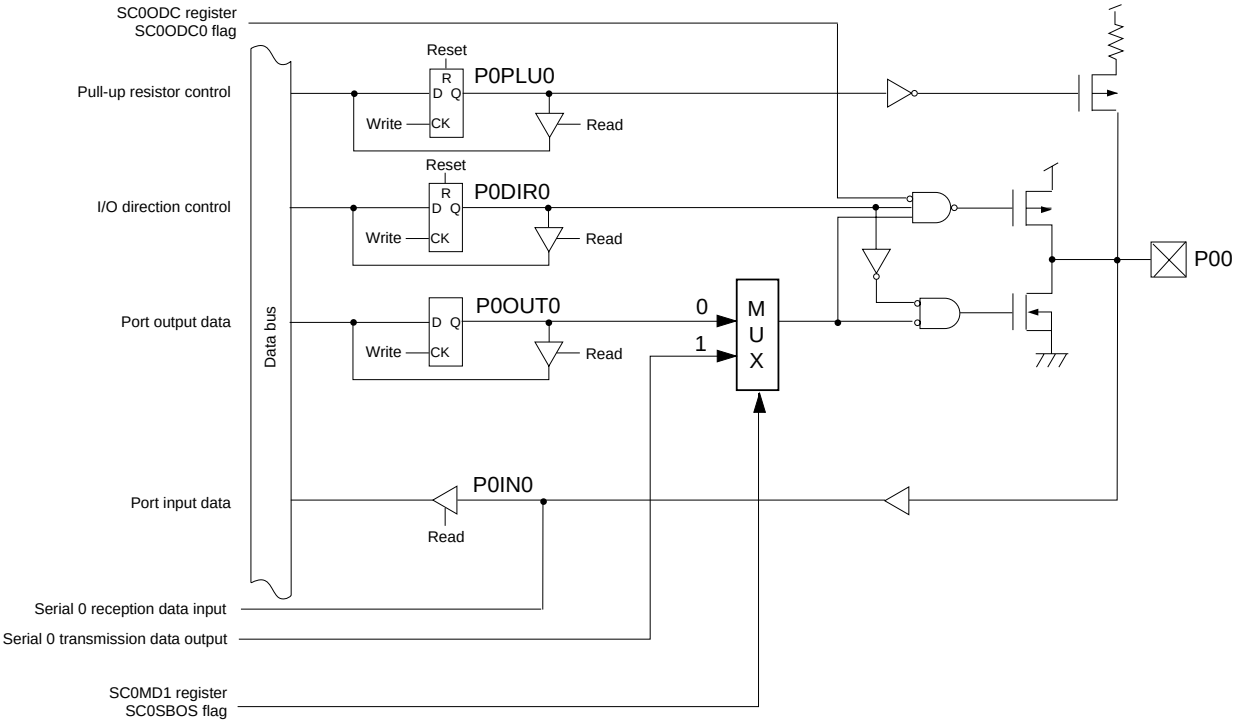


Figure 4-2-2 Block diagram (P00)

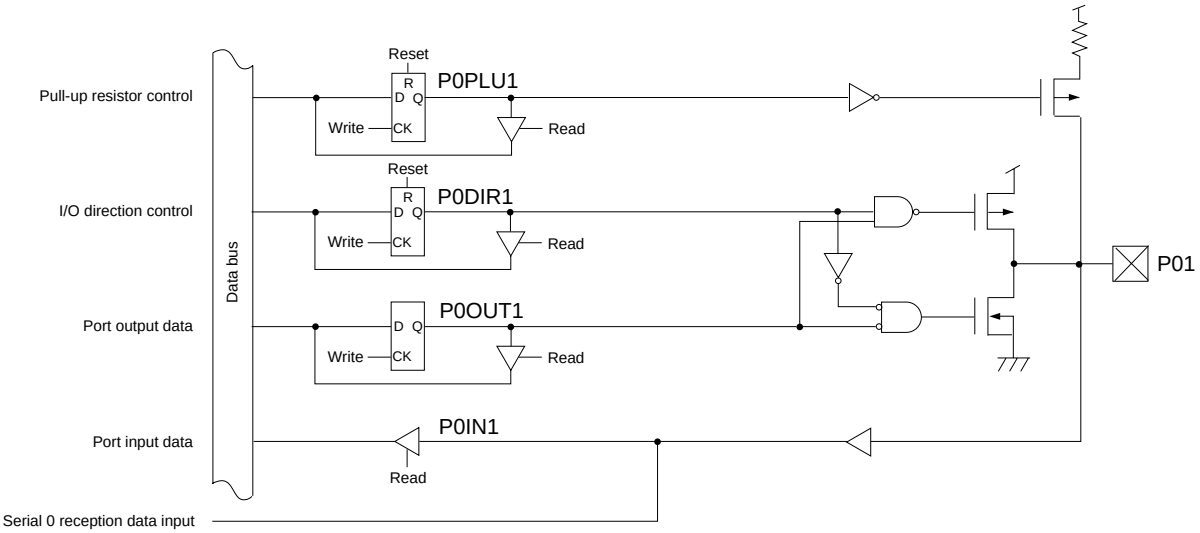


Figure 4-2-3 Block diagram (P01)

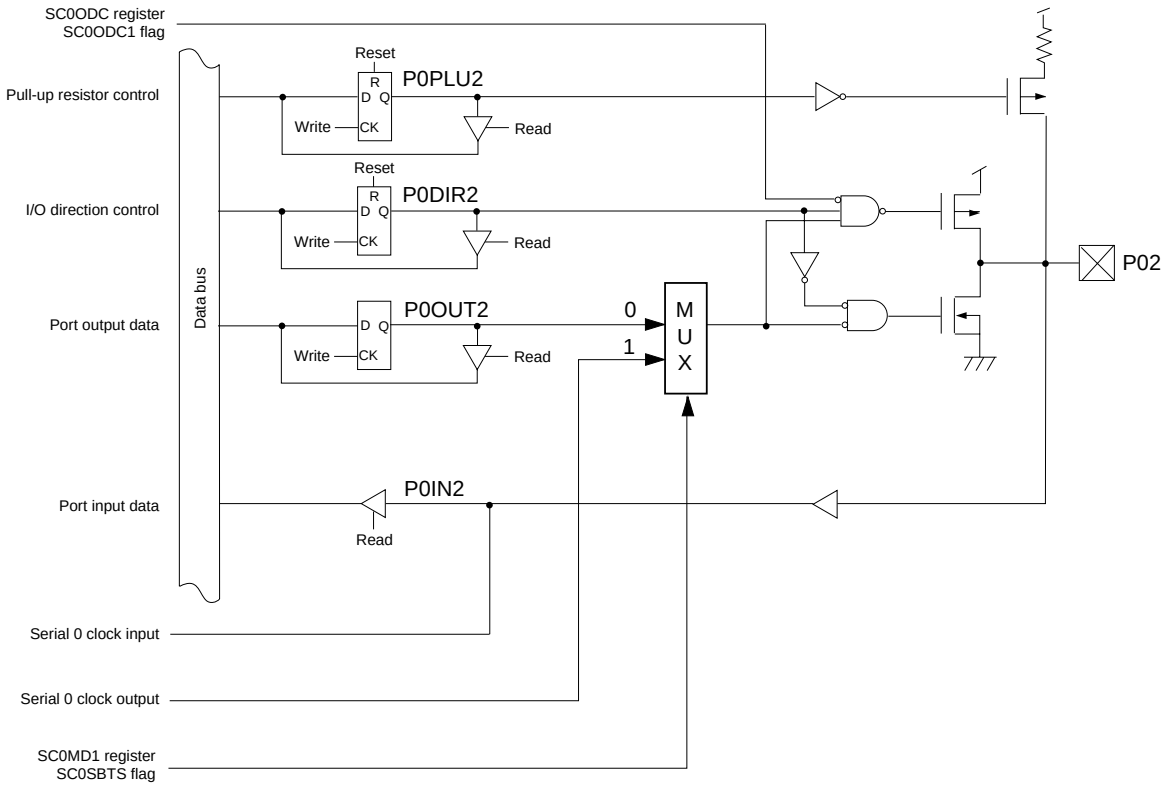


Figure 4-2-4 Block diagram (P02)

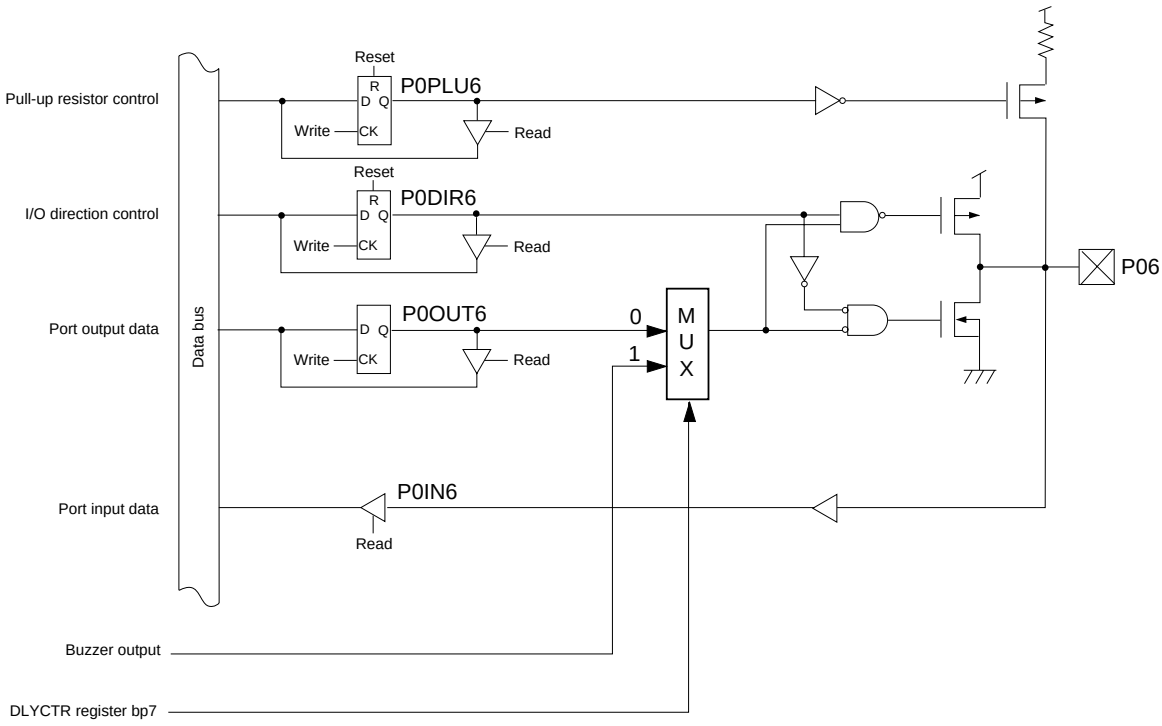


Figure 4-2-5 Block diagram (P06)

4-3 Port 1

4-3-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port 1 I/O direction control register (P1DIR). The control flag of the port 1 direction control register (P1DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 1 direction control register (P1DIR) to "0" and read the value of the port 1 input register (P1IN).

To output data to pin, set the control flag of the port 1 direction control register (P1DIR) to "1" and write the value of the port 1 output register (P1OUT).

Each bit can be set individually if pull-up resistor is added or not with the port 1 pull-up resistor control register (P1PLU). Set the control flag of the port 1 pull-up resistor control register (P1PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

P10 to P15 are used as timer I/O pin, as well. P10 is used as remote control carrier output pin, as well. The port 1 output mode register (P1OMD) can select P10 to P15 output mode by each bit. When the port 1 output mode register (P1OMD) is "1", special function data is output, and when it is "0", they are used as general port.

4-3-2 Registers

	7	6	5	4	3	2	1	0	
P1OUT	—	—	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	(At reset : - - X X X X X X)

P1OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 1 output register (P1OUT : x'03F11', R/W)

	7	6	5	4	3	2	1	0	
P1IN	—	—	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	(At reset : - - X X X X X X)

P1IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 1 input register (P1IN : x'03F21', R)

	7	6	5	4	3	2	1	0	
P1DIR	—	—	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	(At reset : - - 0 0 0 0 0 0)

P1DIR	I/O mode selection
0	Input mode
1	Output mode

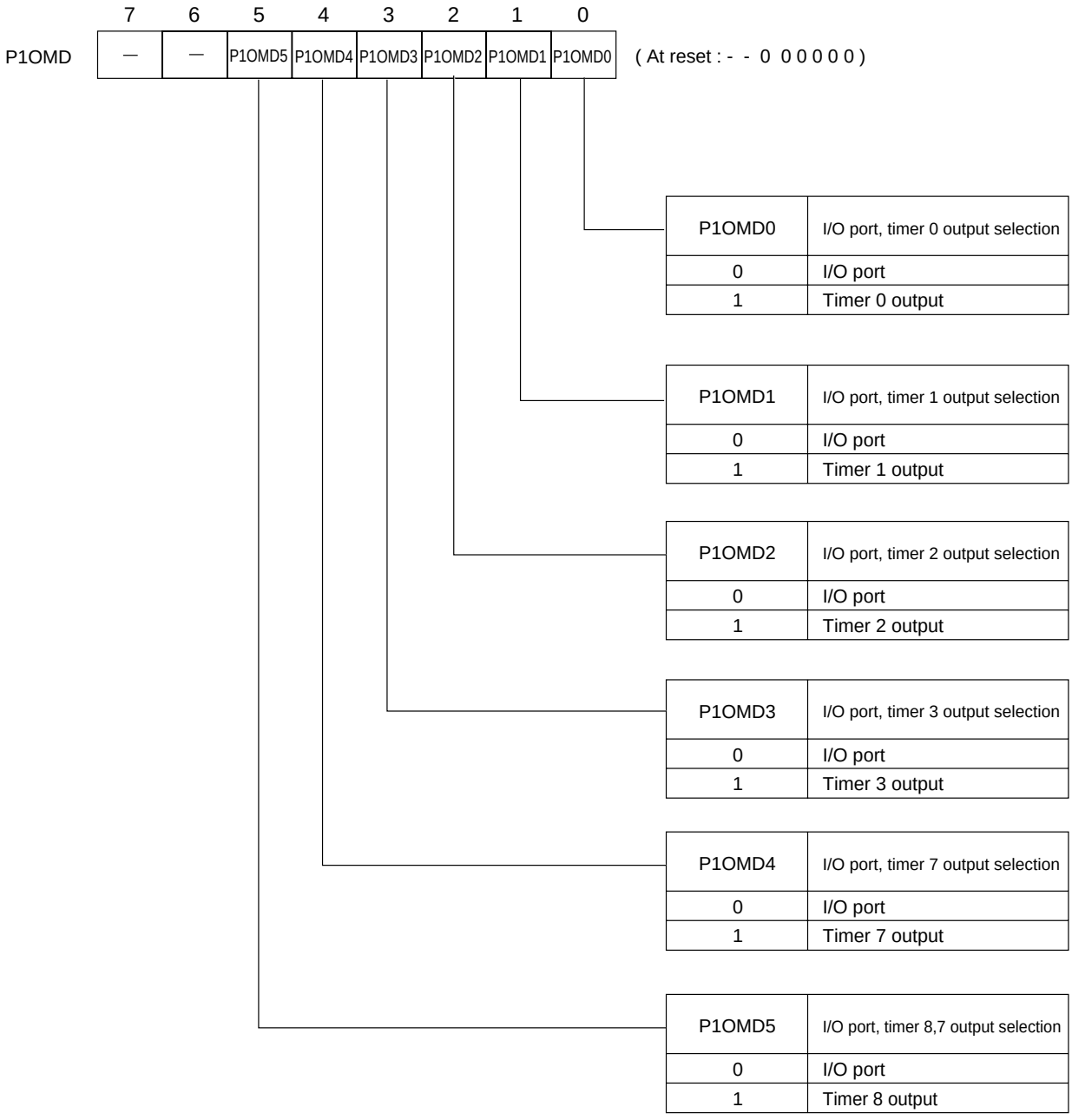
Port 1 direction control register (P1DIR : x'03F31', R/W)

	7	6	5	4	3	2	1	0	
P1PLU	—	—	P1PLU5	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	(At reset : - - 0 0 0 0 0 0)

P1PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 1 pull-up resistor control register (P1PLU : x'03F41', R/W)

Figure 4-3-1 Port 1 Registers (1/3)



Port 1 output mode register (P1OMD : x'03F2F', R/W)

Figure 4-3-2 Port 1 Registers (2/3)

4-3-3 Block Diagram

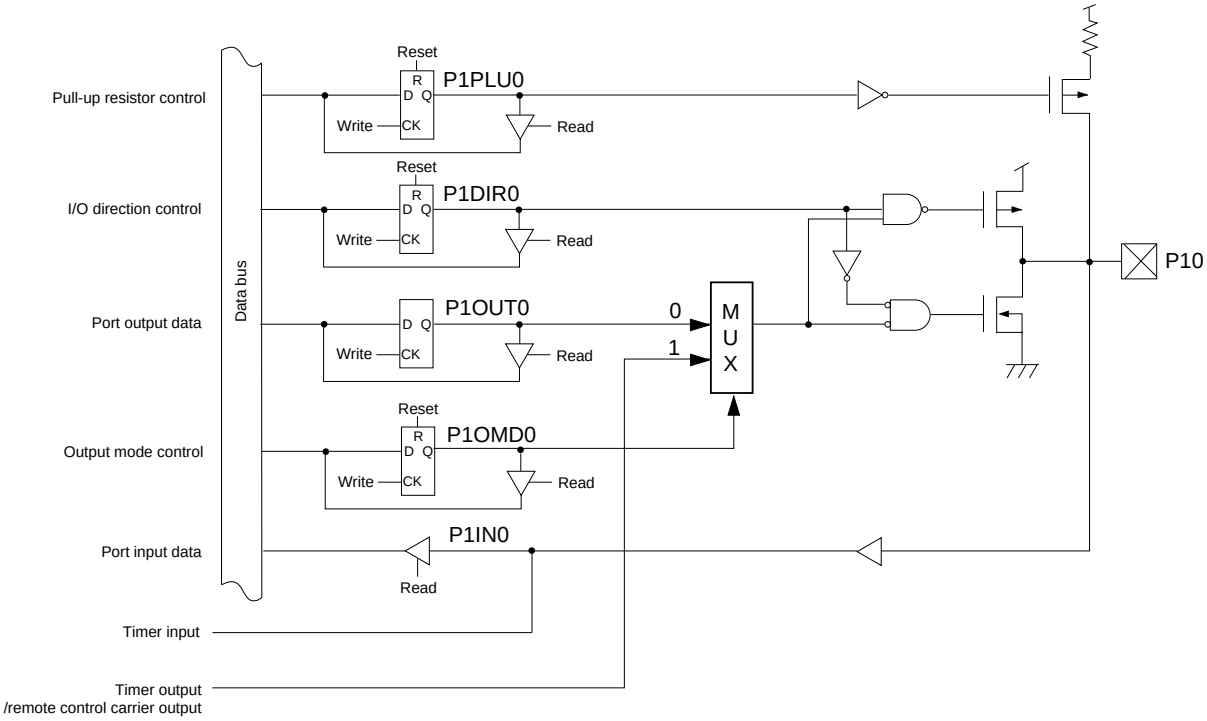


Figure 4-3-3 Block Diagram (P10)

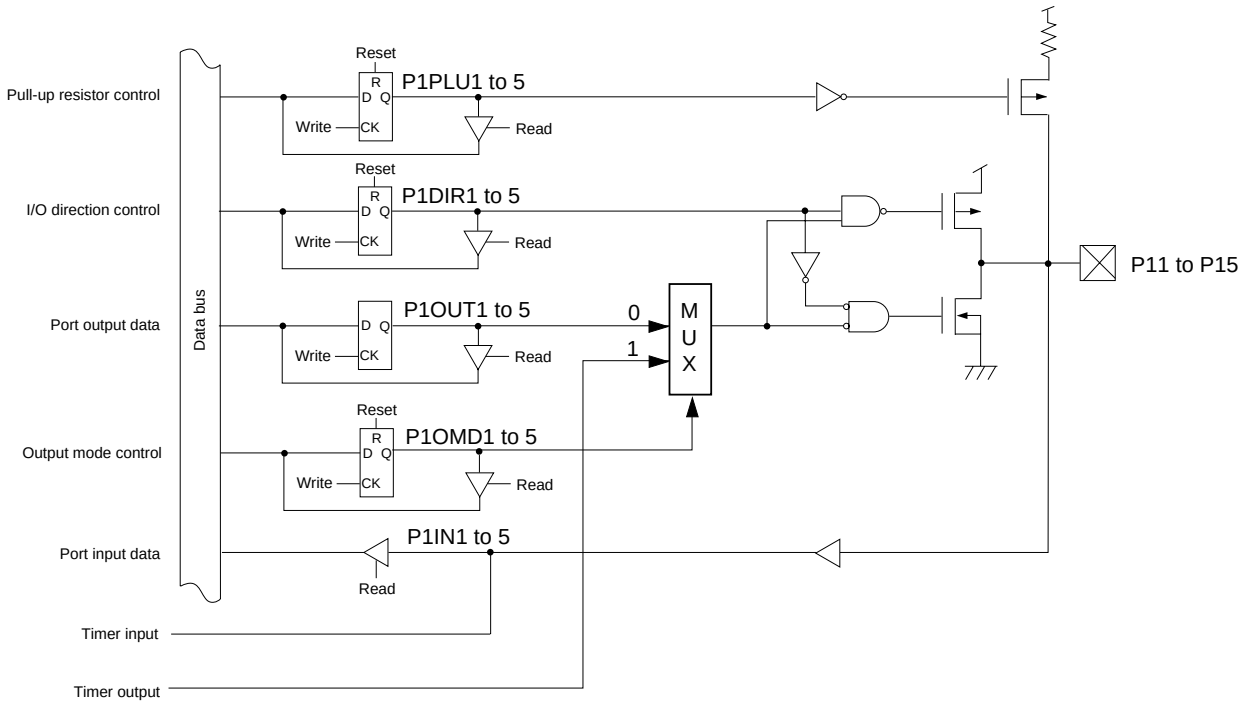


Figure 4-3-4 Block Diagram (P11 to P15)

4-4 Port 2

4-4-1 Description

■General Port Setup
Port 2 is input port, except P27. To read input data of pin, read out the value of the port 2 input register (P2IN).

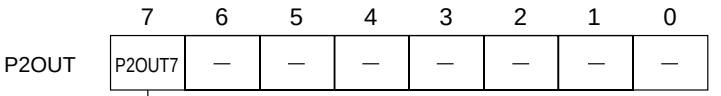
P27 is reset pin. When the software is reset, write "0" to the bp7 of the port 2 output register (P2OUT).

The port 2 pull-up resistor control register (P2PLU) can select if port 2 is added pull-up resistor or not, by 1 bit. When the control flag of the port 2 pull-up resistor control register (P2PLU) is set to "1", pull-up resistor is added. P27 is always added pull-up resistor.

■Special Function Pin Setup
P20 and P22 are used as external interrupt pins, as well.

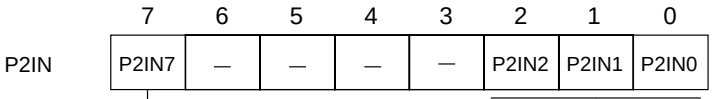
P21 is used as an input pin for external interrupt and AC zero-cross. To read data of AC zero-cross, set "1" to the bp7 of the noise filter control register (NFCTR) and read the value of the port 2 input register (P2IN).

4-4-2 Registers



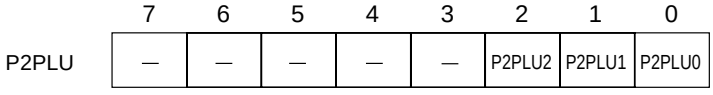
P2OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 2 output register(P2OUT : x'03F12', R/W)



P2IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 2 input register(P2IN : x'03F22', R)



P2PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 2 pull-up resistor control register(P2PLU : x'03F42', R/W)

Figure 4-4-1 Port 2 Registers

4-4-3 Block Diagram

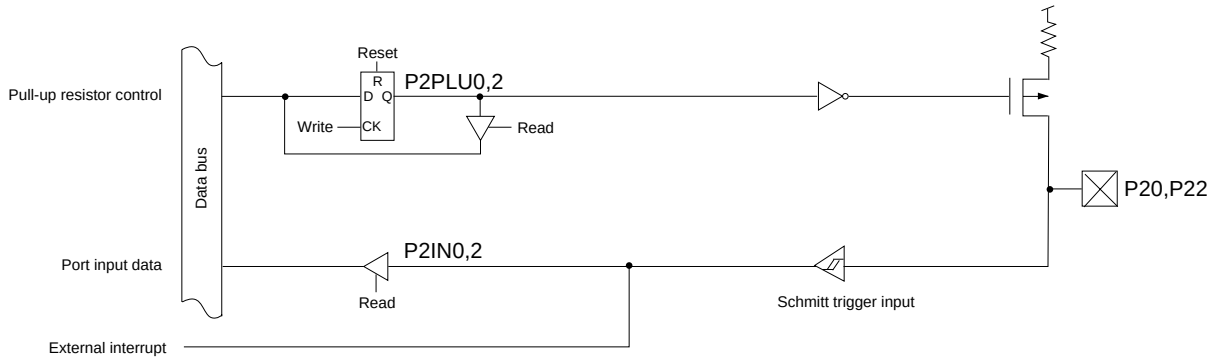


Figure 4-4-2 Block Diagram (P20 and P22)

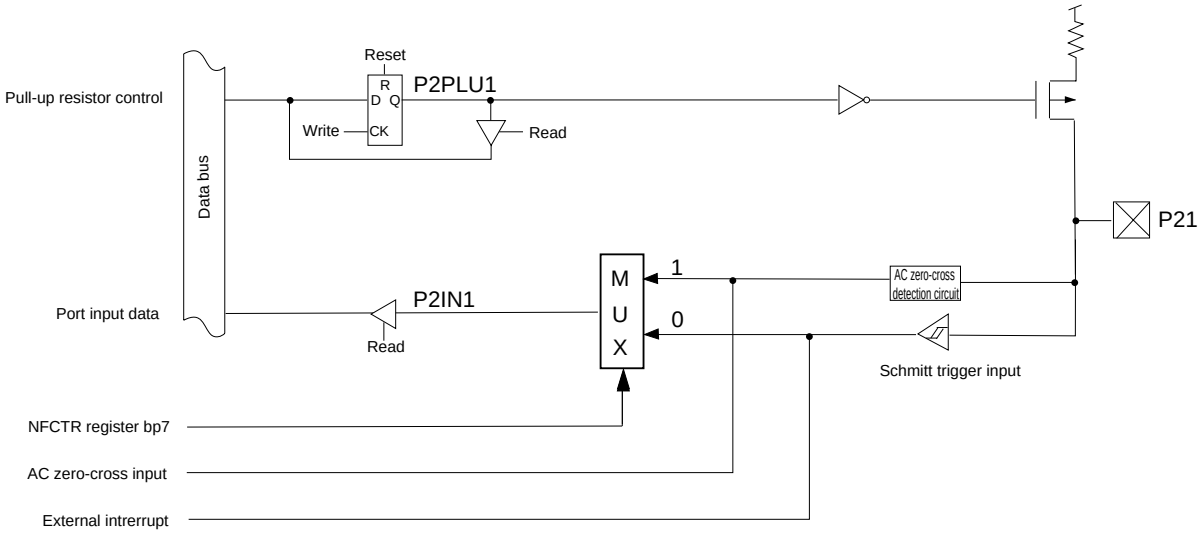


Figure 4-4-3 Block Diagram (P21)

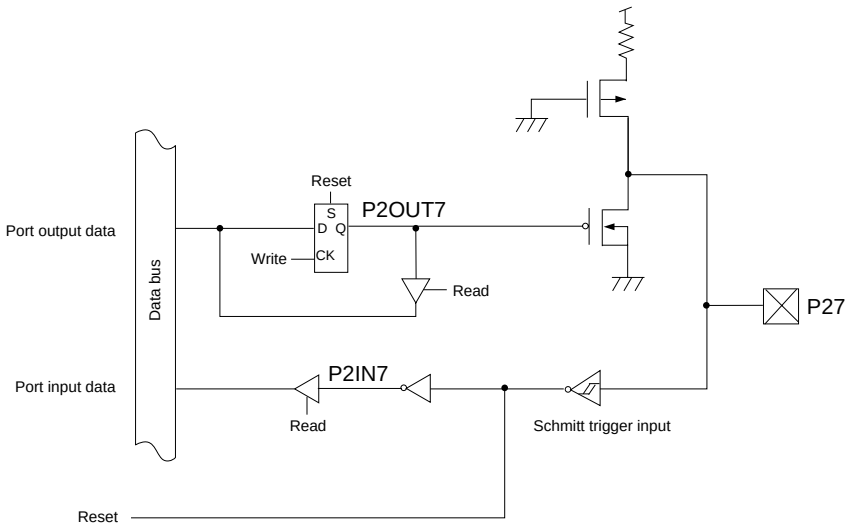


Figure 4-4-4 Block Diagram (P27)

4-5 Port 3

4-5-1 Description

■General Port Setup
Each bit can be set individually as either an input or output by the port 3 I/O direction control register (P3DIR). The control flag of the port 3 direction control register (P3DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 3 direction control register (P3DIR) to "0" and read the value of the port 3 input register (P3IN).

To output data to pin, set the control flag of the port 3 direction control register (P3DIR) to "1" and write data to the port 3 output register (P3OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 3 pull-up resistor control register (P3PLU). Set the control flag of the port 3 pull-up resistor control register (P3PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup
PB0 to PB3 can be used as the LCD common output pins (COM0 to COM3). Set "1" to bit 4 to 7 (COMSL0 to 3) of the LCD output control register 2 (LCCTR2) to use these ports.
When common output is selected, input mode is set and the pull-up resistors are set to "without pull-up resistor" automatically.

4-5-2 Registers

	7	6	5	4	3	2	1	0	
P3OUT	—	—	—	—	P3OUT3	P3OUT2	P3OUT1	P3OUT0	(At reset : - - - - X X X X)

P3OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 3 output register (P3OUT : x'03F13', R/W)

	7	6	5	4	3	2	1	0	
P3IN	—	—	—	—	P3IN3	P3IN2	P3IN1	P3IN0	(At reset : - - - - X X X X)

P3IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 3 input register (P3IN : x'03F23', R)

	7	6	5	4	3	2	1	0	
P3DIR	—	—	—	—	P3DIR3	P3DIR2	P3DIR1	P3DIR0	(At reset : - - - - 0 0 0 0)

P3DIR	I/O mode selection
0	Input mode
1	Output mode

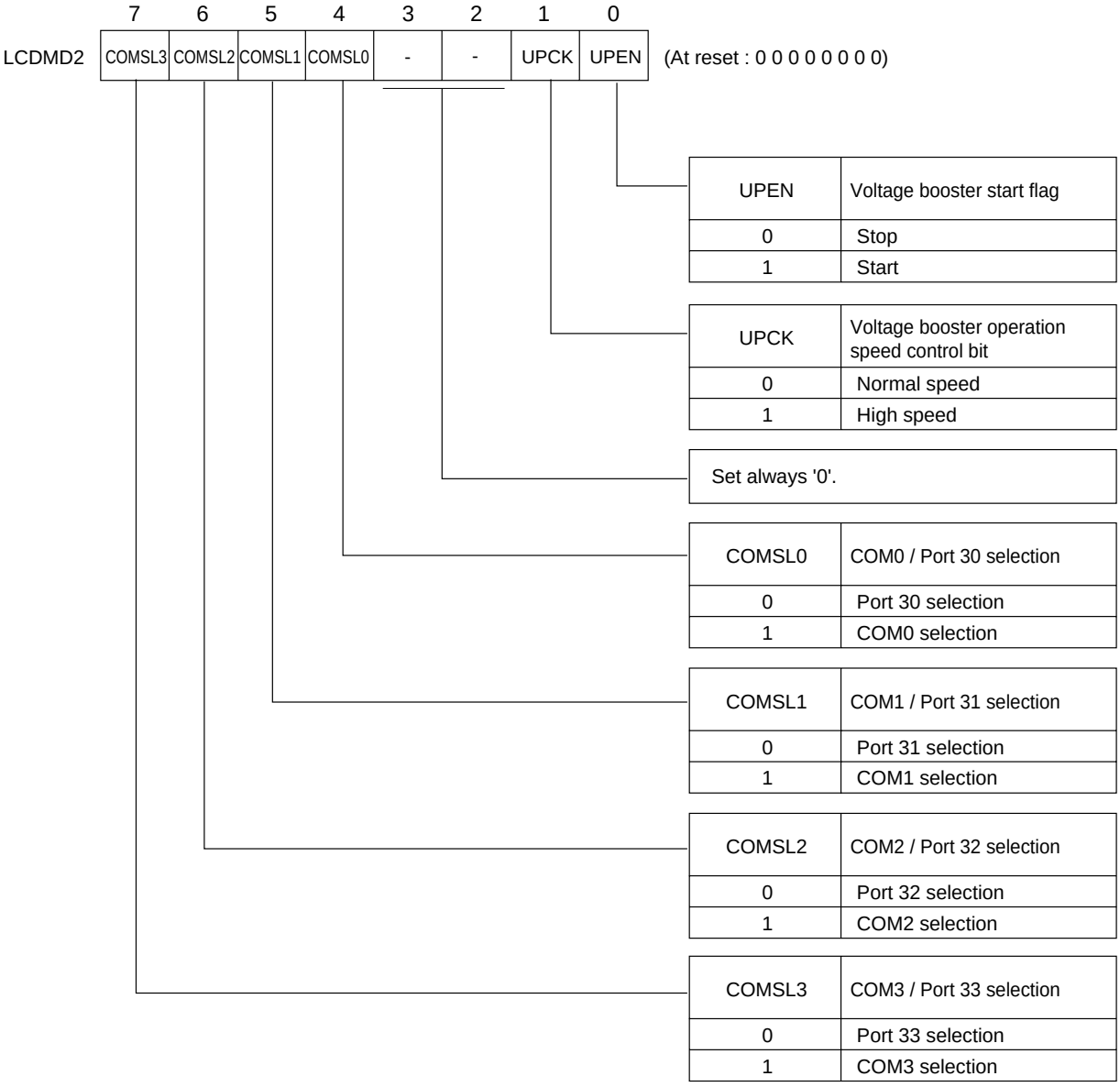
Port 3 direction control register (P3DIR : x'03F33', R/W)

	7	6	5	4	3	2	1	0	
P3PLU	—	—	—	—	P3PLU3	P3PLU2	P3PLU1	P3PLU0	(At reset : - - - - 0 0 0 0)

P3PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 3 pull-up resistor control register (P3PLU : x'03F43', R/W)

Figure 4-5-1 Port 3 Registers (1/2)


7 6 5 4 3 2 1 0
LCDMD2
COMSL3 COMSL2 COMSL1 COMSL0 - - UPCK UPEN
(At reset : 0 0 0 0 0 0 0 0)
UPEN | Voltage booster start flag
0 | Stop
1 | Start
UPCK | Voltage booster operation speed control bit
0 | Normal speed
1 | High speed
Set always '0'.
COMSL0 | COM0 / Port 30 selection
0 | Port 30 selection
1 | COM0 selection
COMSL1 | COM1 / Port 31 selection
0 | Port 31 selection
1 | COM1 selection
COMSL2 | COM2 / Port 32 selection
0 | Port 32 selection
1 | COM2 selection
COMSL3 | COM3 / Port 33 selection
0 | Port 33 selection
1 | COM3 selection

LCD mode control register 2 (LCDMD2 : X'03FDA', R/W)

Figure 4-5-2 Port 3 Registers (2/2)

4-5-3 Block Diagram

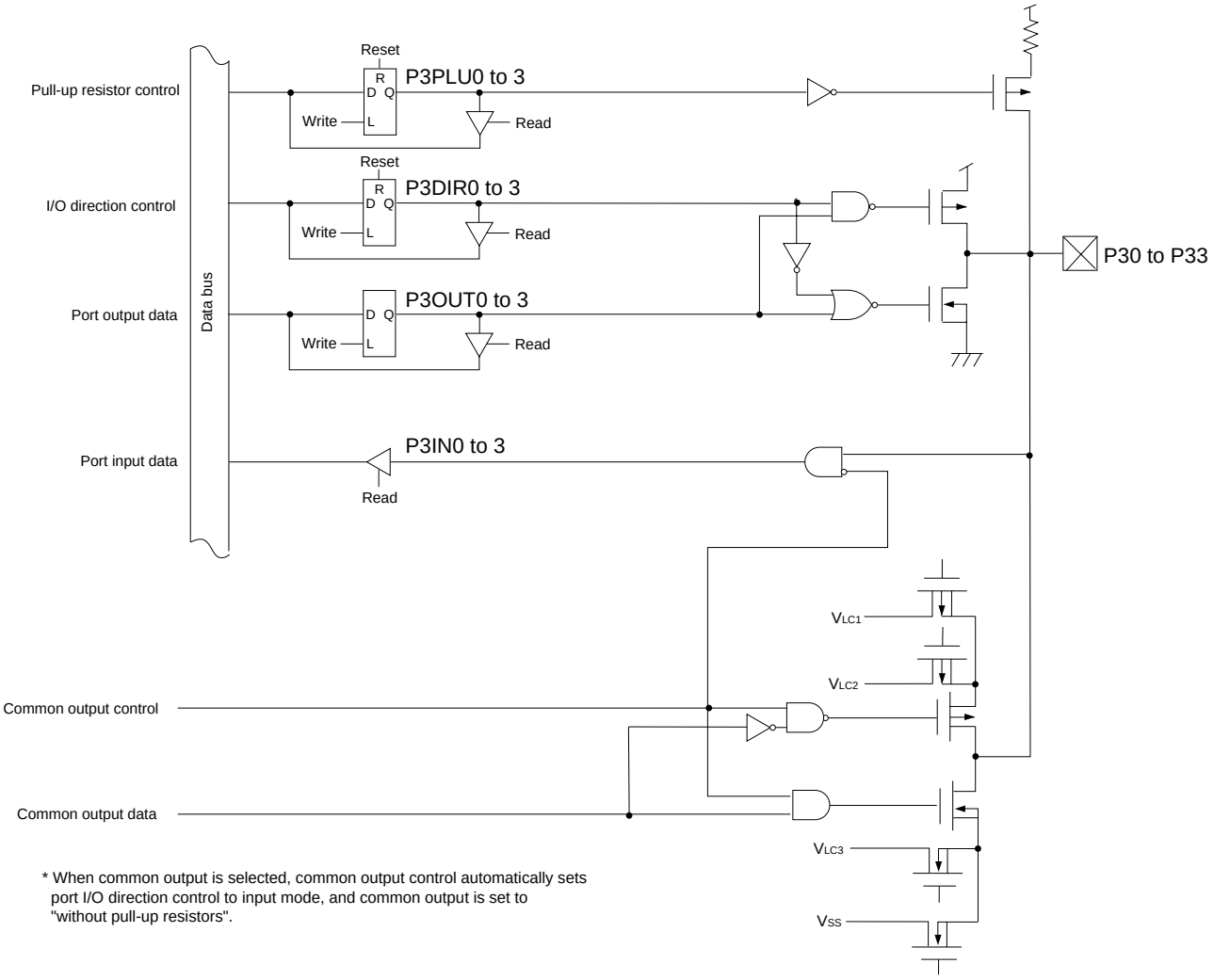


Figure 4-5-3 Block Diagram (P30 to P33)

4-6 Port 5

4-6-1 Description

■General Port Setup
Each bit can be set individually to either an input or output by the port 5 I/O direction control register (P5DIR). The control flag of the port 5 direction control register (P5DIR) is set to "1" for output mode, and "0" for input mode.

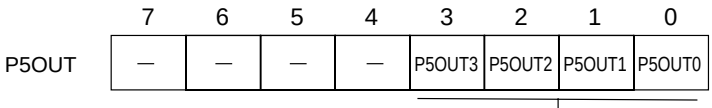
To read input data of pin, set the control flag of the port 5 direction control register (P5DIR) to "0" and read the value of the port 5 input register (P5IN).

To output data to pin, set the control flag of the port 5 direction control register (P5DIR) to "1" and write data to the port 5 output register (P5OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 5 pull-up resistor control register (P5PLU). Set the control flag of the port 5 pull-up resistor control register (P5PLU) to "1" to add pull-up resistor.

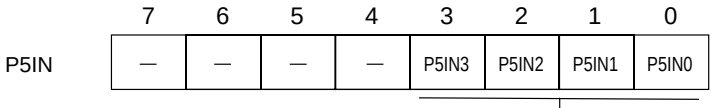
■Special Function Pin Setup
P50 to P53 are large current output pins and can be used as output pins of timer 0, timer 7, timer 2, and timer 8. The output mode for each pin can be selected with port 5 output mode register (P5OMD). When "1" is set to the port 5 output mode resister (P5OMD), each pin can be used as the timer output pin. When "0" is set to the port 5 output mode register (P5OMD), each pin can be used as the general purpose port pin.

4-6-2 Registers



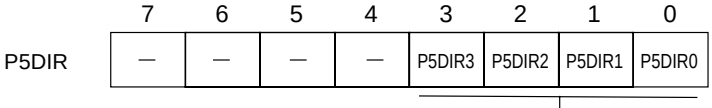
P5OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 5 output register (P5OUT : x'03F15', R/W)



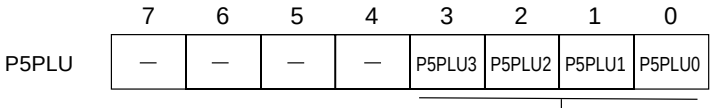
P5IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 5 input register (P5IN : x'03F25', R)



P5DIR	I/O mode selection
0	Input mode
1	Output mode

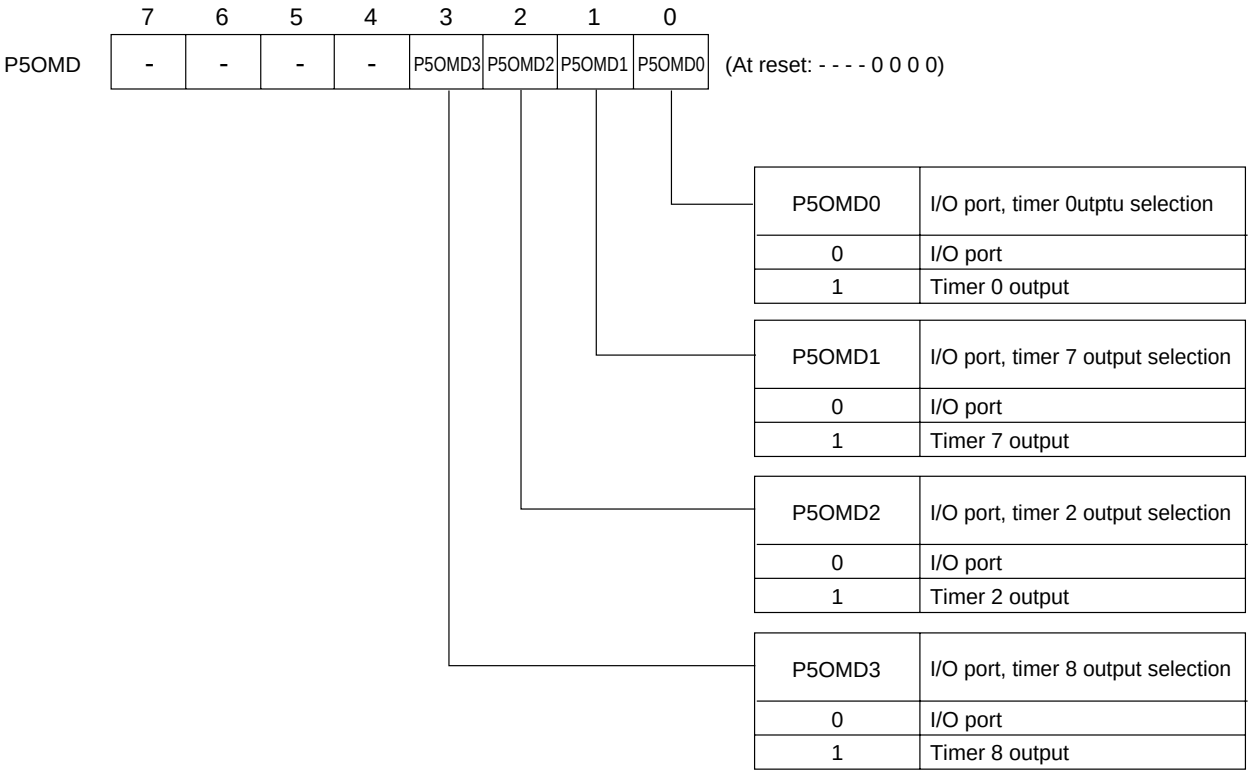
Port 5 direction control register (P5DIR : x'03F35', R/W)



P5PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 5 pull-up resistor control register (P5PLU : x'03F45', R/W)

Figure 4-6-1 Port 5 Registers (1/2)


7 6 5 4 3 2 1 0
P5OMD
- - - - P5OMD3 P5OMD2 P5OMD1 P5OMD0
(At reset: - - - - 0 0 0 0)
P5OMD0 I/O port, timer 0utptu selection
0 I/O port
1 Timer 0 output
P5OMD1 I/O port, timer 7 output selection
0 I/O port
1 Timer 7 output
P5OMD2 I/O port, timer 2 output selection
0 I/O port
1 Timer 2 output
P5OMD3 I/O port, timer 8 output selection
0 I/O port
1 Timer 8 output

Port 5 output mode register (P5OMD: X'03F3F', R/W)

Figure 4-6-2 Port 5 Registers (2/2)

4-6-3 Block Diagram

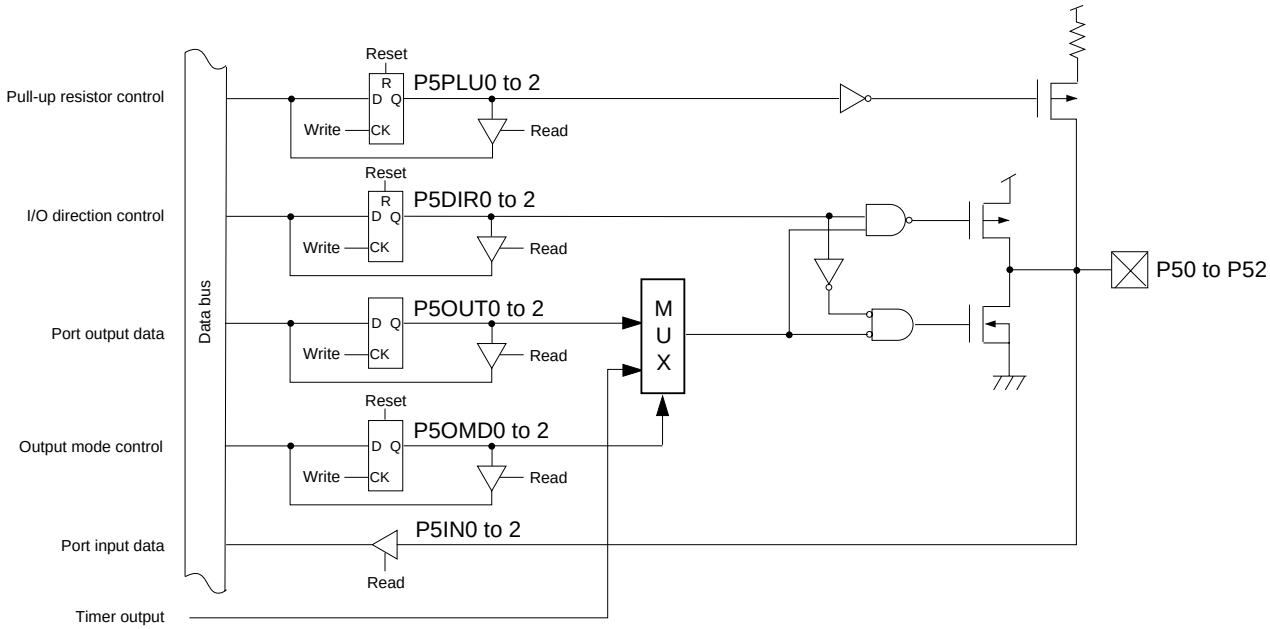


Figure 4-6-3 Block Diagram (P50 to P52)

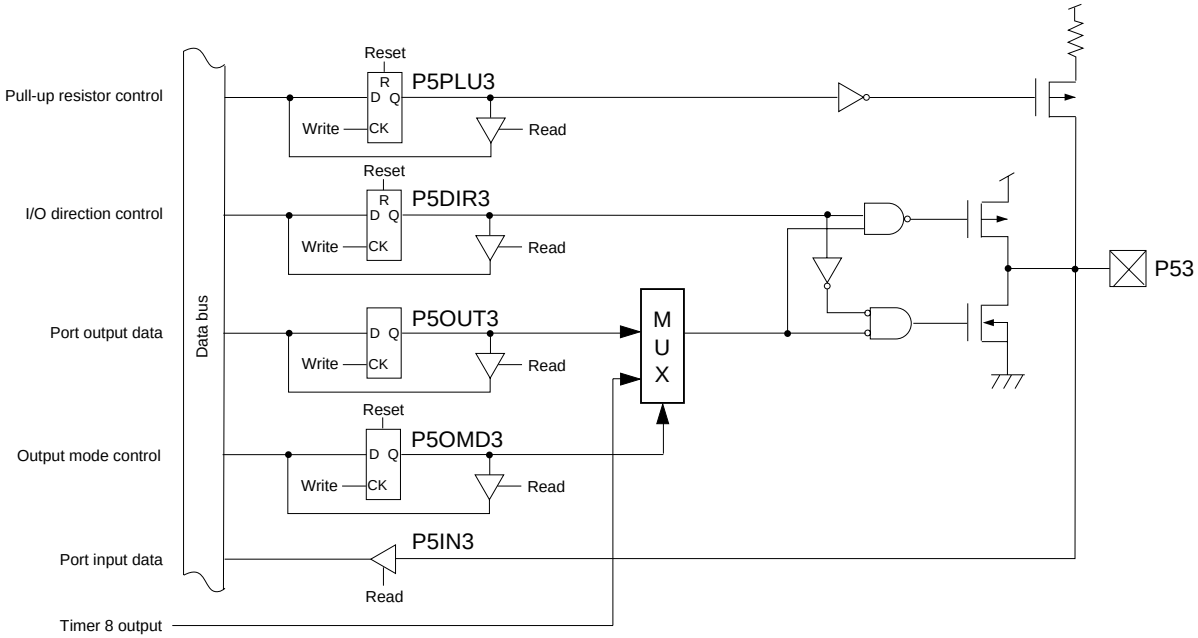


Figure 4-6-4 Block Diagram (P53)

4-7 Port 6

4-7-1 Description

■General port Setup
Each bit can be set individually to either an input or output by the port 6 I/O direction control register (P6DIR). The control flag of the port 6 direction control register (P6DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 6 direction control register (P6DIR) to "0" and read the value of the port 6 input register (P6IN).

To output data to pin, set the control flag of the port 6 direction control register (P6DIR) to "1" and write data to the port 6 output register (P6OUT).

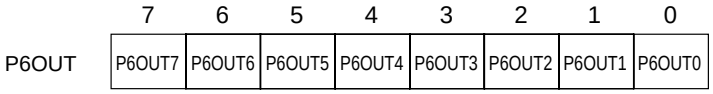
Each bit can be set individually if pull-up / pull-down resistor is added or not, by the port 6 pull-up / pull-down resistor control register (P6PLUD). Set the control flag of the port 6 pull-up / pull-down resistor control register (P6PLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp4 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup
P60 to P67 can be used as the LCD segment output pins, as well. To use these ports as SEG16 to SEG23 pins, set "1" to bit0 to 7 (LC2SL0 to LC2SL7) in the LCD output control register 2 (LCCTR2). The ports and the segments can be switched in 1-bit unit. When segment output is selected, input mode is set and the pull-up resistors are set to "without pull up resistors" automatically..

P60 to P67 are used as input pins for KEY interrupt, as well.
[☞ Chapter 3 3-3-6. Key Input Interrupt]
[☞ Chapter 3 3-3-2. Block Diagram, 3-3-3. Control Registers]

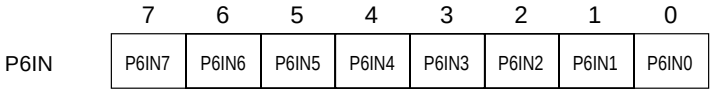
Each bit can be set individually to synchronous output by the port 6 synchronous output control register (P6SYO). The port 6 synchronous output control register (P6SYO) is set to "1" for synchronous output, and "0" for general port. The pin control register (FLOAT) can select the event that generates synchronous output. When the bp1, bp0 of the pin control register (FLOAT) is "00", the external interrupt 2 (IRQ2) is selected. And "01" for the timer 7 interrupt, "10" for the timer 2 interrupt, "11" for the timer 1 interrupt. For further detail, refer to 4-14. Synchronous output function [p.IV-43].

4-7-2 Registers



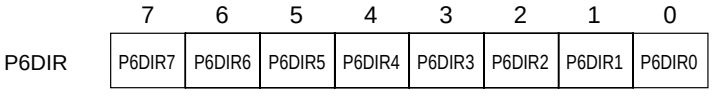
P6OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 6 output register (P6OUT : x'03F16', R/W)



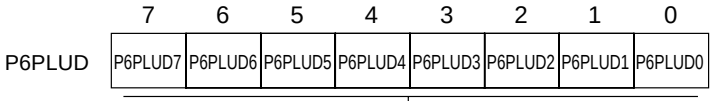
P6IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 6 intput register (P6IN : x'03F26', R)



P6DIR	I/O mode selection
0	Input mode
1	Output mode

Port 6 direction control register (P6DIR : x'03F36', R/W)



P6PLUD	Pull-up/pull-down resistor selection
0	No pull-up/pull-down resistor
1	Pull-up/pull-down resistor

Port 6 pull-up/pull-down resistor control register (P6PLUD : x'03F46', R/W)

Figure 4-7-1 Port 6 Registers (1/3)

	7	6	5	4	3	2	1	0	
P6SYO	P6SYO7	P6SYO6	P6SYO5	P6SYO4	P6SYO3	P6SYO2	P6SYO1	P6SYO0	(At reset : 0 0 0 0 0 0 0 0)

P6SYO	I/O port, synchronous output pin selection
0	I/O port (Disable synchronous output)
1	Synchronous output pin (Enable synchronous output)

Port 6 synchronous output control register (P6SYO : x'03F1E', R/W)

	7	6	5	4	3	2	1	0	
FLOAT	—	PARDWN	P7RDWN	P6RDWN	—	—	SYOEVS1	SYOEVS0	(At reset: - 0 0 0 - - 0 0)

SYOEVS1	SYOEVS0	P6 synchronous output event selection
0	0	External interrupt IRQ2
	1	Timer 7 interrupt
1	0	Timer 2 interrupt
	1	Timer 1 interrupt

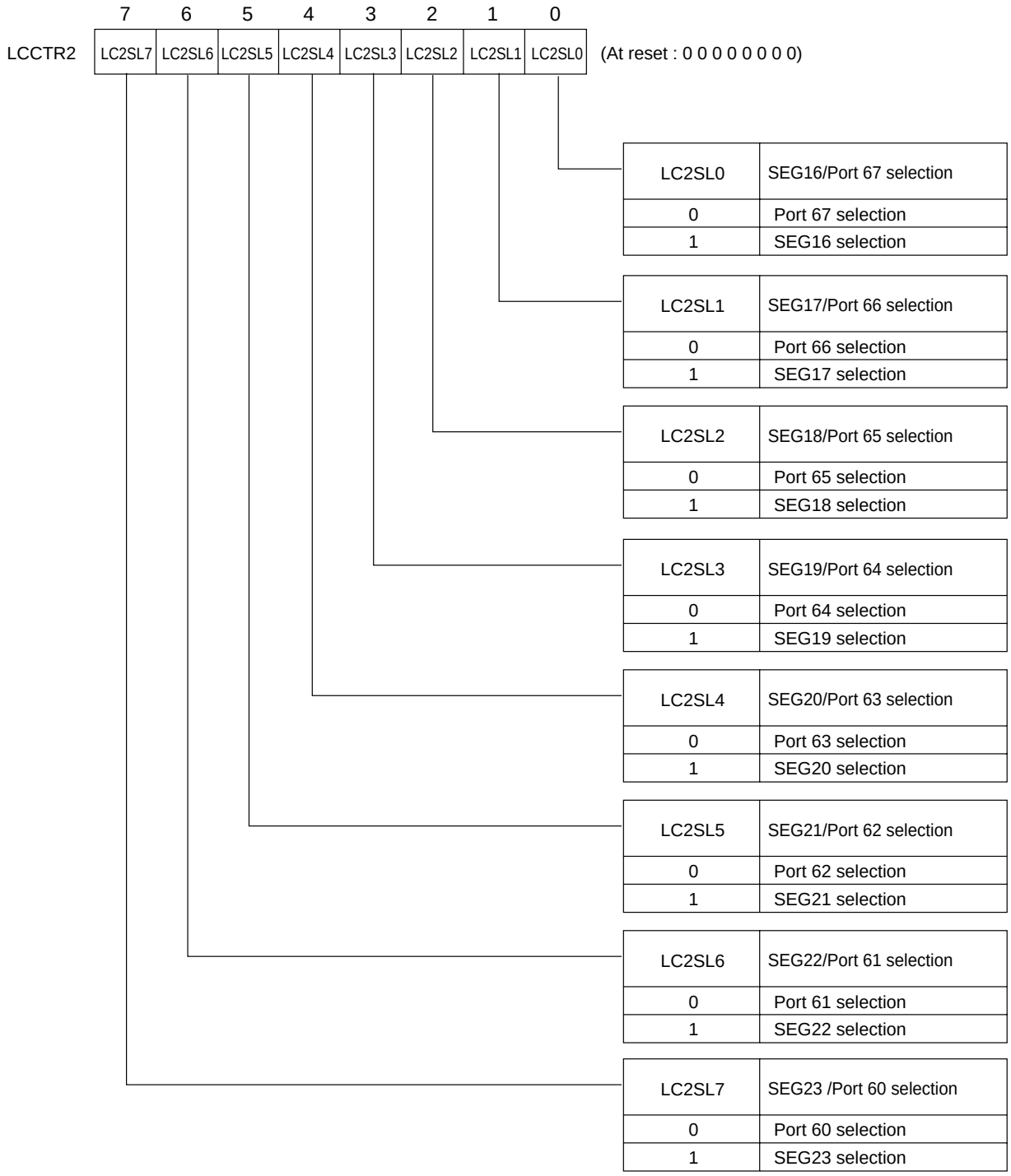
P6RDWN	P6 pull-up/pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

P7RDWN	P7 pull-up/pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	PA pull-up/pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

Pull-up/Pull-down resistor selection, Pin control register (FLOAT: X'03F2E', R/W)

Figure 4-7-2 Port 6 Registers (2/3)


7 6 5 4 3 2 1 0
LCCTR2
LC2SL7 LC2SL6 LC2SL5 LC2SL4 LC2SL3 LC2SL2 LC2SL1 LC2SL0
(At reset : 0 0 0 0 0 0 0 0)
LC2SL0 SEG16/Port 67 selection
0 Port 67 selection
1 SEG16 selection
LC2SL1 SEG17/Port 66 selection
0 Port 66 selection
1 SEG17 selection
LC2SL2 SEG18/Port 65 selection
0 Port 65 selection
1 SEG18 selection
LC2SL3 SEG19/Port 64 selection
0 Port 64 selection
1 SEG19 selection
LC2SL4 SEG20/Port 63 selection
0 Port 63 selection
1 SEG20 selection
LC2SL5 SEG21/Port 62 selection
0 Port 62 selection
1 SEG21 selection
LC2SL6 SEG22/Port 61 selection
0 Port 61 selection
1 SEG22 selection
LC2SL7 SEG23 /Port 60 selection
0 Port 60 selection
1 SEG23 selection

LCD output control register 2 (LCCTR2: X'03FDC', R/W)

Figure 4-7-3 Port 6 Registers (3/3)

4-7-3 Block Diagram

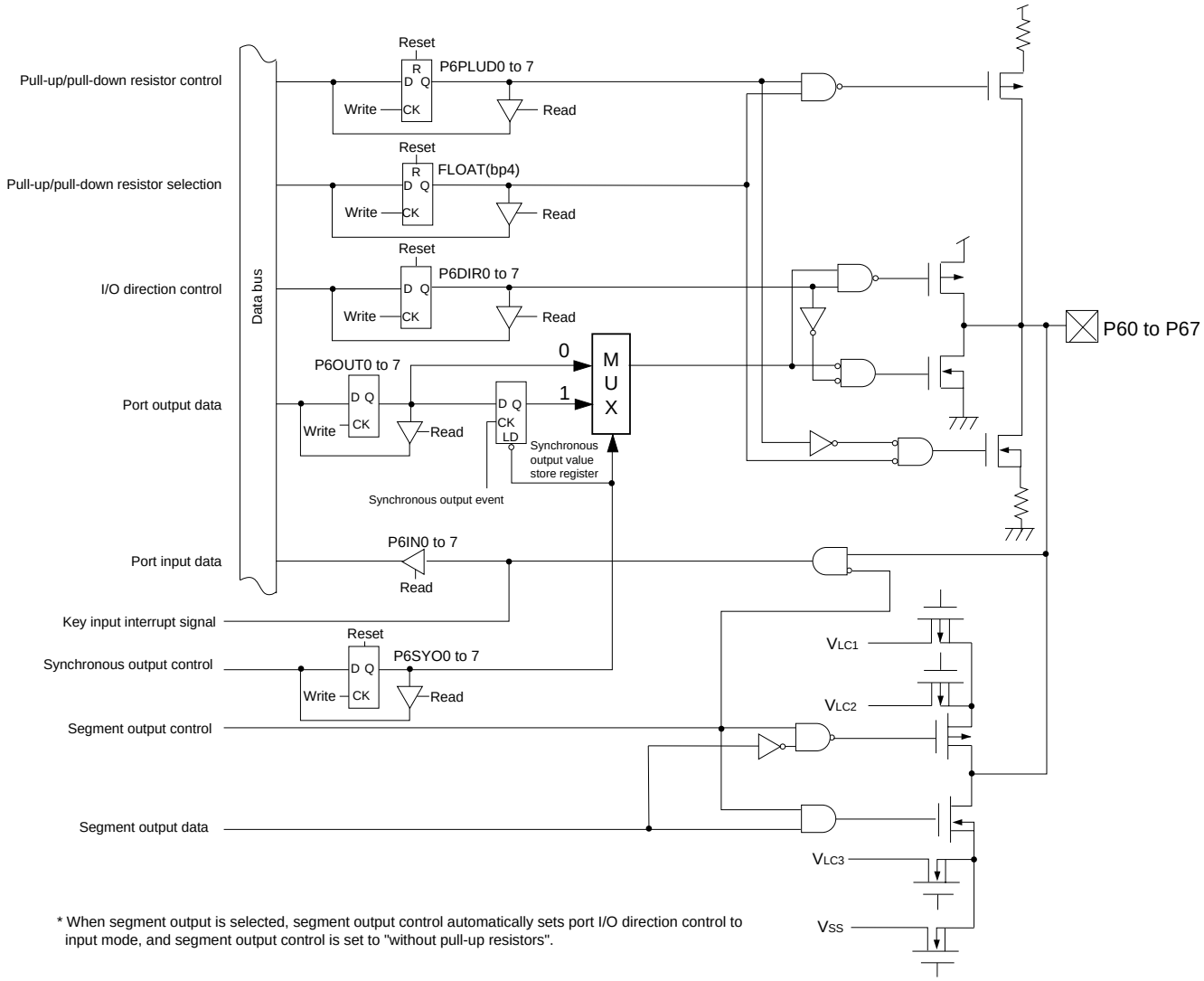


Figure 4-7-4 Block Diagram (P60 to P67)

4-8 Port 7

4-8-1 Description

■General Port Setup
Each bit can be set individually to either an input or output by the port 7 I/O direction control register (P7DIR). The control flag of the port 5 direction control register (P7DIR) is set to "1" for output mode, and "0" for input mode.

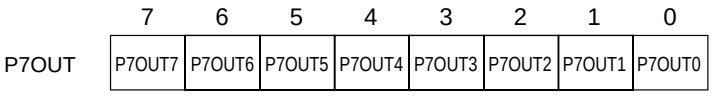
To read input data of pin, set the control flag of the port 7 direction control register (P7DIR) to "0" and read the value of the port 7 input register (P7IN).

To output data to pin, set the control flag of the port 7 direction control register (P7DIR) to "1" and write data to the port 7 output register (P7OUT).

Each bit can be set individually if pull-up / pull-down resistor is added or not, by the port 7 pull-up / pull-down resistor control register (P7PLUD). Set the control flag of the port 7 pull-up / pull-down resistor control register (P7PLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp5 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

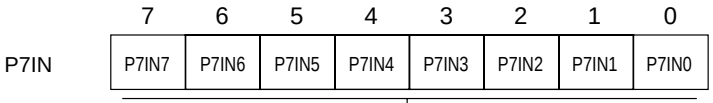
■Special Function Pin Setup
P70 to P77 can be used as the LCD segment output pins, as well. When used as SEG8 to SEG15 pins, set "1" of bit 4 to 7 (LC2SL4 to LC2SL7) in the LCD output control register 1 (LCCTR1). The ports and the segments can be switched by 2-bits. When segment output is selected, input mode is set and the pull-up resistors are set to "without pull up resistors" automatically.

4-8-2 Registers



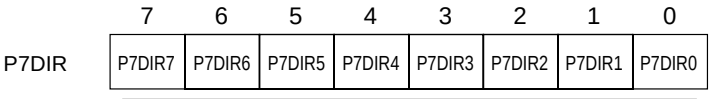
P7OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 7 output register (P7OUT : x'03F17', R/W)



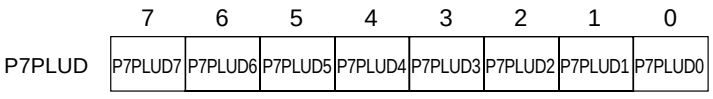
P7IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 7 input register (P7IN : x'03F27', R)



P7DIR	I/O mode selection
0	Input mode
1	Output mode

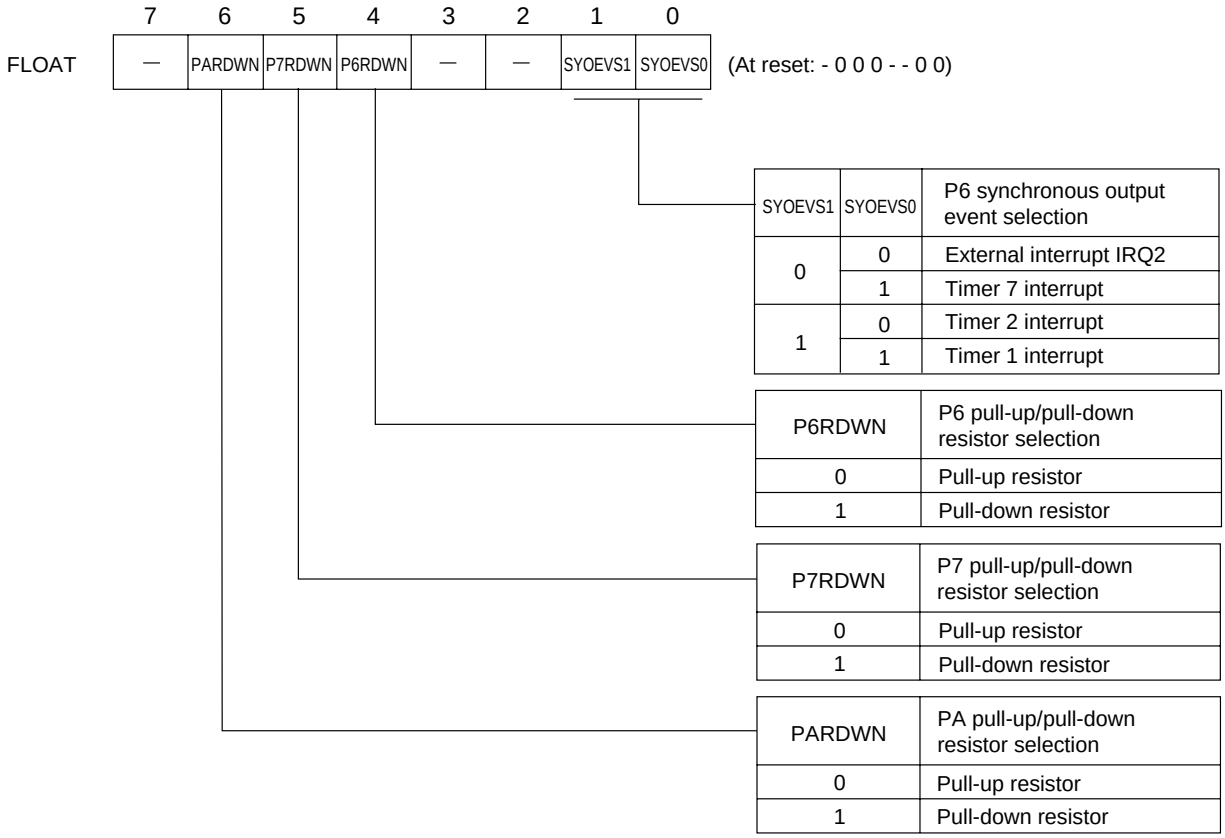
Port 7 direction control register (P7DIR : x'03F37', R/W)



P7PLUD	Pull-up/pull-down resistor selection
0	No pull-up/pull-down resistor
1	Pull-up/pull-down resistor

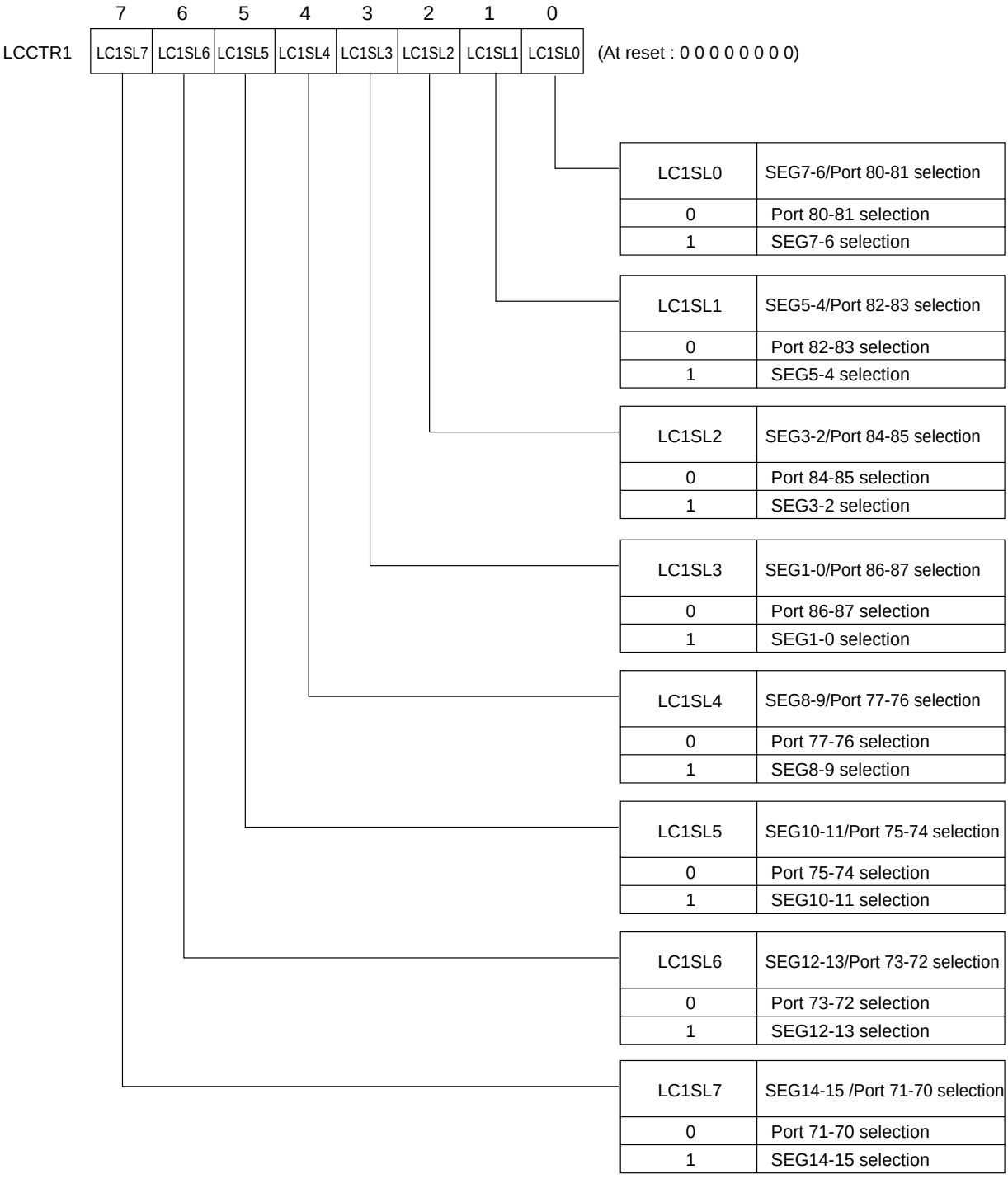
Port 7 pull-up/pull-down resistor control register (P7PLUD : x'03F47', R/W)

Figure 4-8-1 Port 7 Registers (1/3)



Pull-up/Pull-down resistor selection, Pin control register (FLOAT: X'03F2E', R/W)

Figure 4-8-2 Port 7 Registers (2/3)


7 6 5 4 3 2 1 0
LCCTR1
LC1SL7 LC1SL6 LC1SL5 LC1SL4 LC1SL3 LC1SL2 LC1SL1 LC1SL0
(At reset : 0 0 0 0 0 0 0 0)
LC1SL0 SEG7-6/Port 80-81 selection
0 Port 80-81 selection
1 SEG7-6 selection
LC1SL1 SEG5-4/Port 82-83 selection
0 Port 82-83 selection
1 SEG5-4 selection
LC1SL2 SEG3-2/Port 84-85 selection
0 Port 84-85 selection
1 SEG3-2 selection
LC1SL3 SEG1-0/Port 86-87 selection
0 Port 86-87 selection
1 SEG1-0 selection
LC1SL4 SEG8-9/Port 77-76 selection
0 Port 77-76 selection
1 SEG8-9 selection
LC1SL5 SEG10-11/Port 75-74 selection
0 Port 75-74 selection
1 SEG10-11 selection
LC1SL6 SEG12-13/Port 73-72 selection
0 Port 73-72 selection
1 SEG12-13 selection
LC1SL7 SEG14-15 /Port 71-70 selection
0 Port 71-70 selection
1 SEG14-15 selection

LCD output control register 1 (LCCTR1 : X'03FDB', R/W)

Figure 4-8-3 Port 7 Registers (3/3)

4-8-3 Block Diagram

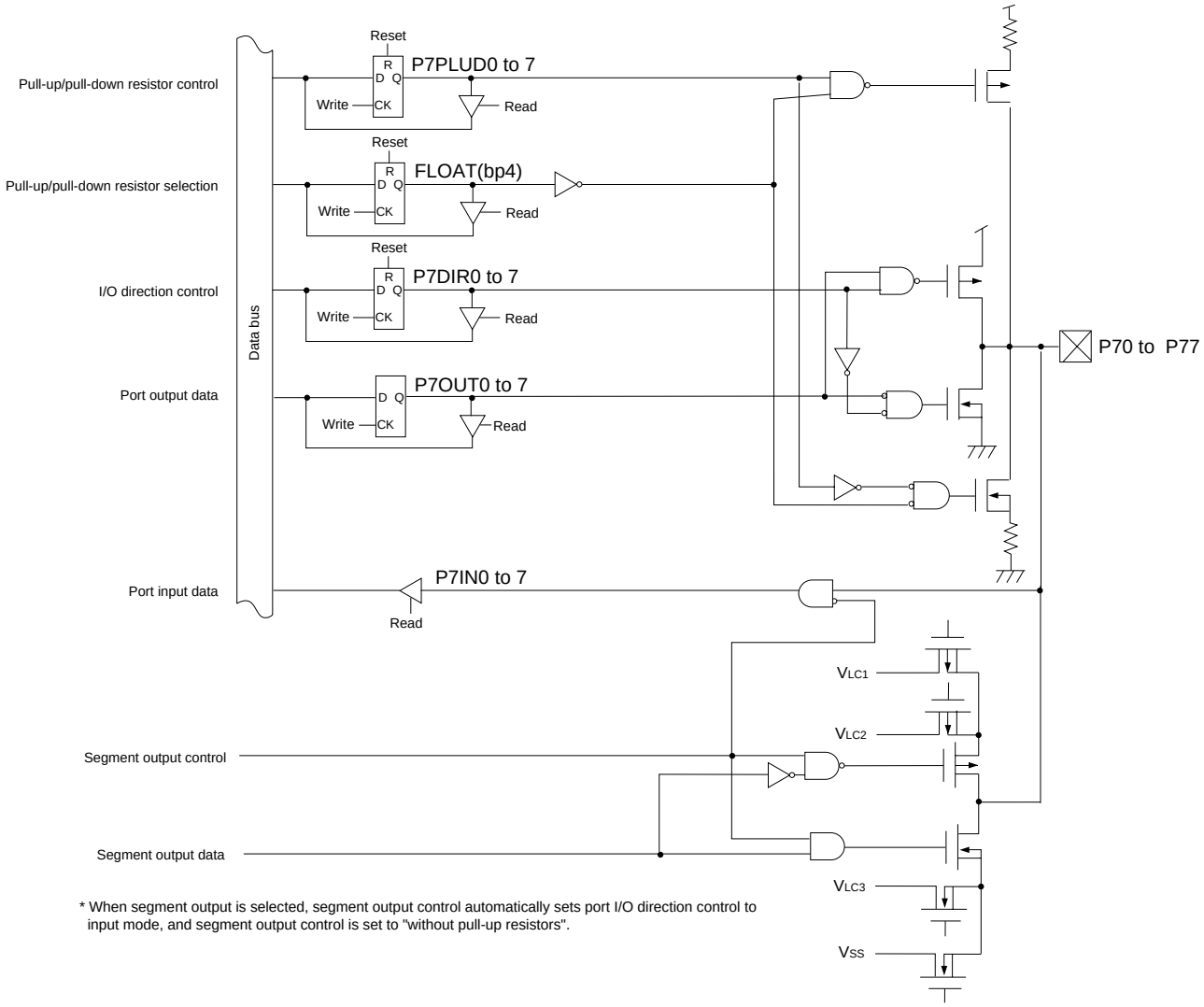


Figure 4-8-4 Block Diagram (P70 to P77)

4-9 Port 8

4-9-1 Description

■General Port Setup

Each bit can be set individually to either an input or output by the port 8 control I/O direction register (P8DIR). The control flag of the port 8 direction control register (P8DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 8 direction control register (P8DIR) to "0" and read the value of the port 8 input register (P8IN).

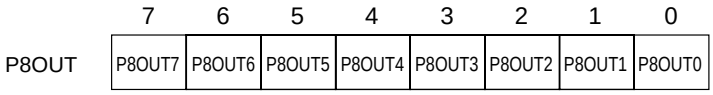
To output data to pin, set the control flag of the port 8 direction control register (P8DIR) to "1" and write data to the port 8 output register (P8OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

■ Special Function Pin Setup

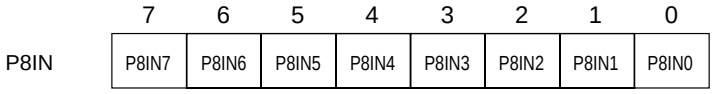
P80 to P87 can be used as the LCD segment output pins. To use these ports as SEG0 to SEG7 pins, set "1" to bit 0 to 3 (LC1SL0 to LC1SL3) in the LCD output control register 1 (LCCTR1). The ports and the segments can be switched in 2 bits unit. When segment output is selected, input mode is set and the pull-up resistors are set to "without pull-up resistors" automatically.

4-9-2 Registers



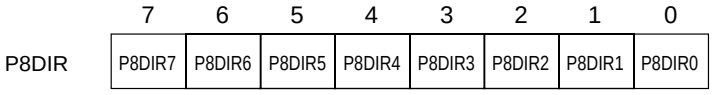
P8OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 8 output register (P8OUT : x'03F18', R/W)



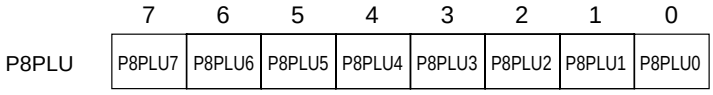
P8IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 8 input register (P8IN : x'03F28', R)



P8DIR	I/O mode selection
0	Input mode
1	Output mode

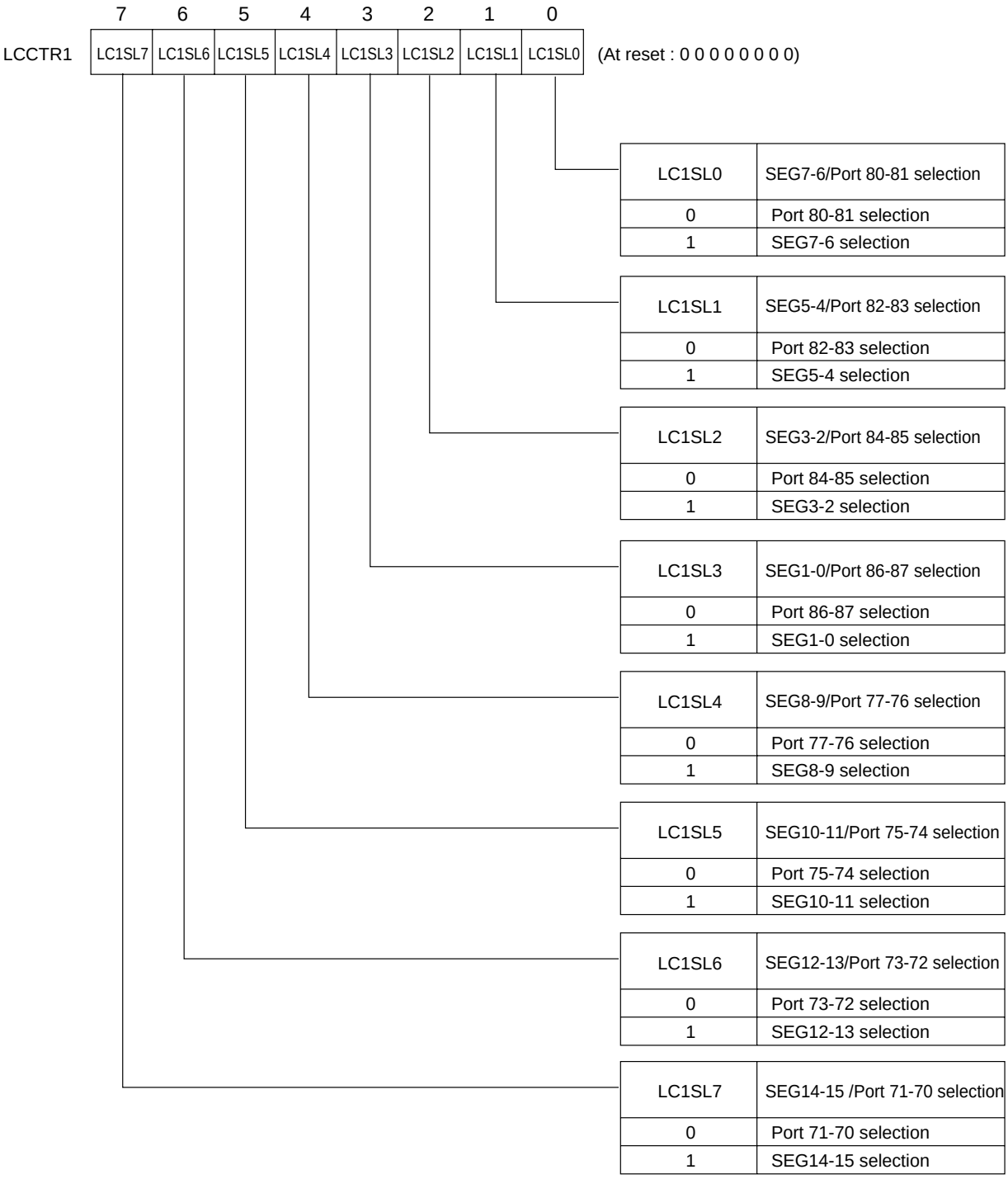
Port 8 direction control register (P8DIR : x'03F38', R/W)



P8PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 8 pull-up resistor control register (P8PLU : x'03F48', R/W)

Figure 4-9-1 Port 8 Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR1
LC1SL7 LC1SL6 LC1SL5 LC1SL4 LC1SL3 LC1SL2 LC1SL1 LC1SL0
(At reset : 0 0 0 0 0 0 0 0)
LC1SL0 SEG7-6/Port 80-81 selection
0 Port 80-81 selection
1 SEG7-6 selection
LC1SL1 SEG5-4/Port 82-83 selection
0 Port 82-83 selection
1 SEG5-4 selection
LC1SL2 SEG3-2/Port 84-85 selection
0 Port 84-85 selection
1 SEG3-2 selection
LC1SL3 SEG1-0/Port 86-87 selection
0 Port 86-87 selection
1 SEG1-0 selection
LC1SL4 SEG8-9/Port 77-76 selection
0 Port 77-76 selection
1 SEG8-9 selection
LC1SL5 SEG10-11/Port 75-74 selection
0 Port 75-74 selection
1 SEG10-11 selection
LC1SL6 SEG12-13/Port 73-72 selection
0 Port 73-72 selection
1 SEG12-13 selection
LC1SL7 SEG14-15 /Port 71-70 selection
0 Port 71-70 selection
1 SEG14-15 selection

LCD output control register 1 (LCCTR1 : X'03FDB', R/W)

Figure 4-9-2 Port 8 Registers (2/2)

4-9-3 Block Diagram

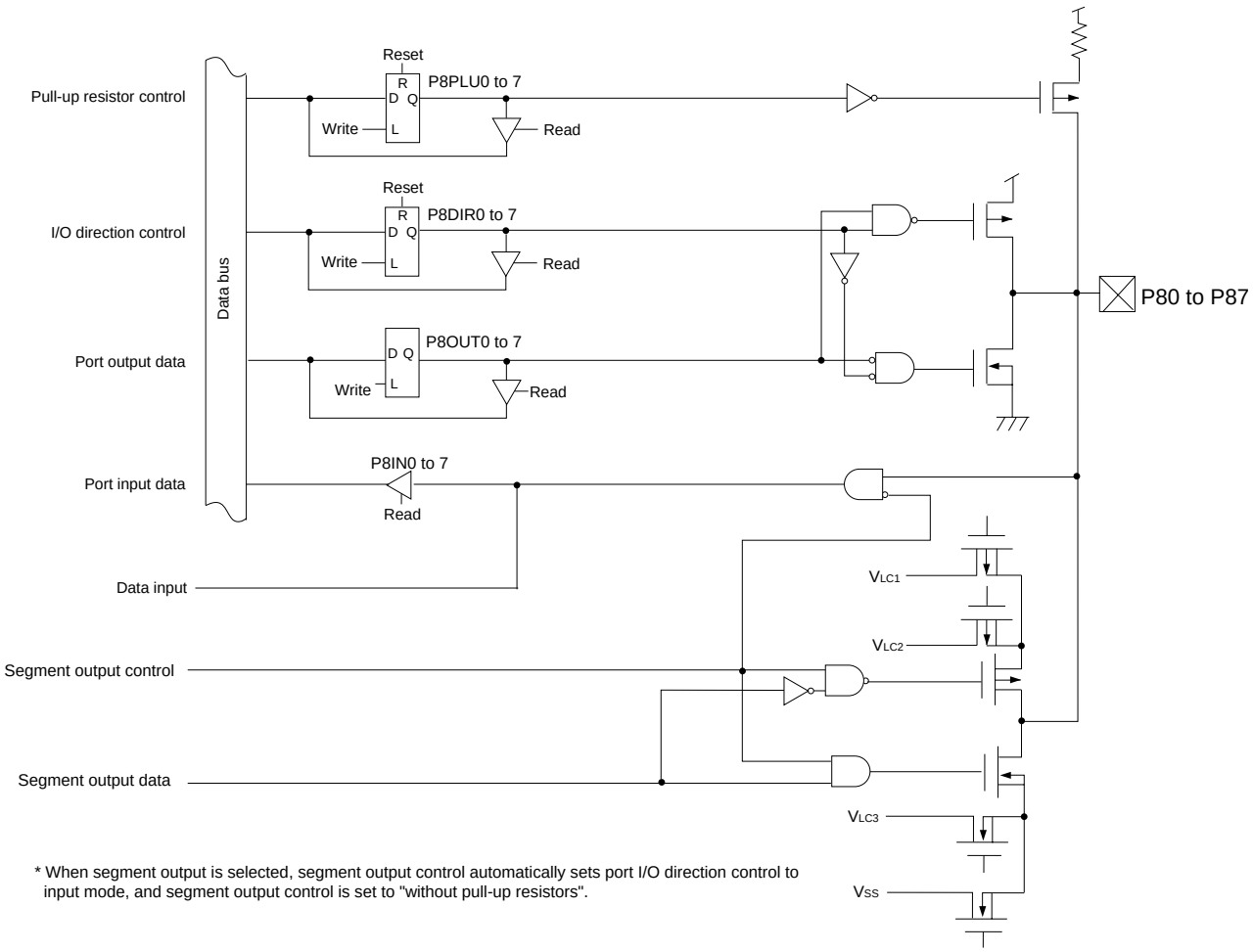


Figure 4-9-3 Block Diagram (P80 to P87)

4-10 Port A

4-10-1 Description

■General Port Setup

All bits of port A are for input only. To read input data of pin, read out the value of the port A input register (PAIN).

Each bit can be set individually if pull-up / pull-down resistor is added or not, by the port A pull-up / pull-down resistor control register (PAPLUD). Set the control flag of the port A pull-up / pull-down resistor control register (PAPLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp6 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup

PA0 to PA3 are used as input pins for analog. Each bit can be set individually as an input by the port A input mode register (PAIMD). When they are used as analog input pins, set the port A input mode register (PAIMD) to "1". Then, the value of the port A input register (PAIN) is read to be "1".

By setting the control flag of the PAIMD register to "1", the through current is not occurred when an analog voltage is set to pin,

4-10-2 Registers

	7	6	5	4	3	2	1	0	
PAIN	—	—	—	—	PAIN3	PAIN2	PAIN1	PAIN0	(At reset: - - - - X X X X)

PAIN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port A input register (PAIN: X'03F2A', R)

	7	6	5	4	3	2	1	0	
PAIMD	—	—	—	—	PAIMD3	PAIMD2	PAIMD1	PAIMD0	(At reset: - - - - 0 0 0 0)

PAIMD	I/O port, analog n input pin selection
0	I/O port
1	Analog n input pin

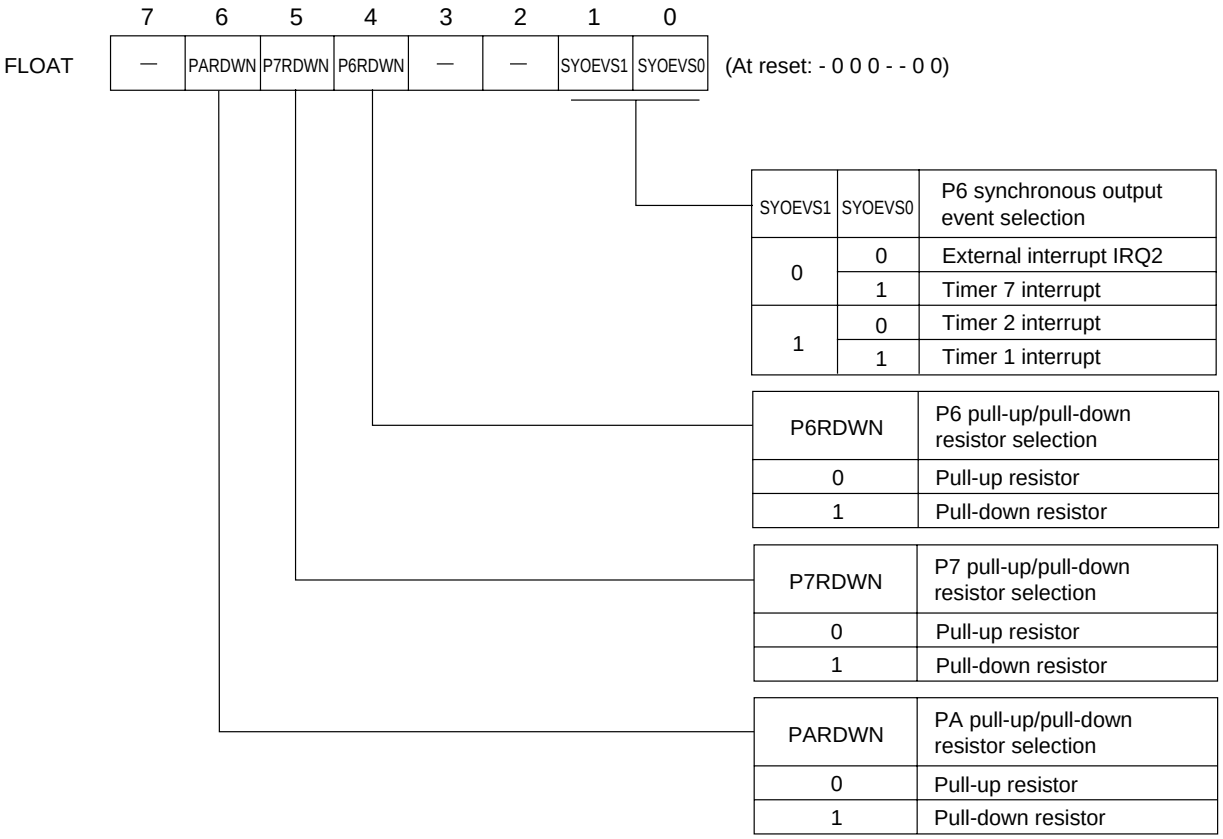
Port A input control register (PAIMD: X'03F3A', R/W)

	7	6	5	4	3	2	1	0	
PAPLUD	—	—	—	—	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	(At reset: - - - - 0 0 0 0)

PAPLUD	Pull-up/pull-down resistor selection
0	No pull-up/pull-down resistor
1	Pull-up/pull-down resistor

Port A pull-up/pull-down resistor control register (PAPLUD: X'03F4A', R/W)

Figure 4-10-1 Port A Registers (1/2)



Pull-up/Pull-down resistor selection, Pin control register (FLOAT: X'03F2E', R/W)

Figure 4-10-2 Port A Registers (2/2)

4-10-3 Block Diagram

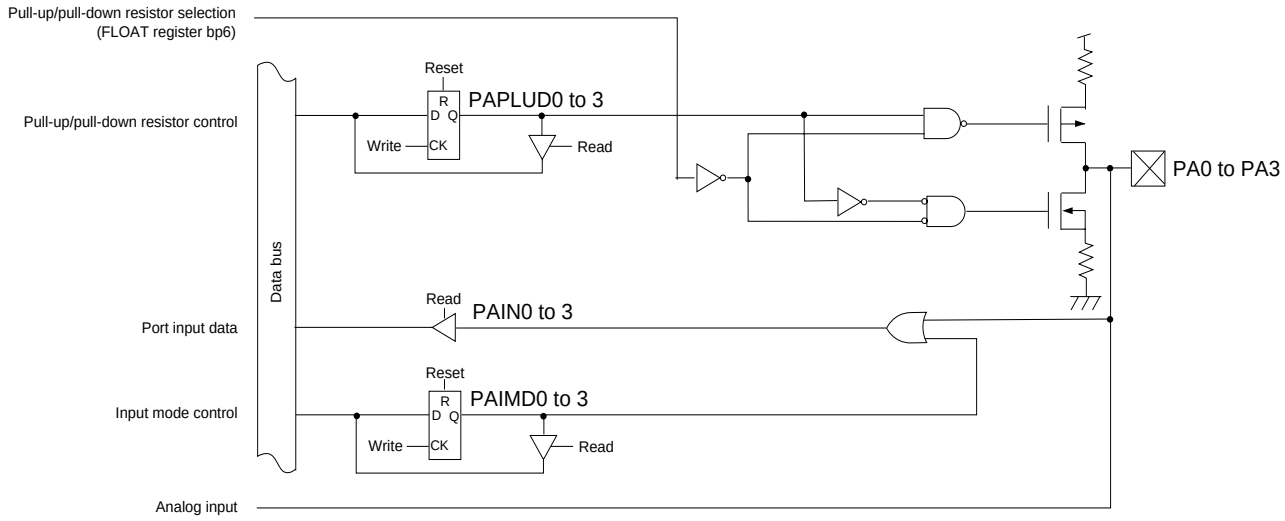


Figure 4-10-3 Block Diagram (PA0 to PA3)

4-11 Synchronous output (Port 6)

Port 6 has the synchronous output function that outputs the arbitrary set data to pins, in synchronization with the generation of the specified event, without setting program. Synchronous event is selected from the external interrupt 2 (P22/IRQ2), timer 1 interrupt, timer 2 interrupt or timer 7 interrupt signal.

4-11-1 Block Diagram

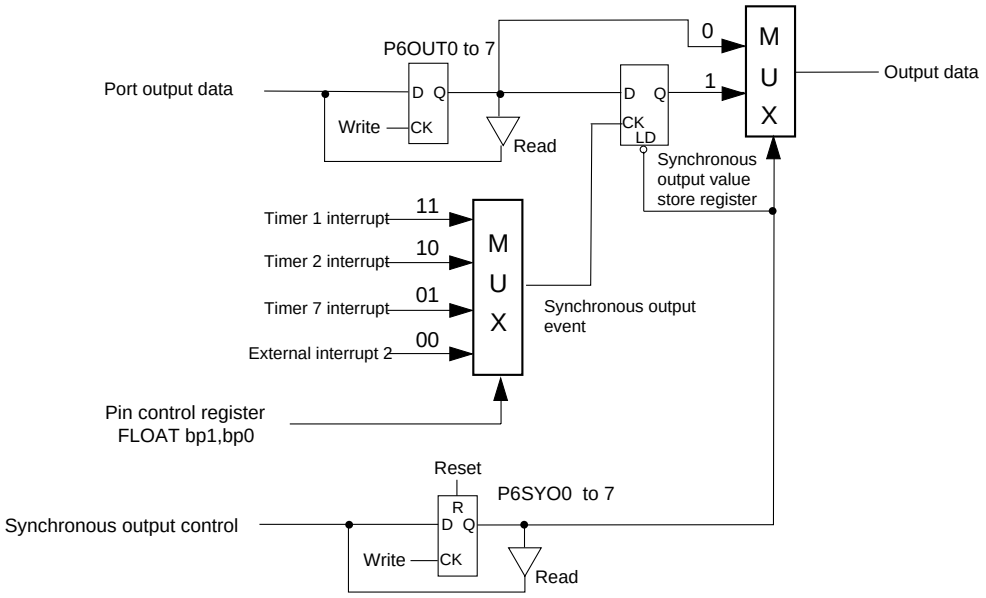


Figure 4-11-1 Synchronous Output Control Block Diagram

4-11-2 Registers

Table 4-11-1 shows the synchronous output control registers of port 6.

Table 4-11-1 Synchronous Output Control Registers

	Register	Address	R/W	Function	Page
Port 6	FLOAT	x'03F2E'	R/W	Pin control register 1	IV - 27
	P6SYO	x'03F1E'	R/W	Synchronous output control register	IV - 27
	P6DIR	x'03F36'	R/W	Port 6 direction control register	IV - 26
	P6PLUD	x'03F46'	R/W	Port 6 pull-up/pull-down resistor control register	IV - 26
	P6OUT	x'03F16'	R/W	Port 6 output register	IV - 26

4-11-3 Operation

■Synchronous Output Setup

The synchronous output control register (P6SYO) selects the synchronous output pin of the port 6, in each bit.

The synchronous output event is selected by the pin control register (FLOAT).

Table 4-11-2 Synchronous Output Event

	Specify to	Page
Synchronous output port	Port 6	Ⅳ - 27
Output event	External interrupt 2 (IRQ2)	Ⅲ - 19, 35
	Timer 1	Ⅵ - 32
	Timer 2	Ⅵ - 32
	Timer7	Ⅶ - 35

When the external interrupt 2 (IRQ2) is selected, the interrupt edge should be specified. The interrupt edge can be specified by the external interrupt 2 control register (IRQ2ICR) or the both edges interrupt control register (EDGDT). The synchronous output recognizes the generation of the specified edge as an event.

■Synchronous Output Operation

When the synchronous output control register (P6SYO) is set to disable the synchronous output (I/O port), the port 6 is functioned as a general port. When the port 6 is set to disable the synchronous output, the same value to the port 6 output register (P6OUT) is always loaded to the synchronous output value stored register. [☞ Figure 4-11-1. Synchronous Output Control Block Diagram]

After the output mode is selected by the port 6 direction control register (P6DIR), if the synchronous output is enabled by the synchronous output control register (P6SYO), the value of the synchronous output value stored register is output from pins. If the synchronous output event that is set by the pin control register (FLOAT) is never generated, the synchronous output value stored register holds the same value when the synchronous output event is enabled.

Store the value that should be output from pin after the synchronous output event is generated, to the port 6 output register (P6OUT). Once the synchronous output event that is set by the pin control register (FLOAT) is generated, the data of the synchronous output value stored register is switched to the data of the port 6 output register (P6OUT), and the output value from pin is changed.

Before the synchronous output is enabled by the synchronous output control register (P6SYO), set the initial value of the synchronous output to the port 6 output register (P6OUT), in advance.

■Port 6 Synchronous Output (External interrupt 2 IRQ2))

The synchronous output timing when the synchronous output event is set at the falling edge of the external interrupt 2, is shown below. The latched data on port 6 is output in synchronization with the falling edge of the IRQ2.

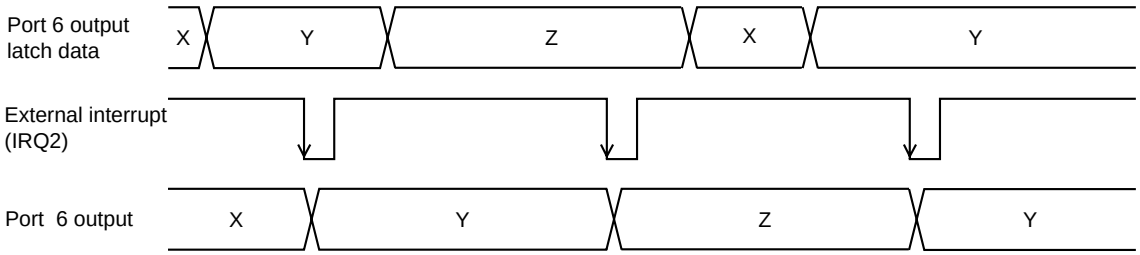


Figure 4-11-2 Synchronous Output Timing by Event Generation (IRQ2)

■Port 6 Synchronous Output (Timer 1, Timer 2, Timer 7)

The timer interrupt flag TMnIRQ is generated when the set values of binary counter and compare register are matched. The latched data on port 6 is output from the port 6 in synchronization with the rising edge of the TMnIRQ. About the setting of each timer operation, refer to chapter 6. 8-bit timers, and chapter 7. 16-bit timers.

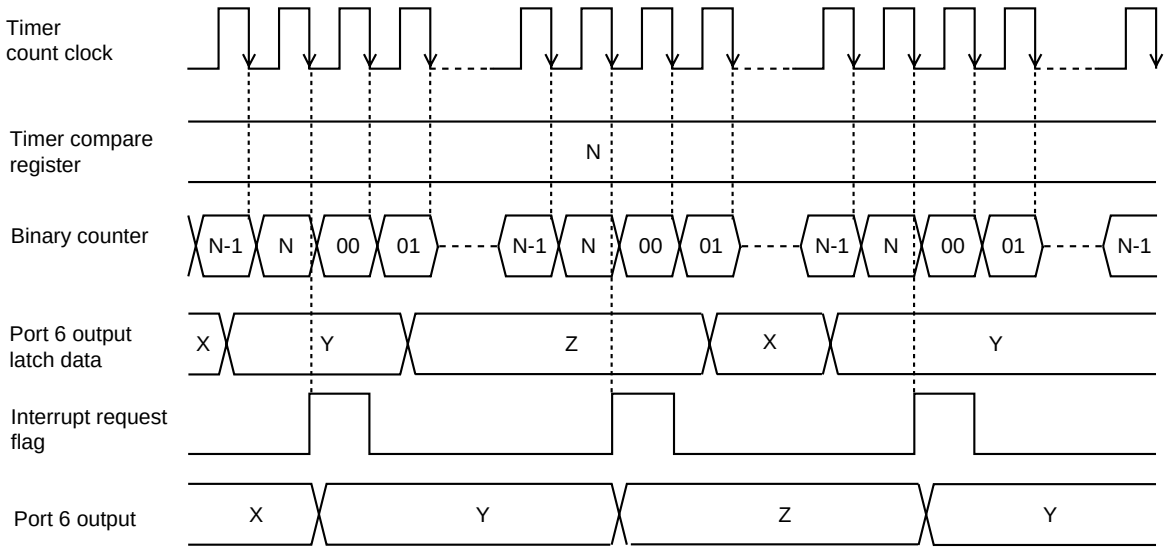


Figure 4-11-3 Synchronous Output Timing by Event Generation (Timers 1, 2 and 7)

4-11-4 Setup Example

A setup example of the port 6 synchronous output by the external interrupt 2 (IRQ2) is shown as follows. As it is operated, the initial output data of port 6 is "55", the synchronous output data is "AA", and the rising edge of the IRQ2 is selected at the synchronous event.

An example setup procedure, with description of each step is shown below.

Setup Procedure	Description
(1) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 00	(1) Set the SYOEVS1-0 flag of the FLOAT register to "00" to set the synchronous output event to the IRQ2.
(2) Specify the interrupt edge. IRQ2ICR(x'3FE4') bp5 : REDG2 = 1 EDGDT(x'3F8F') bp2 : EDGSEL2 = 0	(2) Set the REDG flag of the IRQ2ICR register to "1" to set the active edge of the IRQ2 at the rising edge. Set the EDGSEL2 flag of the EDGDT register "0" to select the programmable active edge interrupt.
(3) Set the initial output data. P6OUT(x'3F16') bp7-0 : P6OUT7-0 = x'55'	(3) Set the initial output data "55" to the P6OUT register. Port 6 outputs "55".
(4) Set the synchronous output pin. P6SYO(x'3F1E') bp7-0 : P6SYO7-0 = x'FF' P6DIR(x'3F36') bp7-0 : P6DIR7-0 = x'FF'	(4) Set port 6 to synchronous output pin by setting the P6SYO7-0 flag of the P6SYO register to "FF". Select the output mode by setting the P6DIR7-0 flag of the P6DIR register to "FF".
(5) Set the synchronous output data. P6OUT(x'3F16') bp7-0 : P6OUT7-0 = x'AA'	(5) Set the synchronous output data "AA" to the P6OUT register.
(6) Event is generated. Rising edge is generated at P22.	(6) Port 6 outputs "AA" at the rising edge of IRQ2.

Chapter 5 Prescaler

5

5-1 Overview

This LSI contains 2 prescalers that are used among the peripheral functions simultaneously. Each prescaler counts with fosc or fs as a base clock. The hardware is as follows ;

Prescaler 0 (fosc base)	15-bit prescaler
Prescaler 1 (fs base)	3-bit prescaler

Prescaler 0 outputs fosc/2, fosc/4, fosc/16, fosc/32, fosc/64, fosc/128, fosc/2^{13}, fosc/2^{15} as cycle clock.
Prescaler 1 outputs fs/2, fs/4, fs/8 as cycle clock.
Use the prescalers when cycle clock based on fosc and fs is used on the following peripheral functions ;

External interrupt 0 interface (with noise filter)
External interrupt 1 interface (with noise filter)
Timer 0 (8-bit timer counter)
Timer 1 (8-bit timer counter)
Timer 2 (8-bit timer counter)
Timer 3 (8-bit timer counter)
Serial 0 (Clock synchronous / Duplex UART)

Refer to chapter 2. 2-5 Clock Switching [p.II-23] for fosc and fs.

5-1-1 Peripheral Functions

Table 5-1-1 shows the selectable clock sources used in each peripheral functions used with prescaler block output.

Table 5-1-1 Peripheral Functions Used with Prescaler Output

Clock source selection	Peripheral functions						
	External interrupt 0	External interrupt 1	Timer 0	Timer 1	Timer 2	Timer 3	Serial 0
fosc/2	-	-	-	-	-	-	√
fosc/4	-	-	√	√	√	√	√
fosc/16	-	-	√	√	√	√	√
fosc/32	-	-	√	-	√	-	-
fosc/64	-	-	√	-	√	√	√
fosc/128	√	√	-	-	-	√	-
$fosc/2^{13}$	-	-	-	√	-	-	-
$fosc/2^{15}$	-	-	-	√	-	-	-
fs/2	-	-	√	√	√	√	√
fs/4	-	-	√	-	√	-	√
fs/8	-	-	-	√	-	√	-
Timer 3 output	-	-	-	-	-	-	√

5-1-2 Block Diagram

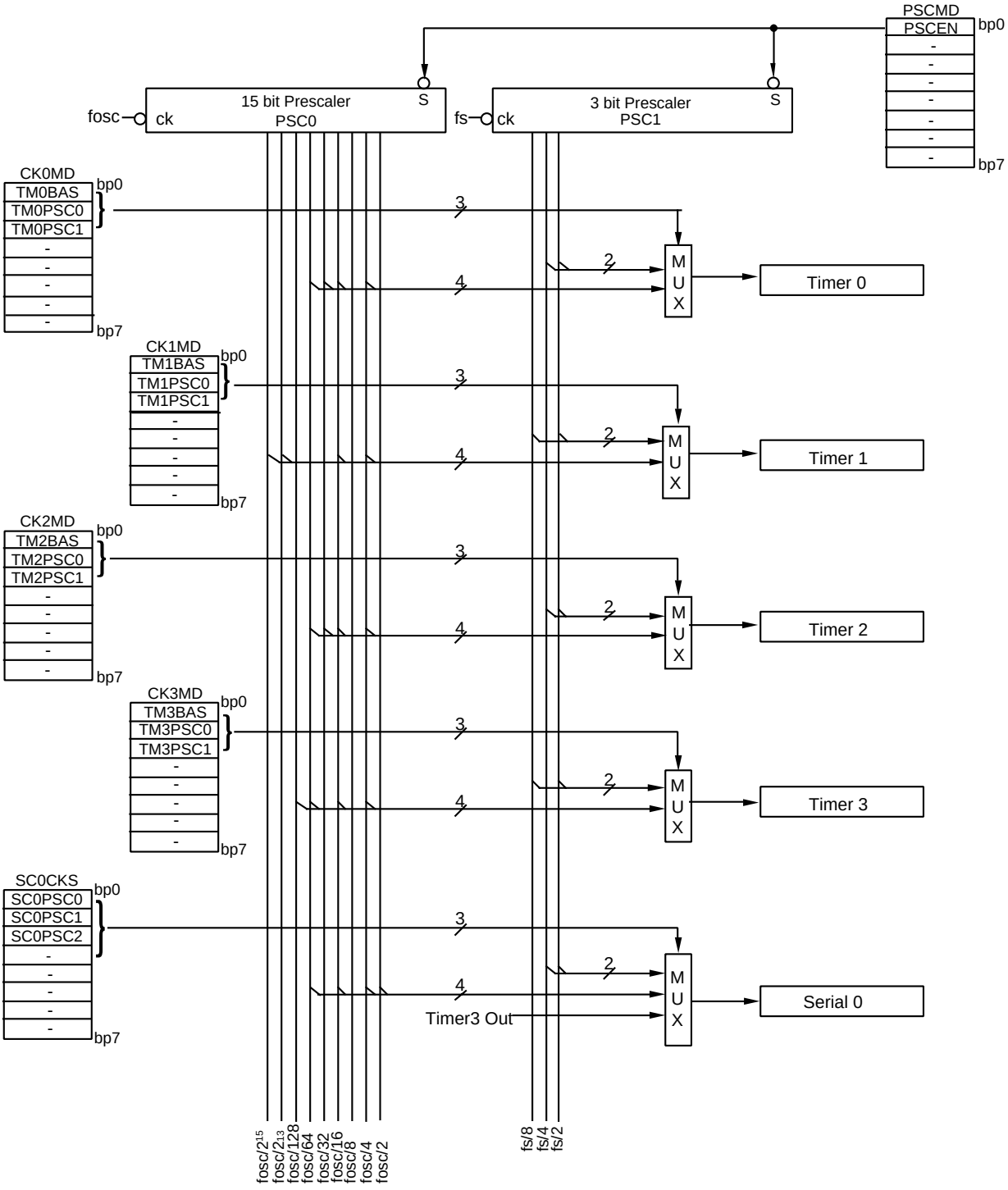


Figure 5-1-1 Prescaler Block Diagram

5-2 Control Registers

5-2-1 Registers List

Table 5-2-1 shows registers control prescaler.

Table 5-2-1 Prescaler Control Registers

Register	Address	R/W	Function	Page
PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V - 7
CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V - 7
CK2MD	x'03F5E'	R/W	Timer 2 prescaler selection register	V - 8
CK3MD	x'03F5F'	R/W	Timer 3 prescaler selection register	V - 8
SC0CKS	x'03F97'	R/W	Serial 0 transfer clock selection register	V - 9, XI - 11

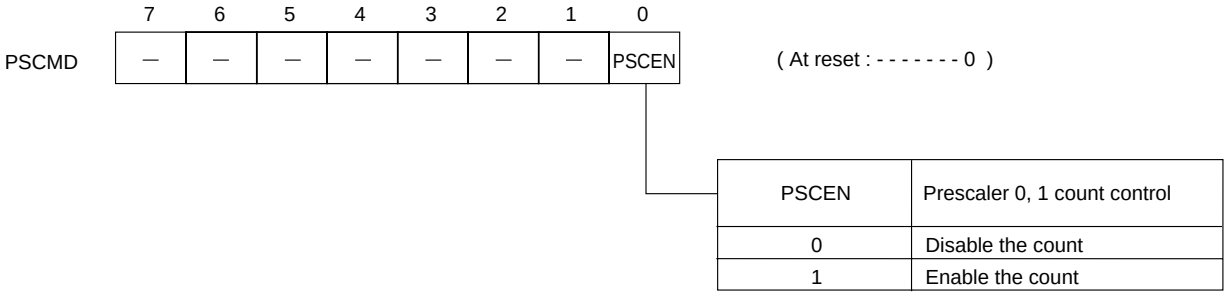
R/W : Readable/Writable

5-2-2 Control Registers

There are three types of Prescaler control registers; the register controls prescaler operation is the prescaler control register (PSCMD), and the register select prescaler output are the timer prescaler selection register (CKnMD) and the serial interface transfer clock selection register (SCnCKS).

The prescaler control register controls prescaler count operation

■Prescaler Control Register (PSCMD)

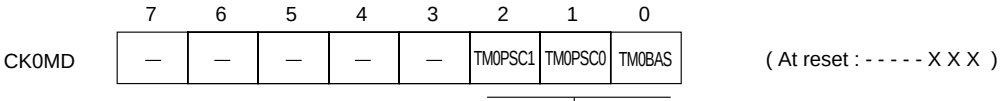


PSCEN	Prescaler 0, 1 count control
0	Disable the count
1	Enable the count

Figure 5-2-1 Prescaler Control Register (PSCMD : x'03F6F', R/W)

The timer prescaler selection register selects the count clock used for 8-bit timer.

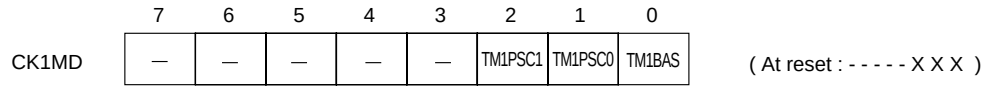
■Timer 0 Prescaler Selection Register (CK0MD)



TM0PSC1	TM0PSC0	TM0BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-2 Timer 0 Prescaler Selection Register (CK0MD : x'03F56', R/W)

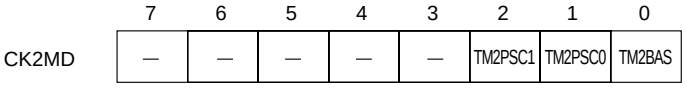
■Timer 1 prescaler selection register (CK1MD)



TM1PSC1	TM1PSC0	TM1BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/2^{13}
	1		fosc/2^{15}
-	0	1	fs/2
	1		fs/8

Figure 5-2-3 Timer 1 Prescaler Selection Register (CK1MD : x'03F57', R/W)

■Timer 2 Prescaler Selection Register (CK2MD)

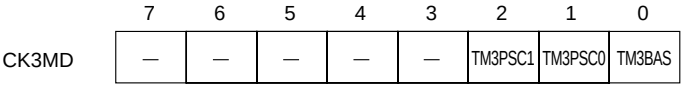


(At reset : - - - - - X X X)

TM2PSC1	TM2PSC0	TM2BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-4 Timer 2 Prescaler Selection Register (CK2MD : x'03F5E', R/W)

■Timer 3 Prescaler Selection Register (CK3MD)



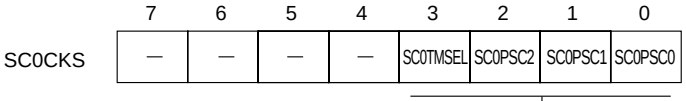
(At reset : - - - - - X X X)

TM3PSC1	TM3PSC0	TM3BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/64
	1		fosc/128
-	0	1	fs/2
	1		fs/8

Figure 5-2-5 Timer 3 Prescaler Selection Register (CK3MD : x'03F5F', R/W)

The serial interface transfer clock selection register (SCnCKS) selects the transfer clock used for serial interface transfer.

■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)



SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0	Clock source selection
-	0	0	0	fosc/2
			1	fosc/4
		1	0	fosc/16
			1	fosc/64
	1	0	0	fs/2
			1	fs/4
0		1	0	Disable
			1	Timer 3 output
1			0	Disable
			1	Disable

Figure 5-2-6 Serial Interface 0 Transfer Clock Selection Register (SC0CKS : x'03F97', R/W)

5-3 Operation

5-3-1 Operation

■Prescaler Operation (Prescalers 0 and 1)
Prescaler 0 and prescaler 1 are 15-bit, 3-bit free running counter that divide the base clock. The PSCEN flag of the prescaler control register (PSCMD) starts or stops the count up operation.

■Count Timing of Prescaler Operation (Prescalers 0 and 1)
Prescaler 0 counts up at the falling edge of fosc.
Prescaler 1 counts up at the falling edge of fs.

■Peripheral Functions with Prescaler Output Cycle Clock
Table 5-3-1 shows the peripheral functions that are capable of using prescaler output clock as a clock source, and the control registers that select the clock source..

Table 5-3-1 Peripheral Functions Used with Prescaler Output Cycle Clock

Peripheral functions		Control register
External interrupt 0	Noise filter sampling clock	-
External interrupt 1	Noise filter sampling clock	-
Timer 0	Count clock	CK0MD
Timer 1	Count clock	CK1MD
Timer 2	Count clock	CK2MD
Timer 3	Count clock	CK3MD
Serial 0	Transfer clock	SC0CKS

When the prescaler output clock source is used, counting of prescaler should be enabled before starting the peripheral functions.

5-3-2 Setup Example

■Prescaler Setup Example (Timer 0 count clock)
Select the clock of fosc/16 output from the prescaler 0, for the count clock of the timer 0.
Example of the setup procedure is shown below.

Setup Procedure	Description
(1) Select the prescaler output. CK0MD (x'3F56') bp2-1 : TM0PSC1-0 = 01 bp0 : TM0BAS = 0 (2) Enable the prescaler output. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Select the prescaler output to fosc/16 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). (2) Enable the prescaler counting by setting the PSCEN flag of the prescaler control register (PSCMD) to "1".

Enable the prescaler counting by the PSCEN flag of the prescaler control register (PSCMD). The prescaler counting is started after it is enabled.
Start the timer operation after the prescaler is set. Also, the selection of the prescaler output should be set by the timer mode register.

Chapter 6 8-bit Timers

6

6-1 Overview

This LSI contains four general purpose 8-bit timers (Timers 0, 1, 2 and 3). The general purpose 8-bit timers are configured in pairs so that they can be used as 16-bit timers with cascade connection. In a cascade connecion, timers 0, and 2 form the "timer 0", or the lower 8 bits of 16-bit counter, and timers 1 and 3 form the "timer 1", or the upper 8 bits.

Fosc or fs can be selected as the clock source for each timer by using the prescaler. Also, remote control output circuit is built in.

6-1-1 Functions

Table 6-1-1 shows functions that can be used with each timer.

Table 6-1-1 Timer Functions

	Timer 0 (8 bit)	Timer 1 (8 bit)	Timer 2 (8 bit)	Timer 3 (8 bit)
Interrupt source	TM0IRQ	TM1IRQ	TM2IRQ	TM3IRQ
Timer operation	√	√	√	√
Event count	√	√	√	√
Timer pulse output	√	√	√	√
PWM output	√	-	√	-
High current timer output pin	√	-	√	-
Additional pulse method PWM(2bit)	-	-	√	-
Synchronous output	-	√	√	-
Serial transfer clock output	-	-	-	√
Pulse width measurement	√	-	√	-
Cascade connection	√		√	
Remote control carrier output	√	-	-	√
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input	fosc fosc/4 fosc/16 $fosc/2^{13}$ $fosc/2^{15}$ fs/2 fs/8 fx TM1IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM2IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM3IO input

fosc : Machine clock (High frequency oscillation)
fx : Machine clock (Low frequency oscillation)
fs : System clock [☞ Chapter 2 2-5 Clock Switching]
- When timers 3 are used as a baud rate timer for serial function, it is not used as a general timer.

6-1-2 Block Diagram

■Timers 0 and 1 Block Diagram

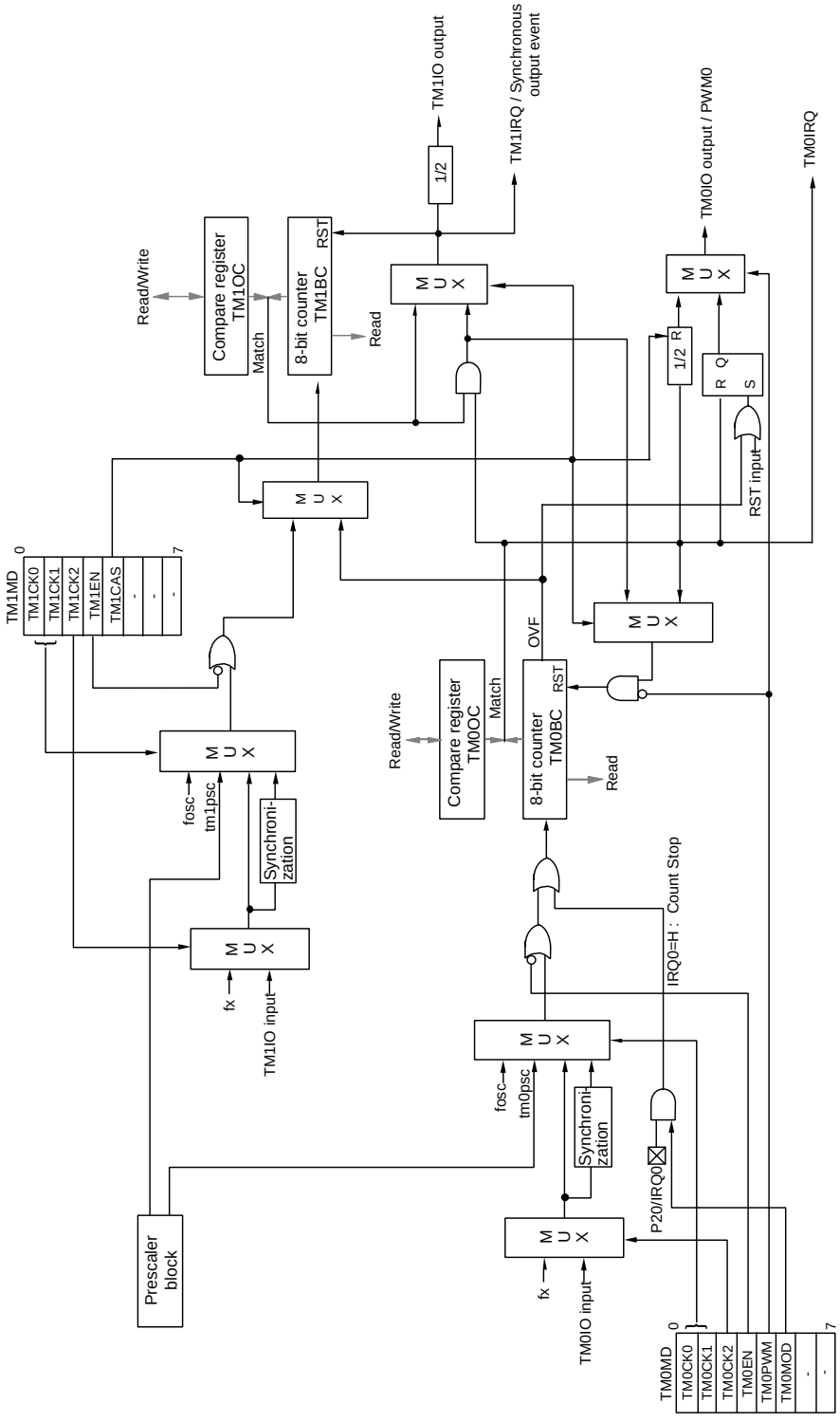


Figure 6-1-1 Timers 0 and 1 Block Diagram

■Timers 2 and 3 Block Diagram

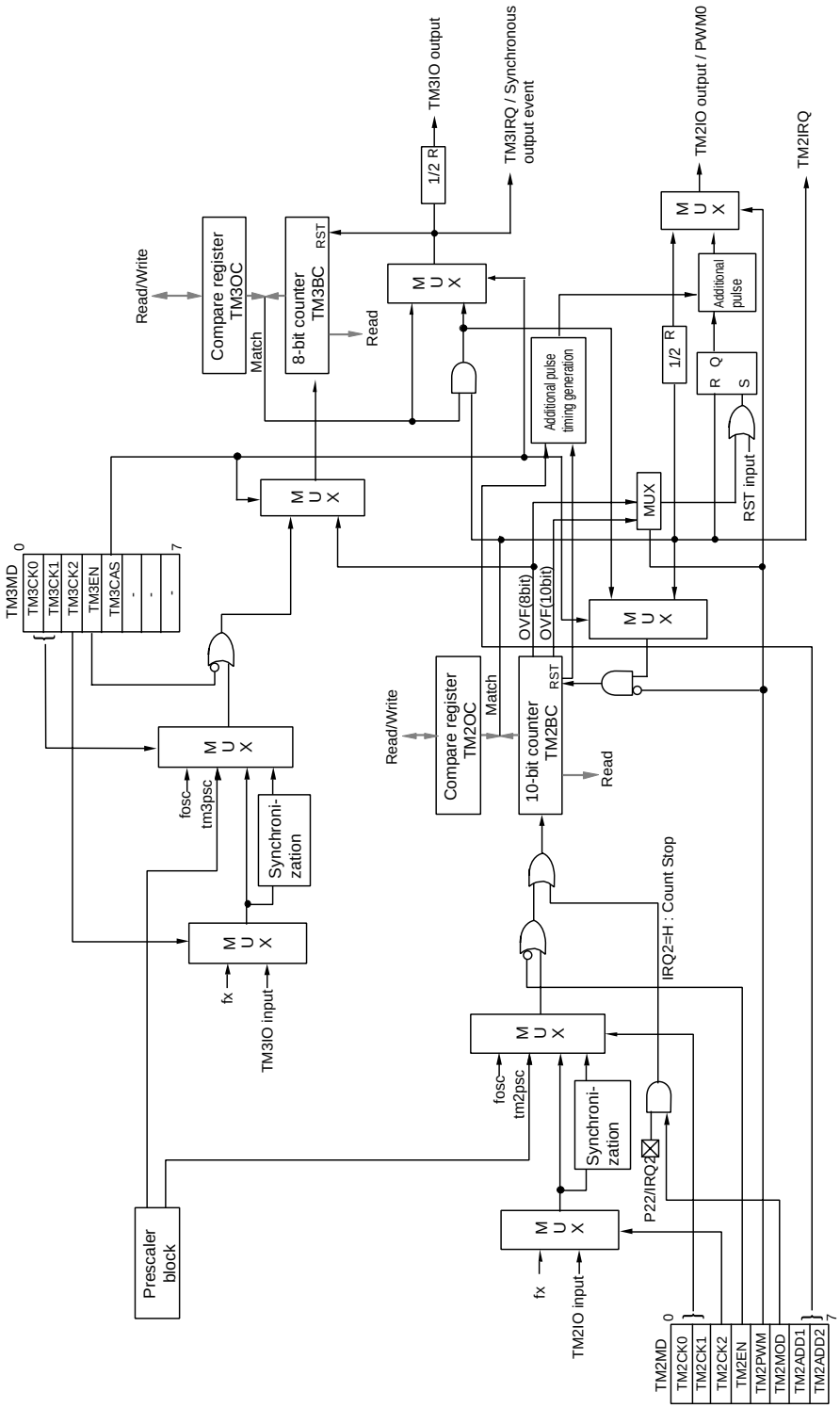


Figure 6-1-2 Timers 2 and 3 Block Diagram

■Remote Control Carrier Output Block Diagram

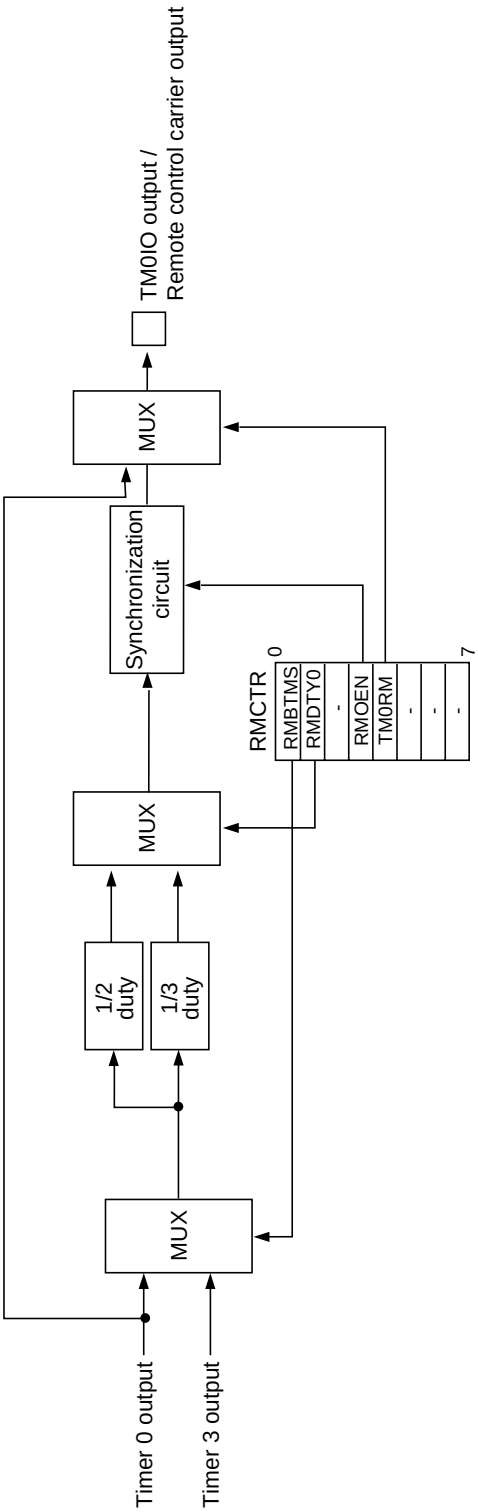


Figure 6-1-3 Remote Control Carrier Output Block Diagram

6-2 Control Registers

Timers 0 to 3 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).
When the prescaler output is selected as the count clock source of timers 0 to 3, they should be controlled by the prescaler control register (PSCMD) and the prescaler selection register (CKnMD). Remote control is controlled by the remote control carrier output control register (RMCTR).

6-2-1 Registers

Table 6-2-1 shows registers that control timers 0 to 3 and remote control.

Table 6-2-1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 0	TM0BC	x'03F50'	R	Timer 0 binary counter	VI - 9
	TM0OC	x'03F52'	R/W	Timer 0 compare register	VI - 8
	TM0MD	x'03F54'	R/W	Timer 0 mode register	VI - 10
	CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V - 7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register	III - 21
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 11
Timer 1	TM1BC	x'03F51'	R	Timer 1 binary counter	VI - 9
	TM1OC	x'03F53'	R/W	Timer 1 compare register	VI - 8
	TM1MD	x'03F55'	R/W	Timer 1 mode register	VI - 11
	CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V - 7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register	III - 22
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 11
Timer 2	TM2BC	x'03F58'	R	Timer 2 binary counter	VI - 9
	TM2OC	x'03F5A'	R/W	Timer 2 compare register	VI - 8
	TM2MD	x'03F5C'	R/W	Timer 2 mode register	VI - 12
	CK2MD	x'03F5E'	R/W	Timer 2 prescaler selection register	V - 8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	TM2ICR	x'03FEB'	R/W	Timer 2 interrupt control register	III - 23
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 11

	Register	Address	R/W	Function	Page
Timer 3	TM3BC	x'03F59'	R	Timer 3 binary counter	VI - 9
	TM3OC	x'03F5B'	R/W	Timer 3 compare register	VI - 8
	TM3MD	x'03F5D'	R/W	Timer 3 mode register	VI - 13
	CK3MD	x'03F5F'	R/W	Timer 3 prescaler selection register	V - 8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	TM3ICR	x'03FEC'	R/W	Timer 3 interrupt control register	III - 24
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 11
Remote control	RMCTR	x'03F6E'	R/W	Remote control carrier output control register	VI - 14

R/W : Readable / Writable

R : Readable only

6-2-2 Programmable Timer Registers

Each of timers 0 to 3 has 8-bit programmable timer registers. Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter are stocked.

■Timer 0 Compare Register (TM0OC)

	7	6	5	4	3	2	1	0	
TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	(At reset : X X X X X X X X)

Figure 6-2-1 Timer 0 Compare Register (TM0OC : x'03F52', R/W)

■Timer 1 Compare Register (TM1OC)

	7	6	5	4	3	2	1	0	
TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	(At reset : X X X X X X X X)

Figure 6-2-2 Timer 1 Compare Register (TM1OC : x'03F53', R/W)

■Timer 2 Compare Register (TM2OC)

	7	6	5	4	3	2	1	0	
TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	(At reset : X X X X X X X X)

Figure 6-2-3 Timer 2 Compare Register (TM2OC : x'03F5A', R/W)

■Timer 3 Compare Register (TM3OC)

	7	6	5	4	3	2	1	0	
TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	(At reset : X X X X X X X X)

Figure 6-2-4 Timer 3 Compare Register (TM3OC : x'03F5B', R/W)

Binary counter is 8-bit up counter. If any data is written to compare register the counting is stopped and binary counter is cleared to x'00'.

■Timer 0 Binary Counter (TM0BC)

	7	6	5	4	3	2	1	0	
TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	(At reset : X X X X X X X X)

Figure 6-2-5 Timer 0 Binary Counter (TM0BC : x'03F50', R)

■Timer 1 Binary Counter (TM1BC)

	7	6	5	4	3	2	1	0	
TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	(At reset : X X X X X X X X)

Figure 6-2-6 Timer 1 Binary Counter (TM1BC : x'03F51', R)

■Timer 2 Binary Counter (TM2BC)

	7	6	5	4	3	2	1	0	
TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	(At reset : X X X X X X X X)

Figure 6-2-7 Timer 2 Binary Counter (TM2BC : x'03F58', R)

■Timer 3 Binary Counter (TM3BC)

	7	6	5	4	3	2	1	0	
TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	(At reset : X X X X X X X X)

Figure 6-2-8 Timer 3 Binary Counter (TM3BC : x'03F59', R)

6-2-3 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 0 to 3.

■Timer 0 Mode Register (TM0MD)

	7	6	5	4	3	2	1	0
TM0MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0

(At reset : - - 0 0 0 0 0 0)

TM0CK2	TM0CK1	TM0CK0	Clock source selection
-	0	0	fosc
		1	tm0psc (prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM0IO input
		1	Synchronous TM0IO input

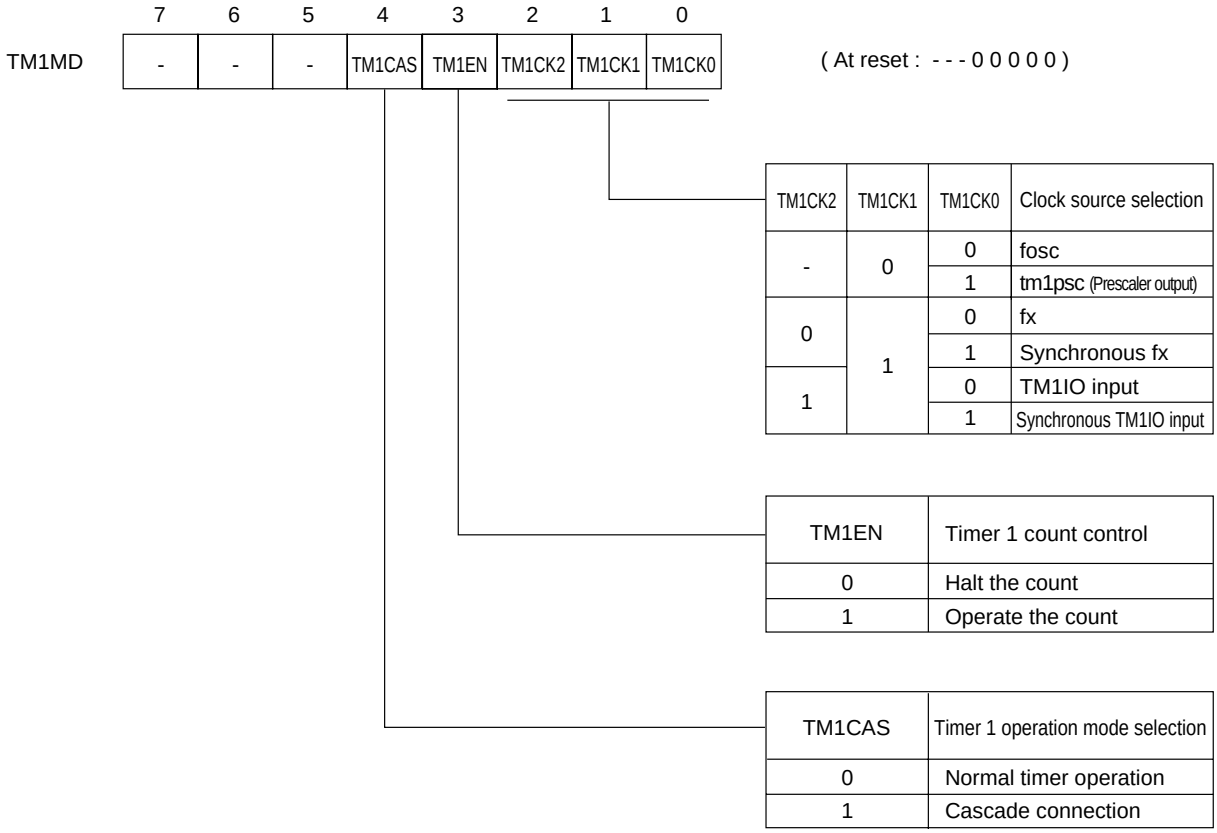
TM0EN	Timer 0 count control
0	Halt the count
1	Operate the count

TM0PWM	Timer 0 operation mode selection
0	Normal timer operation
1	PWM operation

TM0MOD	Pulse width measurement control
0	Normal timer operation
1	Measure the pulse width of P20/IRQ0

Figure 6-2-9 Timer 0 Mode Register (TM0MD : x'03F54', R/W)

■Timer 1 Mode Register (TM1MD)



TM1CK2	TM1CK1	TM1CK0	Clock source selection
-	0	0	fosc
		1	tm1psc (Prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM1IO input
		1	Synchronous TM1IO input

TM1EN	Timer 1 count control
0	Halt the count
1	Operate the count

TM1CAS	Timer 1 operation mode selection
0	Normal timer operation
1	Cascade connection

Figure 6-2-10 Timer 1 Mode Register (TM1MD : x'03F55', R/W)

■Timer 2 Mode Register (TM2MD)

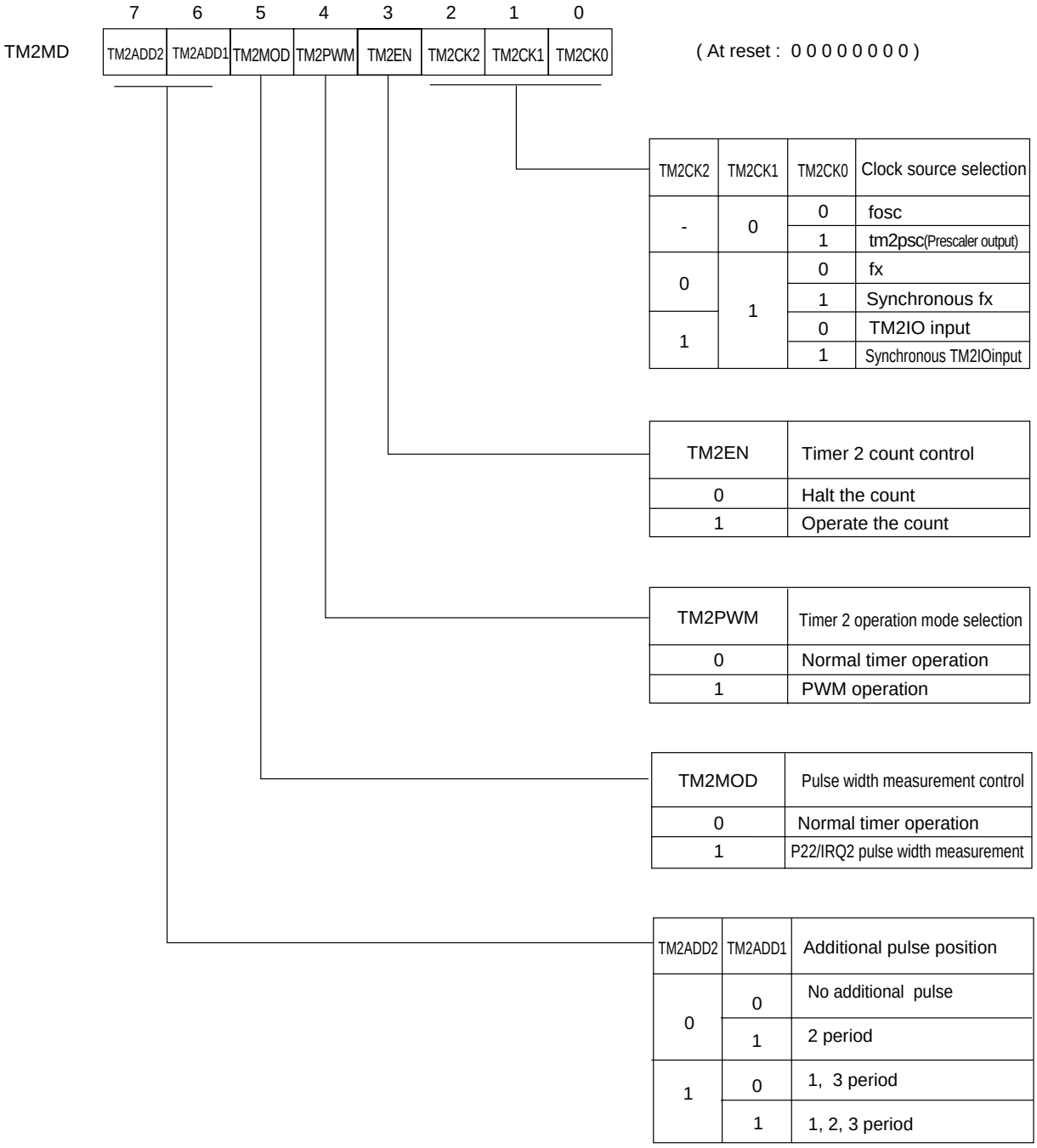
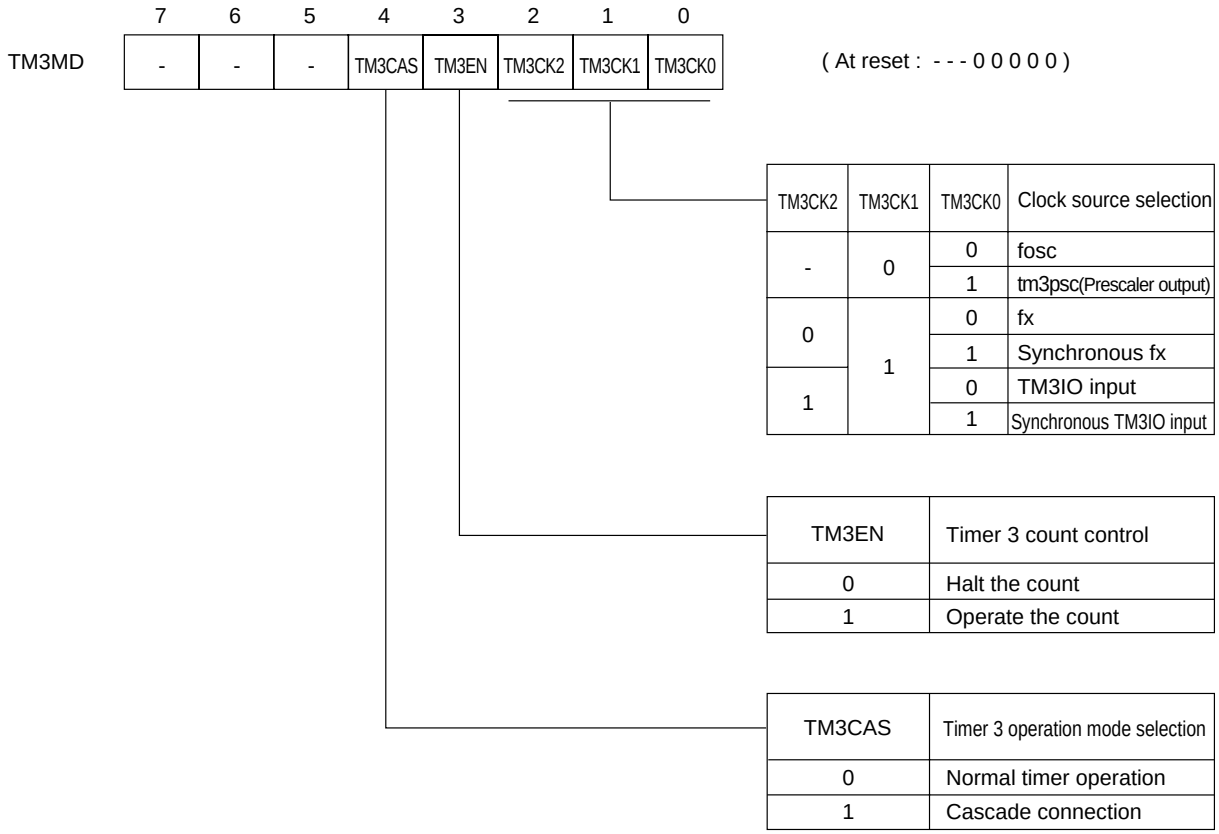

7 6 5 4 3 2 1 0
TM2MD
TM2ADD2 TM2ADD1 TM2MOD TM2PWM TM2EN TM2CK2 TM2CK1 TM2CK0
(At reset : 0 0 0 0 0 0 0 0)
TM2CK2 TM2CK1 TM2CK0 Clock source selection
- 0 0 fosc
1 tm2psc(Prescaler output)
0 1 0 fx
1 Synchronous fx
1 0 TM2IO input
1 Synchronous TM2IOinput
TM2EN Timer 2 count control
0 Halt the count
1 Operate the count
TM2PWM Timer 2 operation mode selection
0 Normal timer operation
1 PWM operation
TM2MOD Pulse width measurement control
0 Normal timer operation
1 P22/IRQ2 pulse width measurement
TM2ADD2 TM2ADD1 Additional pulse position
0 0 No additional pulse
1 2 period
1 0 1, 3 period
1 1, 2, 3 period

Figure 6-2-11 Timer 2 Mode Register (TM2MD : x'03F5C', R/W)

■Timer 3 Mode Register (TM3MD)



TM3CK2	TM3CK1	TM3CK0	Clock source selection
-	0	0	fosc
		1	tm3psc(Prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM3IO input
		1	Synchronous TM3IO input

TM3EN	Timer 3 count control
0	Halt the count
1	Operate the count

TM3CAS	Timer 3 operation mode selection
0	Normal timer operation
1	Cascade connection

Figure 6-2-12 Timer 3 Mode Register (TM3MD : x'03F5D', R/W)

■Remote Control Carrier Output Control Register (RMCTR)

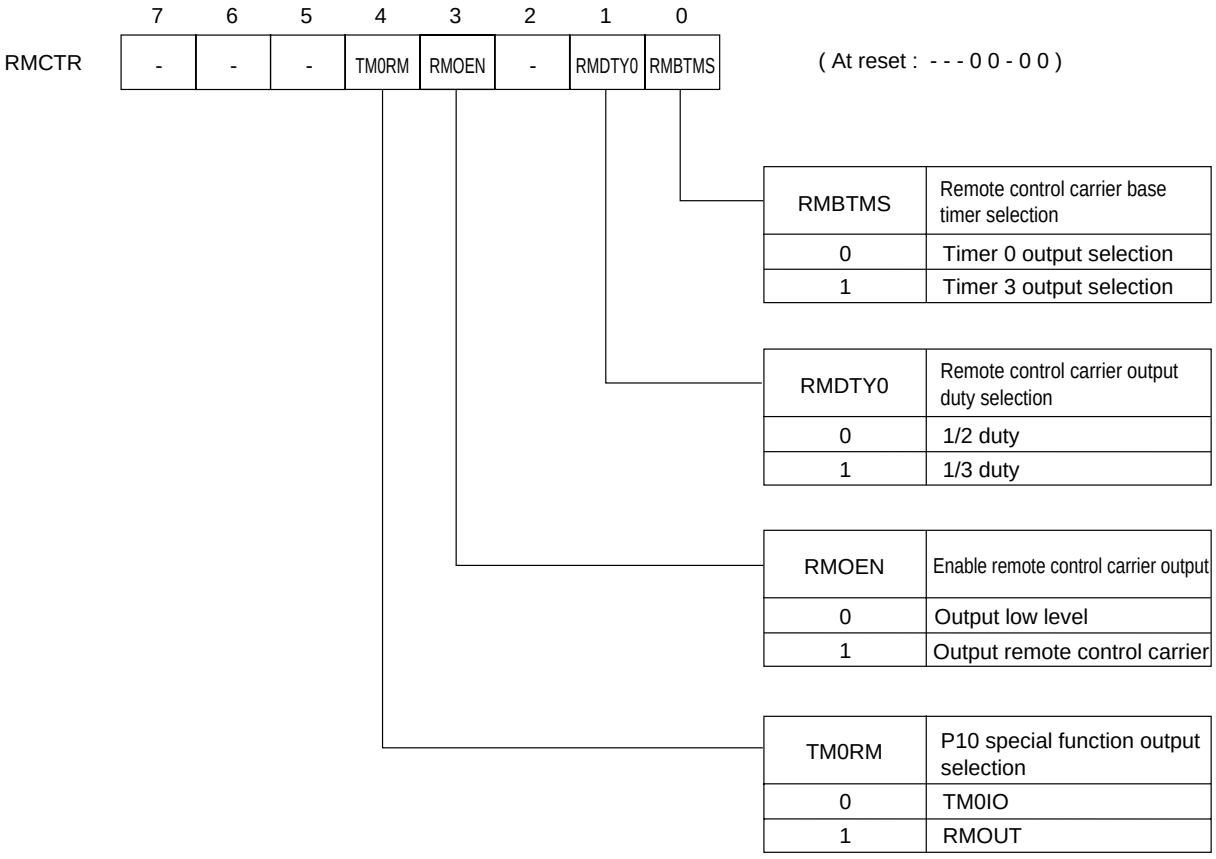


Figure 6-2-13 Remote Control Carrier Output Control Register (RMCTR : x'03F6E', R/W)

6-3 Operation

6-3-1 Operation

The timer operation can constantly generate interrupts.

■8-bit Timer Operation (Timers 0, 1, 2, and 3)
The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from x'00'.
Table 6-3-1 shows clock source that can be selected by timer.

Table 6-3-1 Clock Source (Timers 0, 1, 2, and 3) at Timer Operation

Clock source	per Count	Timer 0 (8 bit)	Timer 1 (8 bit)	Timer 2 (8 bit)	Timer 3 (8 bit)
fosc	50 ns	√	√	√	√
fosc/4	200 ns	√	√	√	√
fosc/16	800 ns	√	√	√	√
fosc/32	1.6 µs	√	-	√	-
fosc/64	3.2 µs	√	-	√	√
fosc/128	6.4 µs	-	-	-	√
$fosc/2^{13}$	409.6 µs	-	√	-	-
$fosc/2^{15}$	1.64 ms	-	√	-	-
fs/2	200 ns	√	√	√	√
fs/4	400 ns	√	-	√	-
fs/8	800 ns	-	√	-	√
fx	30.5 µs	√	√	√	√
Notes : fosc = 20 MHz fx = 32.768 kHz fs = fosc/2 = 10 MHz					

■Count Timing of Timer Operation (Timers 0, 1, 2, and 3)

Binary counter counts up with selected clock source as a count clock.

The basic operation of the whole function of 8-bit timer is as follows ;

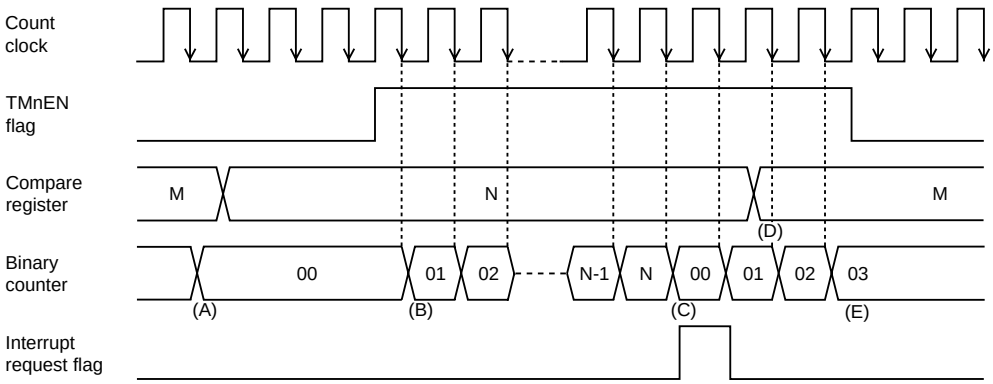


Figure 6-3-1 Count Timing of Timer Operation (Timers 0, 1, 2, and 3)

(A) If the value is written to the compare register during the TMnEN flag is stopped ("0"), the binary counter is cleared to x'00', at the writing cycle.

(B) If the TMnEN flag is operated ("1"), the binary counter is started to count.
The counter starts to count up at the falling edge of the count clock.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to x'00' and the counting is restarted.

(D) Even if the compare register is rewritten during the TMnEN flag is enabled ("1"), the binary counter is not changed.

(E) If the TMnEN flag is stopped ("0"), the binary counter is stopped.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as: Compare register setting = (count till the interrupt request - 1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer is started.

The timer n interrupt request generation (at TMnOC = x'00') has the same waveform at TMnOC = x'01'.

6-3-2 Setup Example

■Timer Operation Setup Example (Timers 0, 1, 2, and 3)
Timer function can be set by using timer 0 that generates the constant interrupt. Interrupt is generated every 250 cycles (100 µs) by selecting fs/4 (at fosc = 20 MHz operation) as a clock source.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the counting of timer 0.
(2) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(3) Select the prescaler output to the clock source by the TM0CK2-0 flag of the TM0MD register.
(4) Select the prescaler output and enable the counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0 = 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select fs/4 to the prescaler output by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the counting of the prescaler.
(5) Set the cycle of the interrupt generation. TM0OC (x'3F52') = x'F9'	(5) Set the value of the interrupt generation cycle to the timer 0 compare register (TM0OC). The cycle is 250, so that the setting value is set to 249 (x'F9'). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). [☞ Chapter 3 3-1-4. Interrupt flag setting] If the interrupt request flag may be already set, clear the request flag.

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.

The TM0BC starts to count up from 'x00'. When the TM0BC reaches the setting value of the TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of the TM0BC becomes x'00' and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may start to count up by the switching operation.

When fx is selected as a count clock source and if binary counter value is read out during opeartion, the read value may be uncertain. To prevent this, select synchronous fx as a count clock source. To do so timer n counts up the binary counter with a signal that is sync with the system clock, and you can always read out correct value from the binary counter. But with synchronous fx, return from STOP/HALT modes is disabled.

6-4 8-bit Event Count

6-4-1 Operation

Event count operation has 2 types ; TMnIO input and synchronous TMnIO input, according to the clock source selection.

■8-bit Event Count Operation

Event count operation means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table 6-4-1 Event Count Input Clock

	Timer 0	Timer 1	Timer 2	Timer 3
Event input	TM0IO input (P10)	TM1IO input (P11)	TM2IO input (P12)	TM3IO input (P13)
	Synchronous TM0IO input	Synchronous TM1IO input	Synchronous TM2IO input	Synchronous TM3IO input

■Count Timing of TMnIO Input (Timers 0, 1, 2, and 3)

When TMnIO input is selected, TMnIO input signal is directly input to the count clock of the timer n. The binary counter is started to count up at the falling edge of the TMnIO input signal.

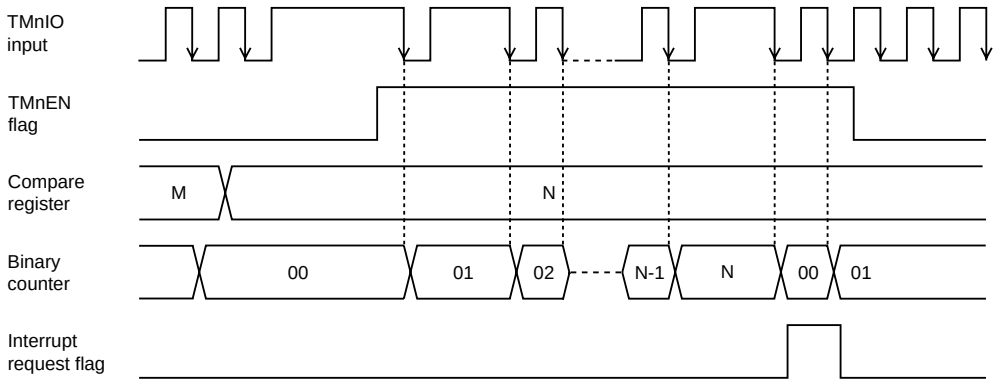


Figure 6-4-1 Count Timing of TMnIO Input (Timers 0 to 3)

When the TMnIO input is selected for count clock source and the value of the timer n binary counter is read out during operation, incorrect value at count up may be read out. To prevent this, use the event count by synchronous TMnIO input, as the following page.

■Count Timing of Synchronous TMnIO Input (Timers 0, 1, 2, and 3)

If the synchronous TMnIO input is selected, the synchronous circuit output signal is inputted to the timer n count clock. The synchronous circuit output signal is in synchronization with the falling edge of the system clock derived the TMnIO input signal.

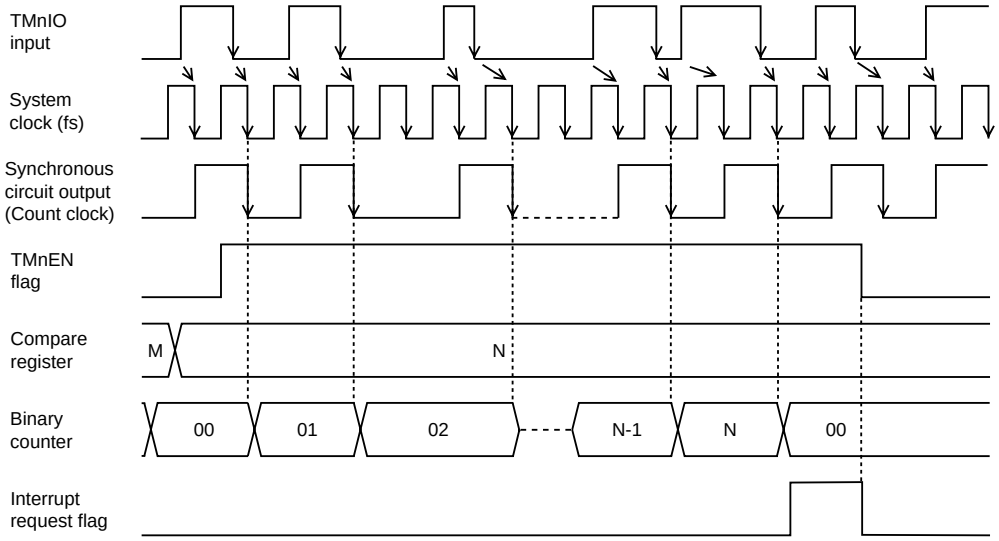


Figure 6-4-2 Count Timing of Synchronous TMnIO Input (Timers 0 to 3)

When the synchronous TMnIO input is selected as the count clock source, the timer n counter counts up in synchronization with system clock, therefore the correct value is always read out.

Synchronous TMnIO input cannot return from STOP/HALT mode.

6-4-2 Setup Example

■Event Count Setup Example (Timers 0, 1, 2, and 3)
If the falling edge of the TMnIO input pin signal is detected 5 times, an interrupt is generated.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to input. P1DIR (x'3F31') bp0 :P1DIR0 = 0	(2) Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "0" to set P10 pin to input mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Port Function]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 110	(4) Select the clock source to TM0IO input by the TM0CK2-0 flag of the TM0MD register.
(5) Set the interrupt generation cycle. TM0OC (x'3F52') = x'04'	(5) Set the timer 0 compare register (TM0OC) the interrupt generation cycle. Counting is 5, so the setting value should be 4. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, cancel all existing interrupt requests. [☞ Chapter 3 3-1-4. Interrupt Flag Setting]

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the event counting. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to start timer 0.

Every time TM0BC detects the falling edge of TM0IO input, TM0BC counts up from 'x00'. When TM0BC reaches the setting value of theTM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of TM0BC becomes x'00' and counting up is restarted.

6-5 8-bit Timer Pulse Output

6-5-1 Operation

The TMnIO pin can output a pulse signal at any frequency.

■Operation of Timer Pulse Output (Timers 0, 1, 2, and 3)
The timers can output signals of 2 x cycle of the setup value in the compare register (TMnOC). Output pins are as follows;

Table 6-5-1 Timer Pulse Output Pins

	Timer 0	Timer 1	Timer 2	Timer 3
Pulse output pin	TM0IO output (P10)	TM1IO output (P11)	TM2IO output (P12)	TM3IO output (P13)

■Count Timing of Timer Pulse Output (Timers 0, 1, 2, and 3)

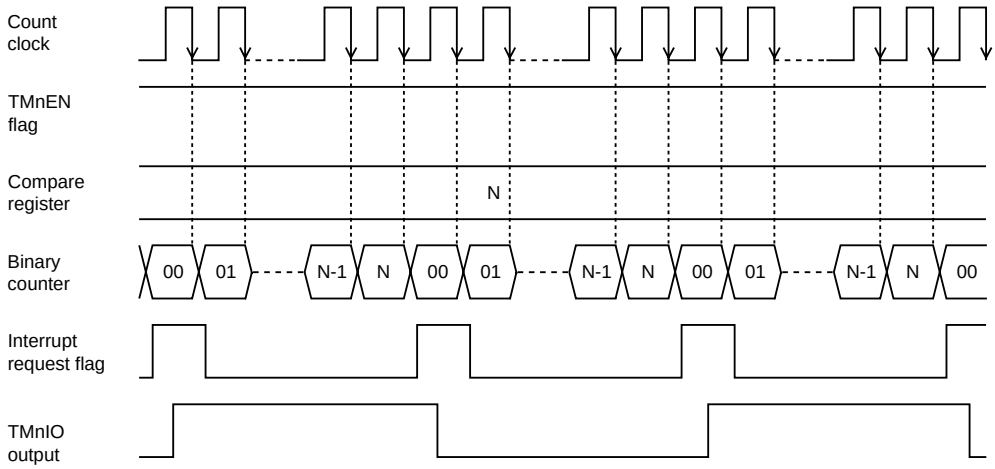


Figure 6-5-1 Count Timing of Timer Pulse Output (Timers 0 to 3)

The TMnIO pin outputs signals of 2 x cycle of the setup value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to x'00', TMnIO output (timer output) is inverted. The inversion of the timer output is changed at the rising edge of the count clock. This is happened to form waveform inside to correct the output cycle.

6-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 0, 1, 2, and 3)
TM0IO pin outputs 50 kHz pulse by using timer 0. For this, select fosc for clock source, and set a 1/2 cycle (100 kHz) for the timer 0 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Ports]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 000	(4) Select fosc for the clock source by the TM0CK2-0 flag of the TM0MD register.
(5) Set the timer pulse output cycle. TM0OC (x'3F52') = x'C7'	(5) Set the timer 0 compare register (TM0OC) to the 1/2 of the timer pulse output cycle. The setting value should be 200-1=199(x'C7'), for 100 kHz to be divided by 20 MHz. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM0BC counts up from x'00'. If TM0BC reaches the setting value of the TM0OC register, then TM0BC is cleared to x'00', TM0IO output signal is inverted and TM0BC restart to count up from x'00'.

At TMnOC = x'00', timer pulse output has the same waveform to at x'01'.

If any data is written to compare register binary counter is stopped, timer output is reset to "L".

Compare register value calculation;

$$\text{Compare register value} = \frac{\text{Timer pulse output cycle}}{\text{Selected clock cycle x 2}} - 1$$

6-6 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

6-6-1 Operation

■Operation of 8-bit PWM Output (Timers 0, and 2)

The PWM waveform with an arbitrary duty cycle is generated by setting the duty cycle of PWM period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer. Table 6-6-1 shows PWM output pins ;

Table 6-6-1 Output Pins of PWM Output

	Timer 0	Timer 2
PWM output pin	TM0IO output pin (P10)	TM2IO output pin (P12)

■Count Timing of PWM Output (at Normal) (Timers 0, and 2)

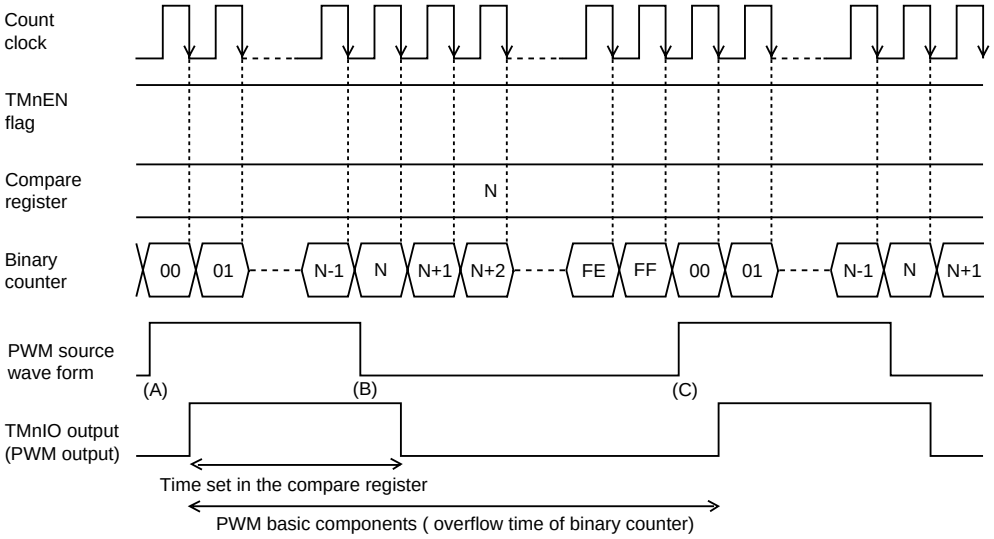


Figure 6-6-1 Count Timing of PWM Output (at Normal)

PWM source waveform,

(A) is "H" while counting up from x'00' to the value stored in the compare register.

(B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.

(C) is "H" again, if the binary counter is overflown.

The PWM outputs PWM source waveform with 1 count clock delay, because the waveform is created inside to correct the output cycle.

■Count Timing of PWM Output (when the compare register is x'00') (Timers 0, and 2)
Here is the count timing when the compare register is set to x'00' ;

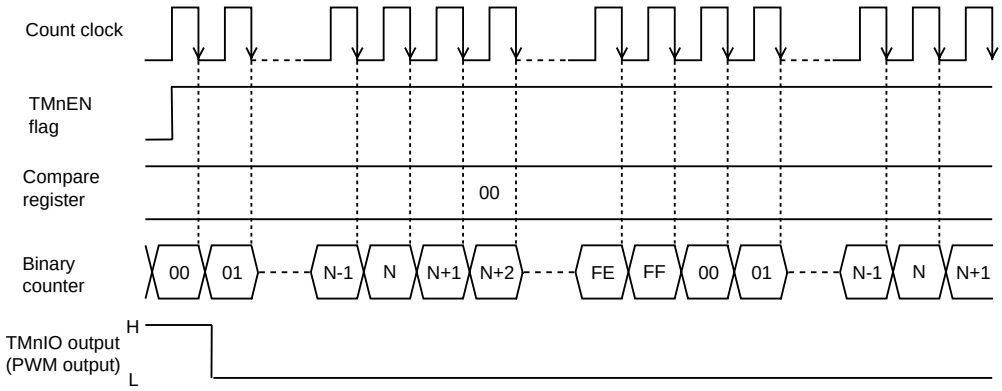


Figure 6-6-2 Count Timing of PWM Output (when compare register is x'00')

When TMnEN flag is stopped ("0") PWM output is "H".

■Count Timing of PWM Output (when the compare register is x'FF') (Timers 0, and 2)
Here is the count timing when the compare register is set to x'FF' ;

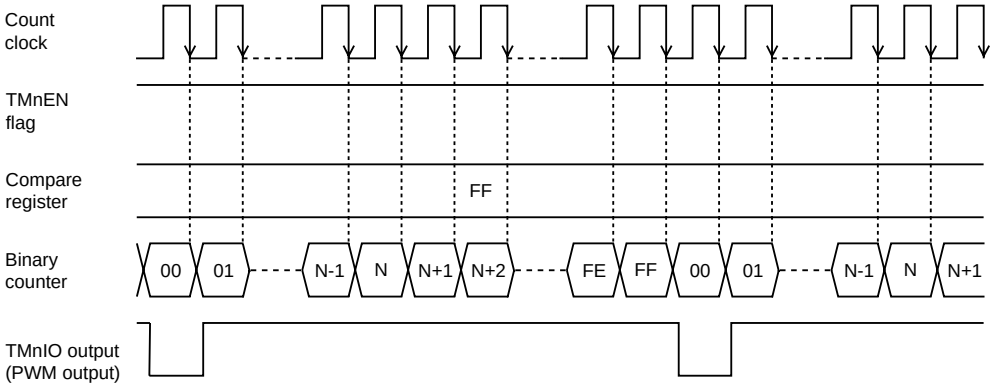


Figure 6-6-3 Count Timing of PWM Output (when compare register is x'FF')

6-6-2 Setup Example

■PWM Output Setup Example (Timers 0, and 2)

The 1/4 duty cycle PWM output waveform is output from the TM0IO output pin at 128 Hz by using timer 0. Low frequency oscillation(fx) is at 32.768 kHz. Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register.

An example setup procedure, with a description of each step is shown below.

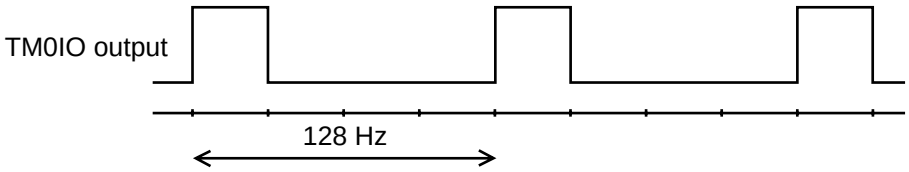


Figure 6-6-4 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin to the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for the output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Ports]
(3) Select the PWM operation. TM0MD (x'3F54') bp4 :TM0PWM = 1 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag of the TM0MD register to "1", the TM0MOD flag to "0" to select the PWM operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 010	(4) Select "fs" for the clock source by the TM0CK2-0 flag of the TM0MD register.

Setup Procedure	Description
(5) Set the period of PWM "H" output. TM0OC (x'3F52') = x'40'	(5) Set the "H" period of PWM output to the timer 0 compare register (TM0OC). The setting value is set to 256 / 4 = 64 (x'40'), because it should be the 1/4 duty of the full count (256). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to operate timer 0.

TM0BC counts up from x'00'. PWM source waveform outputs "H" till TM0BC reaches the setting value of the TM0OC register, and outputs "L" after that. Then, TM0BC continues counting up, and PWM source waveform outputs "H" again, once overflow is happened, and TM0BC restarts counting up from x'00'. TM0IO pin outputs the PWM source waveform with 1 count clock delay.

The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TMnPWM flag of the TMnMD register.

6-6-3 PWM Output With Additional Pulse

■PWM Output with Additional Pulse Method (Timer 2)

In the additional pulse method, an additional bit is added to the 8-bit basic PWM output.

The bit0 to3 can be added during 4 cycle of basic PWM output.

Whether or not, and to which the additional bit is added during 4 cycles of basic PWM output can be controlled with the Timer 2 mode register (TM2MD bit 6, 7).

■Setting the position of the Additional Pulses

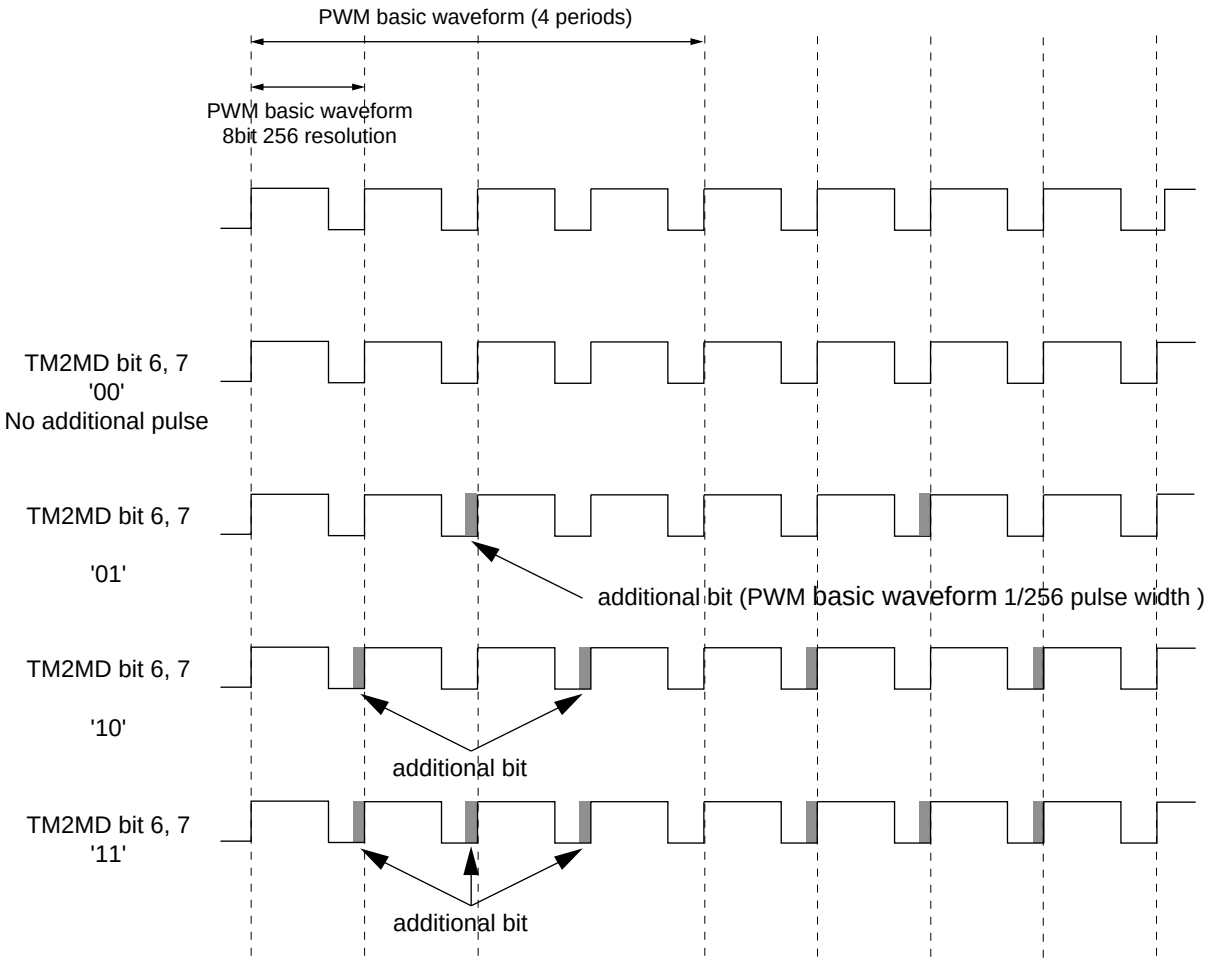
The positions of the additional pulse is set in the Timer 2 mode register (TM2MD) at bits 6 and 7. When TM2MD bits 6 and 7 are set as '00', no additional pulse is added to the basic PWM cycle. When set as '11', 3 out of the 4 periods in the basic PWM cycle are each added with an additional bit pulse.

Table 6-6-3 shows the relationship between the values TM2MD bits 6 and 7, and the additional pulses.

Figure 6-6-5 shows the relationship between values of TM2MD bits 6 and 7, and the positions of the additional pulses.

Table 6-6-3

TM2MD register set value		Additional Pulse position PWM basic wave form(4-periods)
bit7	bit6	
0	0	No additional Pulse
0	1	2 period
1	0	1 and 3 period
1	1	1, 2 and 3 period



During 4 cycles of the PWM basic waveform, additional pulses(1/256 pulse width of PWM basic waveform) can be added in any of the periods 0 to 3.

Figure 6-6-5

6-7 Synchronous Output

6-7-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latch data is output from port 6 at the next count clock.

■Synchronous Output Operation by 8-bit timer (Timer 1, Timer 2)

The port 6 latched data is output from the port 6 output pin in synchronization with the interrupt request generation by the match of the binary counter and the compare register.

Only port 6 can perform synchronous output operation, and individual bits can be set. 8-bit timers that have synchronous output operation are timer 1 and timer 2.

Table 6-7-1 Synchronous Output Port (Timer 1, Timer 2)

	Timer 1	Timer 2
Synchronous output port	Port 6	Port 6

■Timing of Synchronous Output (Timer 1, Timer 2)

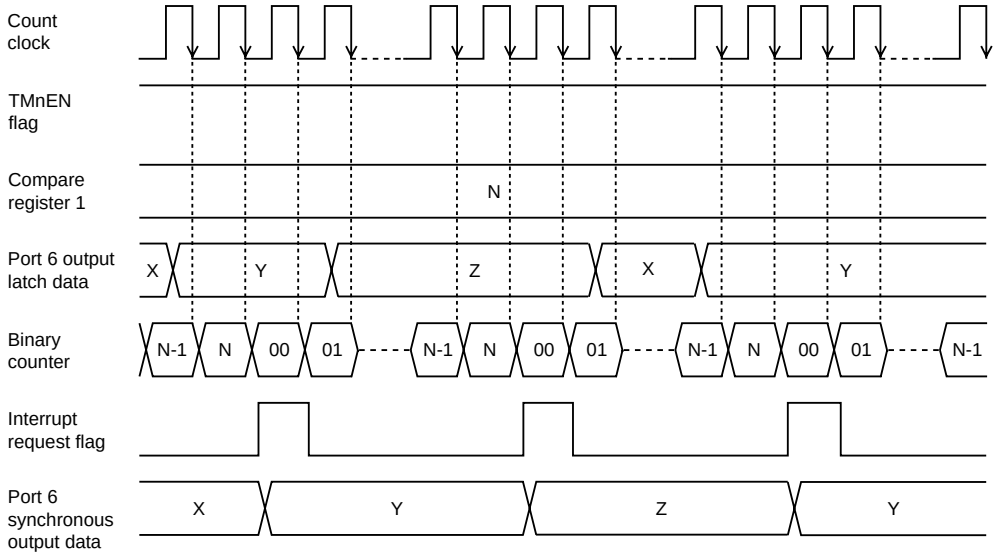


Figure 6-7-1 Timing of Synchronous Output (Timer 1, Timer2)

The port 6 output latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

6-7-2 Setup Example

■Synchronous Output Setup Example (Timer 1, Timer 2)

Setup example that latch data of port 6 is output constantly (100 µs) by using timer 2 from the synchronous output pin is shown below. The clock source of timer 2 is selected fs/4 (fosc=8 MHz at operation). A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Start the counter. TM2MD (x'3F5C') bp3 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 10	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "10" to set the synchronous output event to timer 2 interrupt.
(3) Set the synchronous output pin. P6SYO (x'3F1F') = x'FF' P6DIR (x'3F36') = x'FF'	(3) Set the port 6 synchronous output control register (P6SYO) to x'FF' to set the synchronous output pin. (P67 to P60 are synchronous output pin.) Set the port 6 direction control register (P6DIR) to x'FF' to set port 6 to output mode. Add pull-up resistor, if necessary. [☞ Chapter 4. I/O Ports]
(4) Select the normal timer operation. TM2MD (x'3F5C') bp4 :TM2PWM = 0 bp5 :TM2MOD = 0	(4) Set the TM2PWM flag and TM2MOD flag of the TM2MD register to "0" to select the normal timer operation.
(5) Select the count clock source. TM2MD (x'3F5C') bp2-0 :TM2CK2-0 = 001	(5) Select the prescaler output for clock source by TM2CK2-0 flag of the TM2MD register.
(6) Select the prescaler output and enable counting. CK2MD (x'3F5E') bp2-1 :TM2PSC1-0 = 01 bp0 :TM2BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(6) Select fs/4 for the prescaler output by TM2BAS flag, TM2PSC1-0 of the timer 2 prescaler selection register (CK2MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.

Setup Procedure	Description
(7) Set the synchronous output event generation cycle. TM2OC (x'3F5A') = x'63'	(7) Set the synchronous output generation cycle to the timer 2 compare register (TM2OC). The setting value is set to 100-1=99(x'63'), because 1 MHz is divided by 10 kHz. At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(8) Start the timer operation. TM2MD (x'3F5C') bp3 :TM2EN = 1	(8) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM2BC counts up from x'00'. If any data is written to the port 6 output register (P6OUT), the data of port 6 is output from the synchronous output pin in every time an interrupt request is generated by the match of TM2BC and the set value of the TM2OC register.

6-8 Serial Transfer Clock Output

6-8-1 Operation

Serial transfer clock can be created by using the timer output signal.

■Serial Transfer Clock Operation by 8-bit Timer (Timer 3)
Timer 3 output can be used as a transfer clock source for serial interface 0.

Table 6-8-1 Operation Timer for Serial Transfer Clock

Serial transfer clock	Timer 3
Serial interface 0	√

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

■Timing of Serial Transfer Clock (Timer 3)

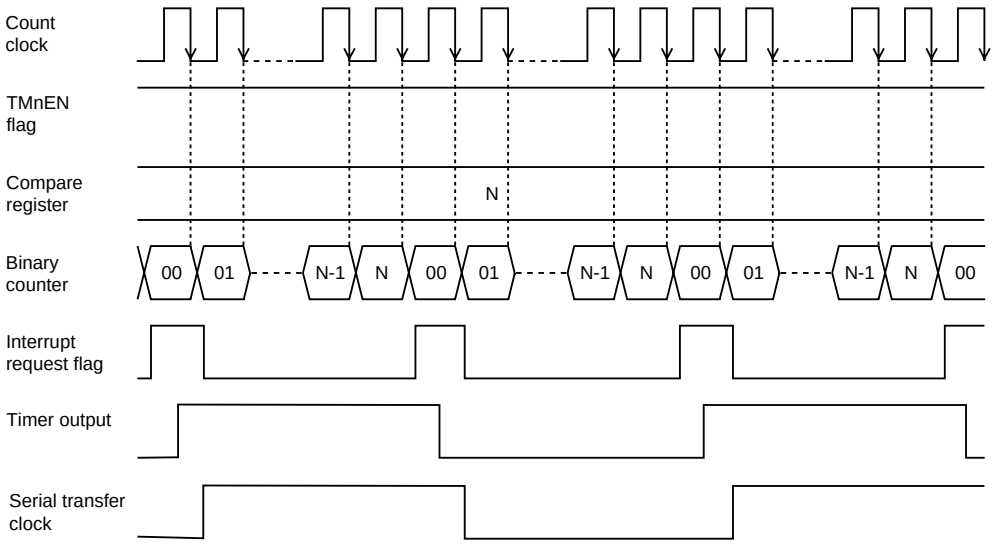


Figure 6-8-1 Timing of Serial Transfer Clock (Timer 3)

The timer output is synchronized to the serial transfer clock by the timer count clock, and its frequency is 1/2 of the set frequency set by the compare register.
Other count timings are same as the timing of timer operation. For the baud rate calculation and the serial interface setup, refer to chapter 11. Serial Interface 0 and chapter 12. Serial Interface 2.

6-8-2 Setup Example

■Serial Transfer Clock Setup Example (Timer 3)

How to create a transfer clock for half duplex UART (Serial 0) using with timer 3 is shown below. The baud rate is selected to be 300 bps, the source clock of timer 3 is selected to be fs/4 (at fosc=8 MHz). An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM3MD (x'3F5D') bp3 :TM3EN = 0	(1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop timer 3 counting.
(2) Select the normal timer operation. TM3MD (x'3F5D') bp4 :TM3CAS = 0	(2) Set the TM3CAS flag flag of the TM3MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM3MD (x'3F5D') bp2-0 :TM3CK2-0 = 001	(3) Select the clock source to prescaler output by the TM3CK2-0 flag of the TM3MD register.
(4) Select the prescaler output and enable counting. CK3MD (x'3F5F') bp2-1 :TM3PSC1-0 = 01 bp0 :TM3BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select the prescaler output to fs/8 by the TM3PSC1-0, TM3BAS flag of the timer 3 prescaler selection register (CK3MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(5) Set the baud rate. TM3OC (x'3F5B') = x'67'	(5) Set the timer 3 compare register (TM3OC) such a value that baud rate comes to 300 bps. [☞ Chapter 11. Table 11-3-23] At that time, the timer 3 binary counter (TM3BC) is initialized to x'00'.
(6) Start the timer operation TM3MD (x'3F5D') bp3 :TM4EN = 1	(6) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.

TM3BC counts up from x'00'. Timer 3 output is the clock of the serial interface 0 at transmission and reception.
For the compare register setup value and the serial operation setup, refer to chapter 11. Serial Interface 0.

6-9 Simple Pulse Width Measurement

6-9-1 Operation

Timer measures the "L" duration of the pulse signal input from the external interrupt pin.

■Simple Pulse Width Measurement Operation by 8-bit Timer (Timers 0, and 2)
When the input signal of the external interrupt pin (simple pulse width) is "L", the binary counter of the timer counts up. Pulse width "L" period can be measured by reading the count of timer. 8-bit timers that have the simple pulse width measurement function are timers 0, and 2.

Table 6-9-1 Simple Pulse Width Measurement Able Pins (Timers 0, and 2)

	Timer 0	Timer 2
Simple pulse width measurement enable pin	External interrupt 0 (P20/IRQ0)	External interrupt 2 (P22/IRQ2)

■Count Timing of Simple Pulse Width Measurement (Timer 0, Timer 2)

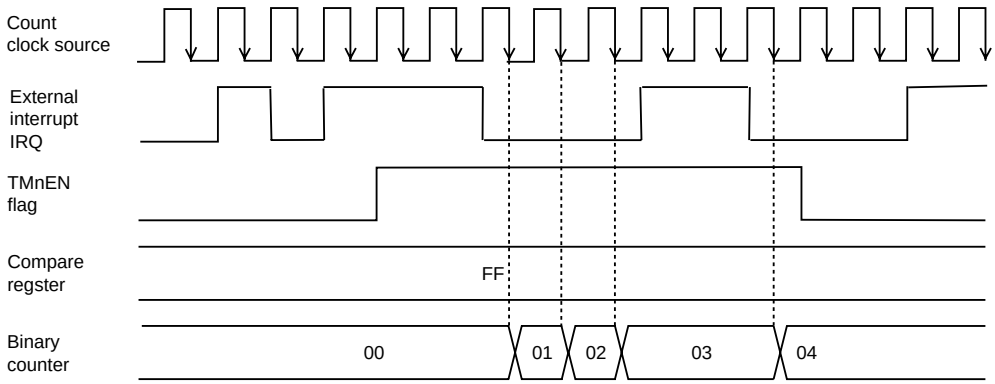


Figure 6-9-1 Count Timing at Measurement of Simple Pulse Width (Timer 0, Timer 2)

When the input signal of the external interrupt pin for simple pulse width measurement is "L" at TMnEN flag operation is ("1"), timer counts up.

6-9-2 Setup Example

■Set up Example of Simple Pulse Width Measurement by 8-bit Timer (Timers 0, and 2)
The pulse width of 'L" period of the external interrupt 0 (IRQ0) input signal is measured by timer 0. The clock source of timer 0 is selected to fosc.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop timer 0 counting.
(2) Set the pulse width measurement operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 1	(2) Set the TM0PWM flag of the TM0MD register to "0" and TM0MOD flag to "1" to enable the timer operation during "L" period to be measured.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(3) Set the clock source to fosc by the TM0CK2-0 flag of the TM0MD register.
(4) Set the compare register. TM0OC (X'3F52') = x'FF'	(4) Set the timer 0 compare register (TM0OC) to the bigger value than the cycle of fosc / "L" period of measured pulse width. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(5) Set the interrupt level IRQ0ICR (x'3FE2') bp7-6 :IRQ0LV1-0 = 10	(5) Set the interrupt level by the IRQ0LV1-0 flag of the external interrupt 0 control register (IRQ0ICR). If interrupt request flag is already set, clear all interrupt request flags. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]
(6) Set the interrupt valid edge. IRQ0ICR (x'3FE2') bp5 :REDG0 = 1	(6) Set the REDG0 flag of the IRQ0ICR register to "1" to specify the interrupt valid edge to the rising edge.

Setup Procedure	Description
(7) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 :IRQ0IE = 1	(7) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(8) Enable the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to enable timer 0 operation.

TM0BC starts to count up with negative edge of the external interrupt 0 (IRQ0) input as a trigger. Timer 0 continues to count up during "L" period of IRQ0 input, then stop the counting with positive edge of IRQ0 input as a trigger. At the same time, reading the value of TM0BC by interrupt handling can detects "L" period.

6-10 Cascade Connection

6-10-1 Operation

Cascading timers 0 and 1, or timer 2 and 3 forms a 16-bit timer.

■8-bit Timer Cascade Connection Operation (Timer 0 + Timer 1, Timer 2 + Timer 3)
Timer 0 and timer 1, or timer 2 and timer 3 are combined to be a 16-bit timer. Cascading timer is operated at clock source of timer 0 or timer 2 which are lower 8 bits.

Table 6-10-1 Timer Functions at Cascade Connection

	Timer 0 + Timer 1 (16 bit)	Timer 2 + Timer 3 (16 bit)
Interrupt source	TM1IRQ	TM3IRQ
Timer operation	√	√
Event count	√ (TM0IO input)	√ (TM2IO input)
Timer pulse output	√ (TM1IO output)	√ (TM3IO output)
PWM output	-	-
Synchronous output	√	-
Serial transfer clock output	-	√ (TM3IO output)
Pulse width measurement	√	√
Remote control carrier output	-	√
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM2IO input
fosc : Machine clock (High frequency oscillation) fx : Machine clock (Low frequency oscillation) fs : System clock [☞Chapter 2 2-5 Clock Switching]		

At cascade connection, the binary counter and the compare register are operated as a 16 bit register. At operation, set the TMnEN flag of the upper and lower 8-bit timers to "1" to be operated. Also, select the clock source by the lower 8-bit timer.
Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 0 and timer 1 are used in cascade connection, timer 1 is used as an interrupt request flag. Timer pulse output of timer 0 is "L" fixed output.
An interrupt request of timer 0 is not generated, but the timer 0 interrupt should be disabled.

When timer 2 and timer 3 are used in cascade connection, timer 3 is used as an interrupt request flag. Timer pulse output of timer 2 is "L" fixed output.
An interrupt request of timer 2 is not generated, but the timer 2 interrupt should be disabled.

If you want to clear the binary counter by rewrite of the compare register value during cascade connection, set the TMnEN flag of the mode register of both upper / lower 8-bit timers to "0" to stop counting before rewrite.

6-10-2 Setup Example

■Cascade Connection Timer Setup Example (Timer 0 + Timer 1, Timer 2 + Timer 3)
Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 0 and timer 1, as a 16-bit timer is shown. An interrupt is generated 2500 times every 1 ms by selecting source clock to fs/4 (fosx=20 MHz at operation).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0 TM1MD (x'3F55') bp3 :TM1EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0", the TM1EN flag of the timer 1 mode register to "0" to stop timer 0 and timer 1 counting.
(2) Select the normal lower timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set both of the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer 0 operation.
(3) Set the cascade connection. TM1MD (x'3F55') bp4 :TM1CAS = 1	(3) Set the TM1CAS flag of the TM1MD register to "1" to connect timer 1 and timer 0 in cascade connection.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(4) Set the clock source to prescaler output by the TM0CK2-0 flag of the TM0MD register.
(5) Select the prescaler output and enable counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0= 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(5) Set the prescaler output to fs/4 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(6) Set the interrupt generation cycle. TMnOC(x'3F53', x'3F52')=x'09C3'	(6) Set the timer 1 compare register + timer 0 compare register (TM1OC + TM0OC) to the interrupt generation cycle (x'09C3' : 2500 cycles - 1). At that time, timer 1 binary counter + timer 0 binary counter (TM1BC + TM0BC) are initialized to x'0000'.

Setup Procedure	Description
(7) Disable the lower timer interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 0	(7) Set the TM0IE flag of the timer 0 interrupt control register (TM0ICR) to "0" to disable the interrupt.
(8) Set the level of the upper timer interrupt. TM1ICR (x'3FEA') bp7-6 :TM1LV1-0 = 10	(8) Set the interrupt level by the TM1LV1-0 flag of the timer 1 interrupt control register (TM1ICR). If any interrupt request flag may be already set, clear all request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the upper timer interrupt. TM1ICR (x'3FEA') bp1 :TM1IE = 1	(9) Set the TM1IE flag of the TM1ICR register to "1" to enable the interrupt.
(10) Start the upper timer operation. TM1MD (x'3F55') bp3 :TM1EN = 1	(10) Set the TM1EN flag of the TM1MD register to "1" to start timer 1.
(11) Start the lower timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(11) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM1BC + TM0BC counts up from x'0000' as a 16-bit timer. When TM1BC + TM0BC reaches the set value of TM1OC + TM0OC register, the timer 1 interrupt request flag is set at the next count clock, and the value of TM1BC + TM0BC becomes x'0000' and restarts count up.

Use a 16-bit access instruction to set the (TM1OC + TM0OC) register.

Start the upper timer operation before the lower timer operation.

6-11 Remote Control Carrier Output

6-11-1 Operation

Carrier pulse for remote control can be generated.

■Operation of Remote Control Carrier Output (Timer 0, Timer 3)
Remote control carrier pulse is generated with output signal of timer 0 or timer 3. Duty rate is selected from 1/2, 1/3. RMOUT (P10) outputs remote control carrier output signal.

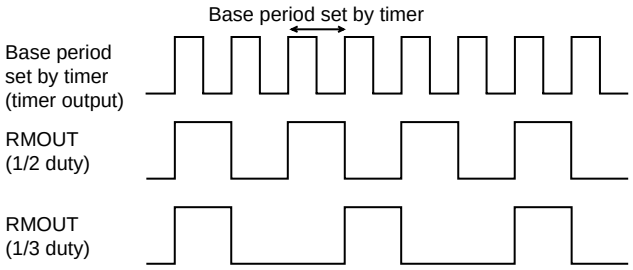


Figure 6-11-1 Duty Rate of Remote Control Carrier Output Signal

■Count Timing of Remote Control Carrier Output (Timer 0, Timer 3)

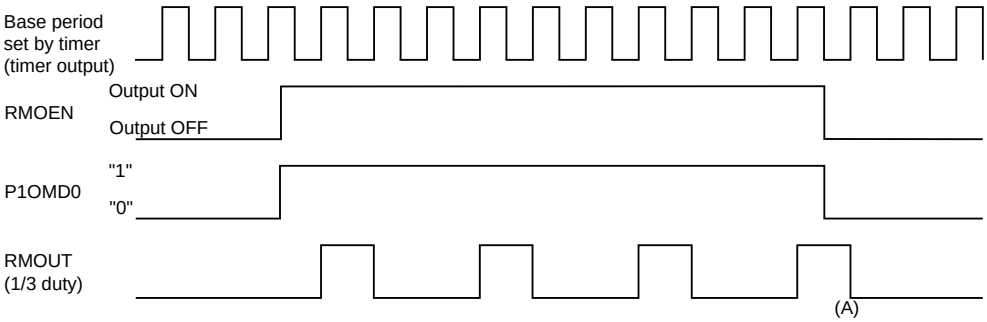


Figure 6-11-2 Count Timing of Remote Control Carrier Output Function (Timer 0, Timer 3)

(A) Even if the RMOEN flag is off when the carrier output is high, the carrier waveform is held by the synchronous circuit.

When the RMOEN flag is switched to on, set the P1OMD0 flag to "1". When it is switched to off, set it to "0".

When the RMOEN flag is changed, do not change the base cycle and its duty at the same time. If they are changed at the same time, the carrier wave form is not output properly.

6-11-2 Setup Example

■Remote Control Carrier Output Setup Example (Timer 0, Timer 3)
Here is the setting example that the RMOUT pin outputs the 1/3 duty carrier pulse signal with "H" period of 36.7 kHz, by using timer 0. The source clock of timer 0 is set to fosc (8 MHz at operation).
An example setup procedure, with a description of each step is shown below.

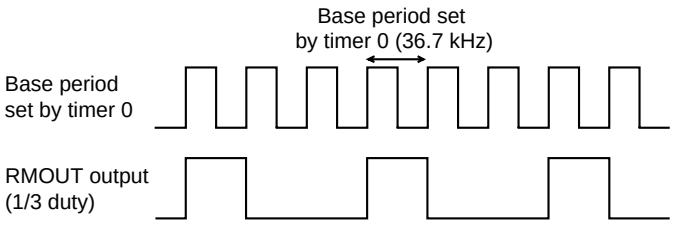


Figure 6-11-3 Output Wave Form of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 0	(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR) to "0" to disable the remote control carrier output.
(2) Select the base cycle setting timer. RMCTR (x'3F6E') bp0 : RMBTMS = 0	(2) Set the RMBTMS flag of the RMCTR register to "0" to set the timer as a base cycle setting timer.
(3) Select the carrier output duty. RMCTR (x'3F6E') bp1 : RMDTY0 = 1	(3) Set the RMDTY0 flag of the RMCTR register to "1" to select 1/3 duty.
(4) Stop the counter. TM0MD (x'3F54') bp3 : TM0EN = 0	(4) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop the timer 0 counting.
(5) Set the remote control carrier output of the special function pin. P1OMD (x'3F2F') bp0 : P1OMD0 = 1 P1DIR (x'3F31') bp0 : P1DIR0 = 1 RMCTR (x'3F6E') bp4 :TM0RM = 1	(5) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin as a special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for output mode. Set the TM0RM flag of the RMCTR register to "1" to select the remote control carrier output.

Setup Procedure	Description
(6) Select the normal timer operation. TM0MD (x'3F54') bp4 : TM0PWM = 0 bp5 : TM0MOD = 0	(6) Set both of the TM0MOD flag and TM0PWM flag of the TM0MD register to "0" to select normal timer operation.
(7) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(7) Select fosc to clock source by the TM0CK2-0 flag of the TM0MD register.
(8) Set the base cycle of remote control carrier. TM0OC (x'3F52') = x'6C'	(8) Set the base cycle of remote control carrier by writing x'6C' to the timer 0 compare register (TM0OC). The set value should be (8 MHz/ 73.4 kHz) - 1 = 108(x'6C') 8 MHz is divided to be 73.4 kHz, 2 times 36.7 kHz.
(9) Start the timer operation. TM0MD (x'3F54') bp3 : TM0EN = 1	(9) Set the TM0EN flag of the TM0MD register to "1" to stop the timer 0 counting.
(10) Enable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 1	(10) Set the RMOEN flag of the RMCTR register to "1" to enable the remote control carrier output.

TM0BC counts up from x'00'. Timer 0 outputs the base cycle pulse set in TM0OC. Then, the 1/3 duty remote control carrier pulse signal is output. If the RMOEN flag of the RMCTR register is "0", the remote control carrier pulse signal output is stopped.

Chapter 7 16-bit Timers

7

7-1 Overview

This LSI contains two general-purpose 16-bit timers (Timer 7,Timer 8). The timer 7 is high-efficiency 16-bit timer and the timer 8 is standard 16-bit timer. The high efficiency 16-bit timer is the timer counter extended from standard 16-bit timer and is upwardly compatible with standard 16-bit timer. The 16-bit timer has compare register with double buffer. High precision 16-bit timer has 2 sets of compare registers with double buffering.

7-1-1 Functions

Table 7-1-1 shows the functions of timer 7 and timer 8.

Table 7-1-1 16-bit Timer Functions

	Timer 7 (High precision 16-bit timer)	Timer 8 (Standard 16-bit timer)
Interrupt source	TM7IRQ1, TM7IRQ2	TM8IRQ1
Timer operation	√	√
Event count	√	√
Timer pulse output	√	√
PWM output (duty is variable)	√	√
High precision PWM output (duty and cycle are variable)	√	–
Synchronous output	√	–
Capture function	√	√
Pulse width measurement	√	√
32-bit cascade connection (Timer cycle, Event count. Standard PWM output, High precision PWM output capture)	√	
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM8IO input TM8IO input/2 TM8IO input/4 TM8IO input/16
fosc : Machine clock (High frequency oscillation) fx: Machine clock (Low frequency oscillation) fs : System clock * Synchronous output can not be used at the processor mode.		

7-1-2 Block Diagram

■Timer 7 Block Diagram

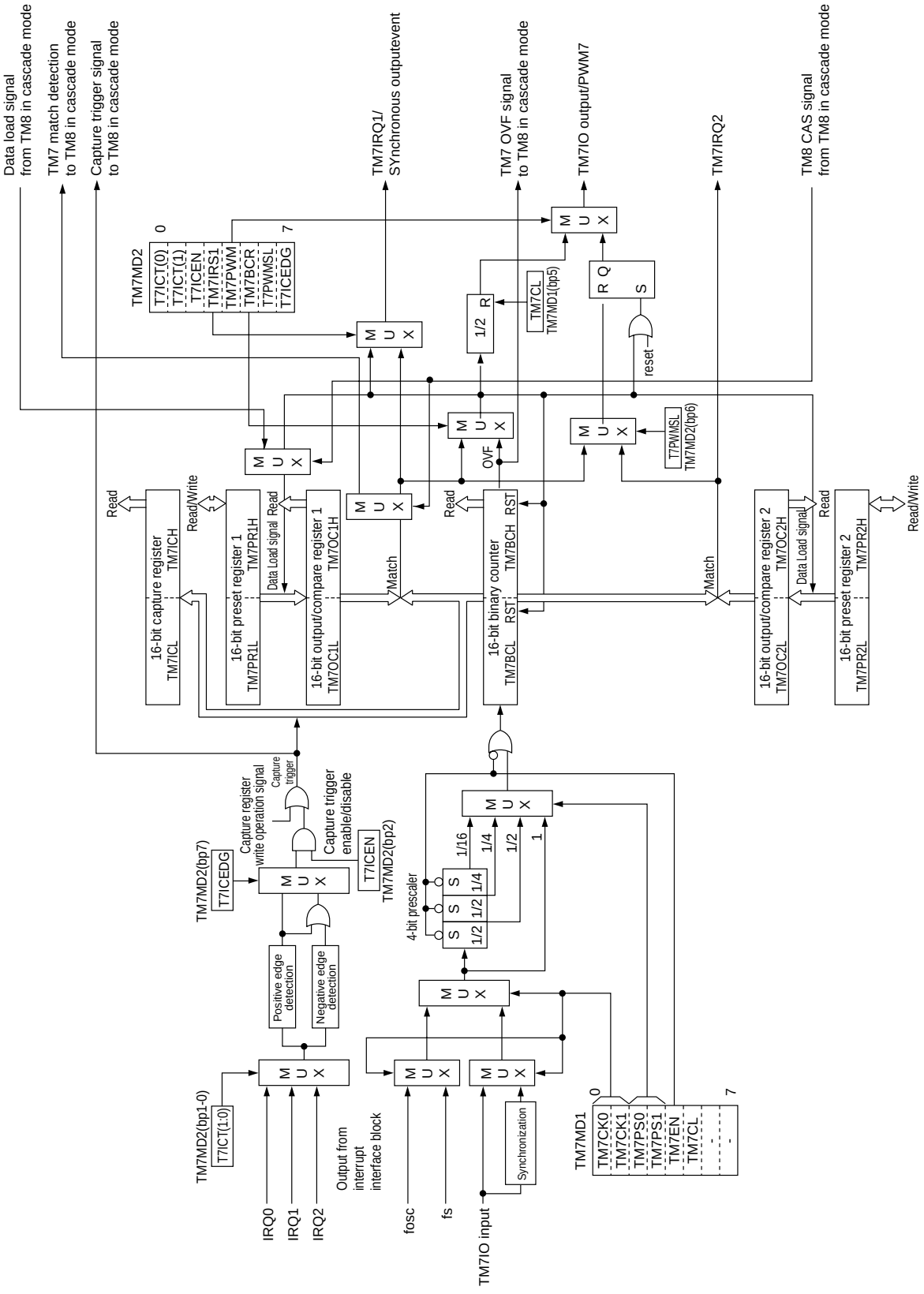


Figure 7-1-1 Timer 7 Block Diagram

■Timer 8 Block Diagram

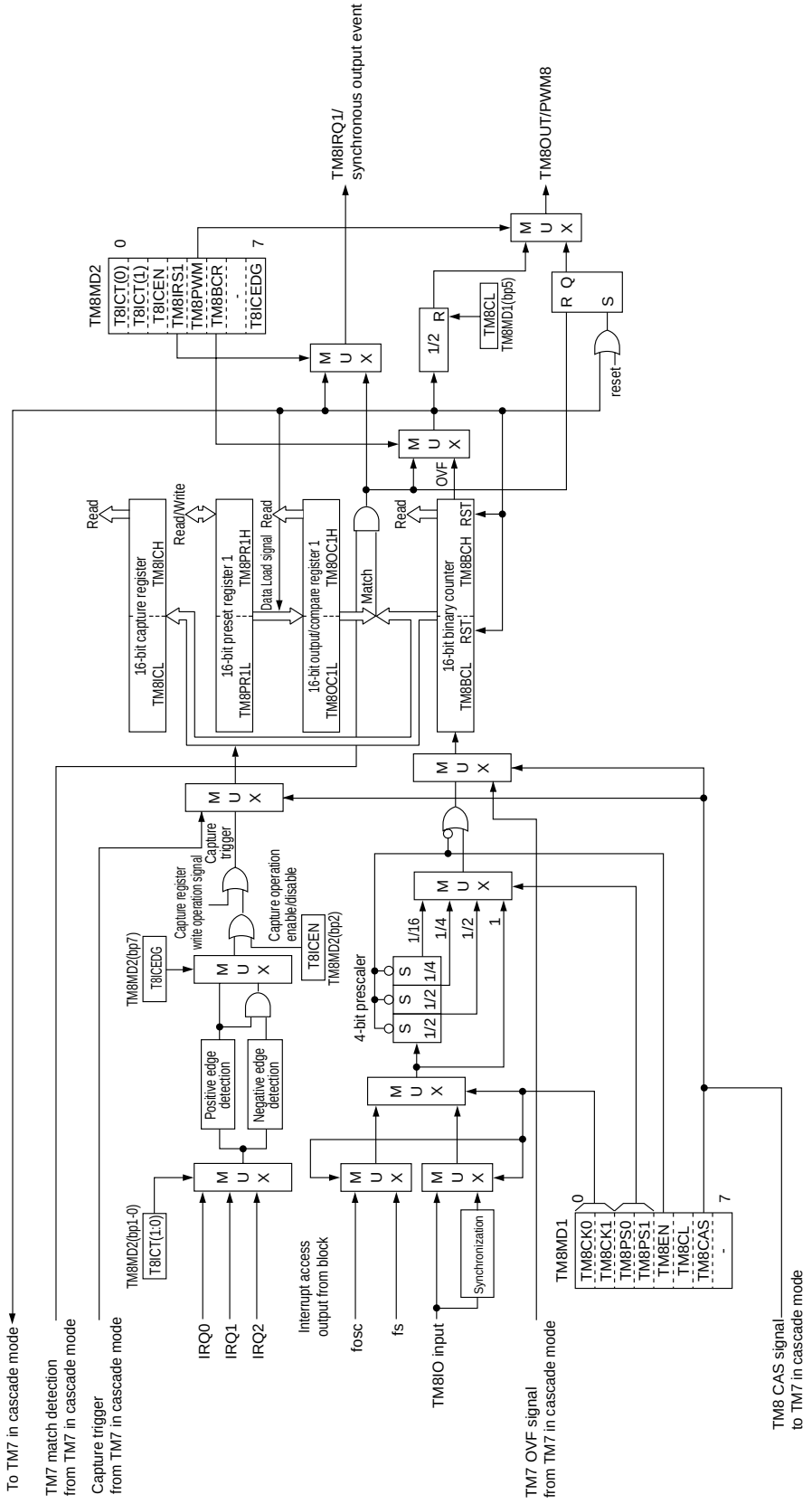


Figure 7-1-2 Timer 8 Block Diagram

7-2 Control Registers

Timer 7 contains the binary counter (TM7BC), the compare register 1 (TM7OC1) with its double buffer preset register 1 (TM7PR1), the compare register 2 (TM7OC2) with its double buffer preset register 2 (TM7PR2) and the input capture register (TM7IC). The mode register 1 (TM7MD1), the mode register 2 (TM7MD2) and control timer 7.Timer 8 contains the binary counter (TM8BC), the compare register 1 (TM8OC1) with its double buffer preset register 1 (TM8PR1) and the input capture register (TM8IC). The mode register 1 (TM8MD1), the mode register 2 (TM8MD2) and control timer 8.

7-2-1 Registers

Table 7-2-1 shows the registers that control timer 7.

Table 7-2-1 16-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 7	TM7BCL	X'03F70'	R	Timer 7 binary counter (lower 8 bits)	VII - 8
	TM7BCH	X'03F71'	R	Timer 7 binary counter (upper 8 bits)	VII - 8
	TM7OC1L	X'03F72'	R	Timer 7 compare register 1 (lower 8 bits)	VII - 6
	TM7OC1H	X'03F73'	R	Timer 7 compare register 1 (upper 8 bits)	VII - 6
	TM7PR1L	X'03F74'	R/W	Timer 7 preset register 1 (lower 8 bits)	VII - 7
	TM7PR1H	X'03F75'	R/W	Timer 7 presets register 1 (upper 8 bits)	VII - 7
	TM7ICL	X'03F76'	R	Timer 7 capture register (lower 8 bits)	VII - 9
	TM7ICH	X'03F77'	R	Timer 7 capture register (upper 8 bits)	VII - 9
	TM7MD1	X'03F78'	R/W	Timer 7 mode register 1	VII - 10
	TM7MD2	X'03F79'	R/W	Timer 7 mode register 2	VII - 11
	TM7OC2L	X'03F7A'	R	Timer 7 compare register 2 (lower 8 bits)	VII - 6
	TM7OC2H	X'03F7B'	R	Timer 7 compare register 2 (upper 8 bits)	VII - 6
	TM7PR2L	X'03F7C'	R/W	Timer 7 preset register 2 (lower 8 bits)	VII - 7
	TM7PR2H	X'03F7D'	R/W	Timer 7 preset register 2 (upper 8 bits)	VII - 7
	TM7ICR	X'03FF1'	R/W	Timer 7 interrupt control register	III - 27
	T7OC2ICR	X'03FF2'	R/W	Timer 7 compare register 2 match interrupt control register	III - 28
	P1OMD	X'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	X'03F31'	R/W	Port 1 direction control register	IV - 11
Timer 8	TM8BCL	X'03F80'	R	Timer 8 binary counter (lower 8 bits)	VII - 8
	TM8BCH	X'03F81'	R	Timer 8 binary counter (upper 8 bits)	VII - 8
	TM8OC1L	X'03F82'	R	Timer 8 compare register 1 (lower 8 bits)	VII - 6
	TM8OC1H	X'03F83'	R	Timer 8 compare register 1 (upper 8 bits)	VII - 6
	TM8PR1L	X'03F84'	R/W	Timer 8 preset register 1 (lower 8 bits)	VII - 7
	TM8PR1H	X'03F85'	R/W	Timer 8 preset register 1 (upper 8 bits)	VII - 7
	TM8ICL	X'03F86'	R	Timer 8 capture register 1 (lower 8 bits)	VII - 9
	TM8ICH	X'03F87'	R	Timer 8 capture register 1 (upper 8 bits)	VII - 9
	TM8MD1	X'03F88'	R/W	Timer 8 mode register 1	VII - 12
	TM8MD2	X'03F89'	R/W	Timer 8 mode register 2	VII - 13
	TM8ICR	X'03FF3'	R/W	Timer 8 interrupt control register	VII - 29
	P1OMD	X'03F2F'	R/W	Port 1 output mode register	IV - 12
	P1DIR	X'03F31'	R/W	Port 1 direction control register	IV - 11

R/W : Readable/Writable
R : Readable only

7-2-2 Programmable Timer Registers

Timer 7 and Timer 8 each have a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of compare register and binary counter. Comparative value written to the preset register in advance is loaded to the register.

■Timer 7 Compare Register 1 (TM7OC1)

	7	6	5	4	3	2	1	0	
TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	(At reset : X X X X X X X X)

Figure 7-2-1 Timer 7 Compare Register 1 Lower 8 bits (TM7OC1L : x'03F72', R)

	7	6	5	4	3	2	1	0	
TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	(At reset : X X X X X X X X)

Figure 7-2-2 Timer 7 Compare Register 1 Upper 8 bits (TM7OC1H : x'03F73', R)

■Timer 7 Compare Register 2 (TM7OC2)

	7	6	5	4	3	2	1	0	
TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	(At reset : X X X X X X X X)

Figure 7-2-3 Timer 7 Compare Register 2 Lower 8 bits (TM7OC2L : x'03F7A', R)

	7	6	5	4	3	2	1	0	
TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	(At reset : X X X X X X X X)

Figure 7-2-4 Timer 7 Compare Register 2 Upper 8 bits (TM7OC2H : x'03F7B', R)

■Timer 8 Compare Register 1 (TM8OC1)

	7	6	5	4	3	2	1	0	
TM8OC1L	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0	(At reset : X X X X X X X X)

Figure 7-2-5 Timer 8 Compare Register 1 Lower 8 bits (TM8OC1L : x'03F82', R)

	7	6	5	4	3	2	1	0	
TM8OC1H	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0	(At reset : X X X X X X X X)

Figure 7-2-6 Timer 8 Compare Register 1 Upper 8 bits (TM8OC1H : x'03F83', R)

The timer 7 preset registers 1 and 2 are buffer registers of the compare registers 1, 2 of timer 7. If the set value is written to the timer 7 preset registers 1, 2 when the counting is stopped, the same set value is loaded to timer 7 compare registers 1, 2. If the set value is written to timer 7 preset registers 1, 2 during counting, the set value of timer 7 preset registers 1, 2 is loaded to timer 7 compare registers 1, 2 at the timing that the timer 7 binary counters are cleared.

■Timer 7 Preset Register 1 (TM7PR1)

	7	6	5	4	3	2	1	0	
TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	(At reset : X X X X X X X X)

Figure 7-2-7 Timer 7 Preset Register 1 Lower 8 bits (TM7PR1L : x'03F74', R/W)

	7	6	5	4	3	2	1	0	
TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	(At reset : X X X X X X X X)

Figure 7-2-8 Timer 7 Preset Register 1 Upper 8 bits (TM7PR1H : x'03F75', R/W)

■Timer 7 Preset Register 2 (TM7PR2)

	7	6	5	4	3	2	1	0	
TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	(At reset : X X X X X X X X)

Figure 7-2-9 Timer 7 Preset Register 2 Lower 8 bits (TM7PR2L : x'03F7C', R/W)

	7	6	5	4	3	2	1	0	
TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	(At reset : X X X X X X X X)

Figure 7-2-10 Timer 7 Preset Register 2 Upper 8 bits (TM7PR2H : x'03F7D', R/W)

■Timer 8 Preset Register 1 (TM8PR1)

	7	6	5	4	3	2	1	0	
TM8PR1L	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR13L	TM8PR1L2	TM8PR1L1	TM8PR1L0	(At reset : X X X X X X X X)

Figure 7-2-11 Timer 8 Preset Register 1 Lower 8 bits (TM8PR1L : x'03F84', R/W)

	7	6	5	4	3	2	1	0	
TM8PR1H	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0	(At reset : X X X X X X X X)

Figure 7-2-12 Timer 8 Preset Register 1 Upper 8 bits (TM8PR1H : x'03F85', R/W)

Binary counter is a 16-bit up counter. If any data is written to a preset register when the counting is stopped, the binary counter is cleared to x'0000'.

■Timer 7 Binary Counter (TM7BC)

	7	6	5	4	3	2	1	0	
TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	(At reset : X X X X X X X X)

Figure 7-2-13 Timer 7 Binary Counter Lower 8 bits (TM7BCL : x'03F70', R)

	7	6	5	4	3	2	1	0	
TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	(At reset : X X X X X X X X)

Figure 7-2-14 Timer 7 Binary Counter Upper 8 bits (TM7BCH : x'03F71', R)

■Timer 8 Binary Counter (TM8BC)

	7	6	5	4	3	2	1	0	
TM8BCL	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0	(At reset : X X X X X X X X)

Figure 7-2-15 Timer 8 Binary Counter Lower 8 bits (TM8BCL : x'03F80', R)

	7	6	5	4	3	2	1	0	
TM8BCH	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0	(At reset : X X X X X X X X)

Figure 7-2-16 Timer 8 Binary Counter Upper 8 bits (TM8BCH : x'03F81', R)

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■Timer 7 Input Capture Register (TM7IC)

	7	6	5	4	3	2	1	0	
TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	(At reset : X X X X X X X X)

Figure 7-2-17 Timer 7 Input Capture Register Lower 8 bits (TM7ICL : x'03F76', R)

	7	6	5	4	3	2	1	0	
TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	(At reset : X X X X X X X X)

Figure 7-2-18 Timer 7 Input Capture Register Upper 8 bits (TM7ICH : x'03F77', R)

■Timer 8 Input Capture Register (TM8IC)

	7	6	5	4	3	2	1	0	
TM8ICL	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0	(At reset : X X X X X X X X)

Figure 7-2-19 Timer 8 Input Capture Register Lower 8 bits (TM8ICL : x'03F86', R)

	7	6	5	4	3	2	1	0	
TM8ICH	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0	(At reset : X X X X X X X X)

Figure 7-2-20 Timer 8 Input Capture Register Upper 8 bits (TM8ICH : x'03F87', R)

7-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 7.

■Timer 7 Mode Register 1 (TM7MD1)

	7	6	5	4	3	2	1	0
TM7MD1	RESERVED	RESERVED	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0

(At reset : 0 0 1 0 0 0 0 0)

TM7CK1	TM7CK0	Clock source selection
0	0	fosc
	1	fs
1	0	TM7IO input
	1	Synchronous TM7IO input

TM7PS1	TM7PS0	Count clock selection
0	0	1/1 of clock
	1	1/2 of clock
1	0	1/4 of clock
	1	1/16 of clock

TM7EN	Timer 7 count control
0	Halt the count
1	Operate the count

TM7CL	Timer output reset control
0	Operate timer output
1	Disable timer output (reset)

RESERVED	Set always "0".

Figure 7-2-21 Timer 7 Mode Register 1 (TM7MD1 : x'03F78', R/W)

■Timer 7 Mode Register 2 (TM7MD2)

	7	6	5	4	3	2	1	0
TM7MD2	T7ICEDG	T7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0

(At reset : 0 0 0 0 0 0 0 0)

T7ICT1	T7ICT0	Capture trigger selection
0	0	IRQ0 (External interrupt 0)
	1	IRQ1 (External interrupt 1)
1	0	IRQ2 (External interrupt 2)
	1	Unavailable

T7ICEN	Input capture operation enable flag
0	Disable capture operation
1	Enable capture operation

TM7IRS1	Timer 7 interrupt source selection
0	Counter clear
1	Match of BC and OC1

TM7PWM	Timer output waveform selection
0	Timer output
1	PWM output

TM7BCR	Timer 7 counter clear source selection
0	Full count OVF
1	Match of BC and OC1

T7PWMSL	PWM mode selection
0	Set duty by OC1
1	Set duty by OC2

T7ICEDG	Capture trigger edge selection
0	Both edges selection
1	Specified edge selection

Figure 7-2-22 Timer 7 Mode Register 2 (TM7MD2 : x'03F79', R/W)

■Timer 8 Mode Register 1 (TM8MD1)

	7	6	5	4	3	2	1	0
TM8MD1	RESERVED	TM8CAS	TM8CL	TM8EN	TM8PS1	TM8PS0	TM8CK1	TM8CK0

(At reset : 0 0 1 0 0 0 0 0)

TM8CK1	TM8CK0	Clock source selection
0	0	fosc
	1	fs
1	0	TM8IO input
	1	Synchronous TM8IO input

TM8PS1	TM8PS0	Count clock selection
0	0	1/1 of clock
	1	1/2 of clock
1	0	1/4 of clock
	1	1/16 of clock

TM8EN	Timer 8 count control
0	Halt the count
1	Operate the count

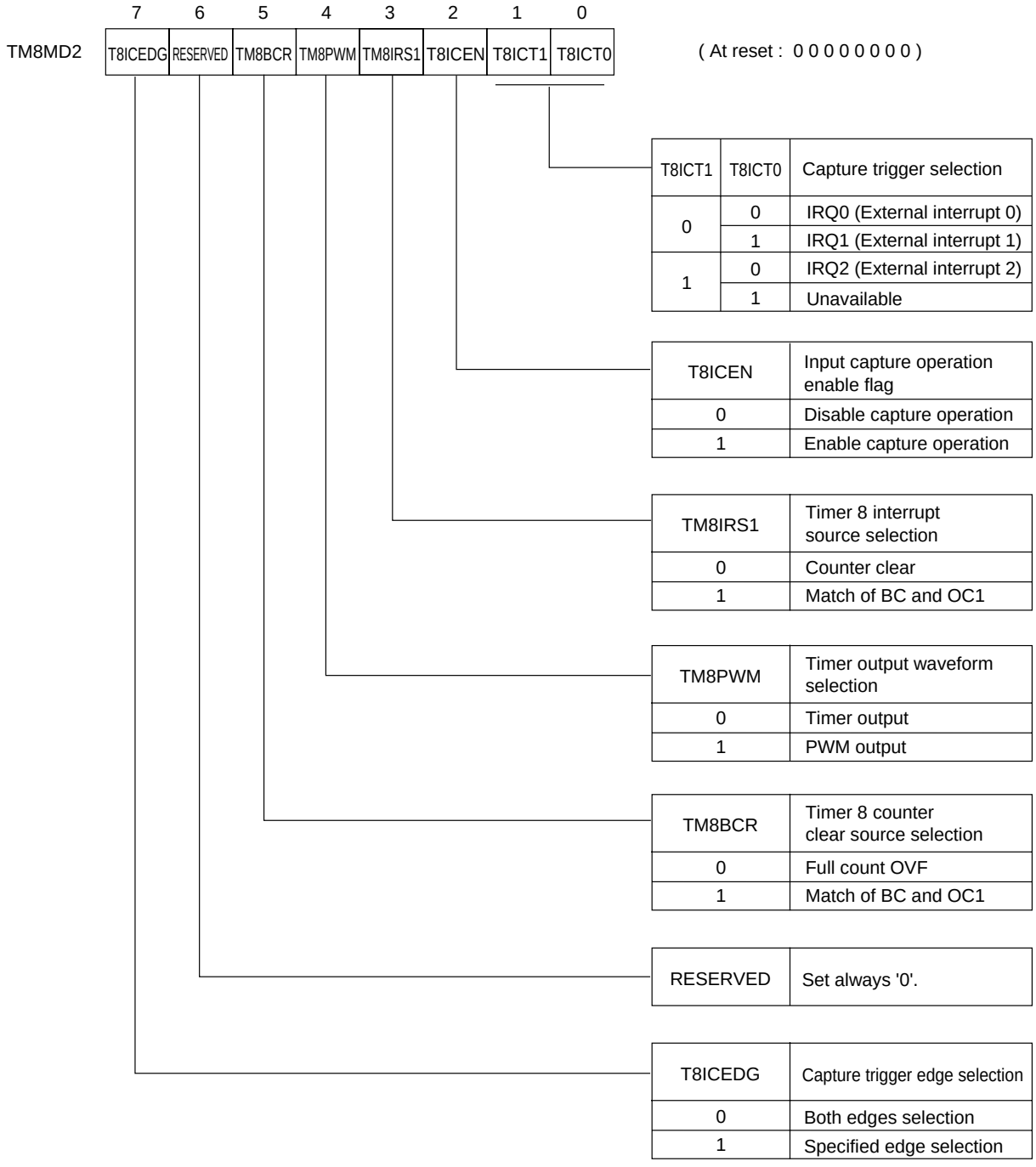
TM8CL	Timer output reset control
0	Operate timer output
1	Reset

TM8CAS	Timer 7, 8 cascade connection control
0	Timer 7, 8 individual operation
1	Timer 7, 8 cascade connection operation

RESERVED	Set always '0'.

Figure 7-2-23 Timer 8 Mode Register 1 (TM8MD1 : x'03F88', R/W)

■Timer 8 Mode Register 2 (TM8MD2)



T8ICT1	T8ICT0	Capture trigger selection
0	0	IRQ0 (External interrupt 0)
	1	IRQ1 (External interrupt 1)
1	0	IRQ2 (External interrupt 2)
	1	Unavailable

T8ICEN	Input capture operation enable flag
0	Disable capture operation
1	Enable capture operation

TM8IRS1	Timer 8 interrupt source selection
0	Counter clear
1	Match of BC and OC1

TM8PWM	Timer output waveform selection
0	Timer output
1	PWM output

TM8BCR	Timer 8 counter clear source selection
0	Full count OVF
1	Match of BC and OC1

RESERVED	Set always '0'.

T8ICEDG	Capture trigger edge selection
0	Both edges selection
1	Specified edge selection

Figure 7-2-24 Timer 8 Mode Register 2 (TM8MD2 : x'03F89', R/W)

7-3 Operation

7-3-1 Operation

The timer operation can constantly generate interrupts.

■16-bit Timer Operation (Timer 7,Timer 8)
The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register 1 (TMnOC1), in advance. When the binary counter (TMnBC) reaches the set value of the compare register 1, an interrupt is generated at the next count clock. There are 2 sources to be selected to clear the binary counter; the TMnOC1 compare match and the full count overflow. After the binary counter is cleared, the counting up is restarted from x'0000'.

Table 7-3-1 16-bit Timer Interrupt Source and Binary Counter Clear Source (Timer 7, Timer 8)

TMnMD2 register		Interrupt source	Binary counter clear source
TMnIRS1 flag	TMnBCR flag		
1	1	TM7nOC1 compare match	TMnOC1 compare match
0	1	TMnOC1 compare match	TMnOC1 compare match
1	0	TMnOC1 compare match	full count overflow
0	0	full count overflow	full count overflow

Timer 7 can generate another set of an independent interrupt (timer 7 compare register 2 match interrupt) by the set value of the timer 7 compare registers (TM7OC2). At the time of the interrupt, the binary counter is cleared as the above setup.

The compare register is double buffer type. So, when the value of the preset register is changed during the counting, the changed value is stored to the compare register when the binary counter is cleared. This function can change the compare register value constantly, without disturbing the cycle during timer operation (Reload function).

When the CPU reads the 16-bit binary counter (TMnBC), the read data is handled in 8-bits units even if it is a 16-bit MOVW instruction. As a result, it will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting operation.

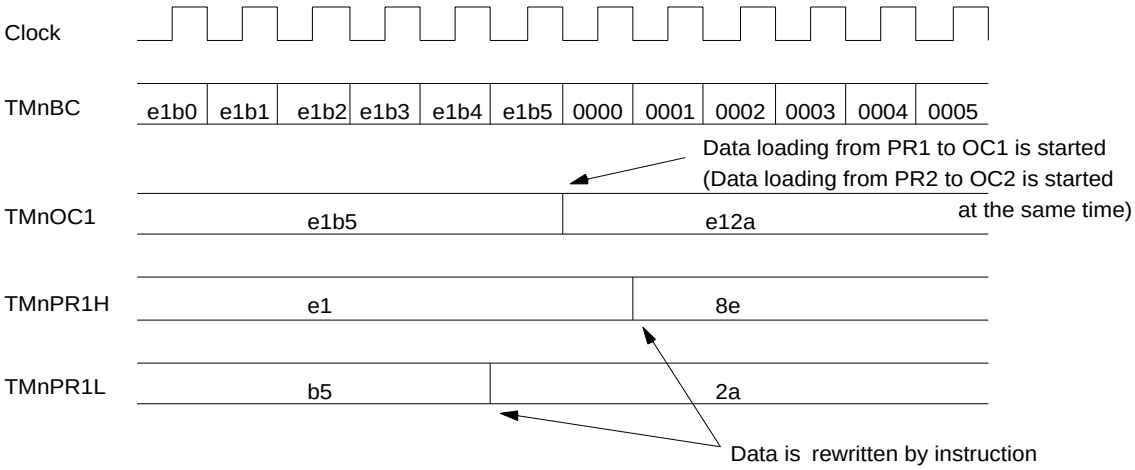
To read the correct value of the 16-bit counting (TM7BC), use the writing program function to the input capture register (TM7IC). By writing to the TM7IC, the counting data of TM7BC can be stored to TM7IC to read out the correct counting value during timer operation.

[☞ Chapter 7-9-1. Operation (p.VII-38)]

When a data is written to 16-bit timer preset register (TM7PR1, TM7PR2), it is recognized as a 8-bit unit data inside LSI even if it is a 16-bit access MOVW instruction. After lower 8 bits of preset register is written, if data loading from preset register to compare register is started before the upper 8 bits is written, data which is not rewritten is loaded to the upper 8 bits and rewritten data is loaded to the lower 8 bits.
Therefore, writing data to the preset register (TM7PR1, TM7PR2) need to be completed before data loading from the preset register to the compare register is started.

Shown below is timing chart of TM7PR1 and TM7OC1 data rewriting and the data loading. When data is written to TM7PR2 wrong data could be loaded due to the same problem.

TM7BC and TM7OC1 compare match and load timing of TM7PR1



Data e12a is loaded to OC1 as PR1rewrting (e1b5 -> 8e2a) and loading to OC1 are operated at the same time.

Table 7-3-2 shows the clock source that can be selected.

Table 7-3-2 Clock Source at Timer Operation (Timer 7, Timer 8)

Clock source	1 count time
fosc	50 ns
fosc/2	100 ns
fosc/4	200 ns
fosc/16	800 ns
fs	100 ns
fs/2	200 ns
fs/4	400 ns
fs/16	1.6 µs
as fosc = 20 MHz, fs = fosc/2 = 10 MHz	

■Count Timing of Timer Operation (Timer 7, Timer 8)

The binary counter counts up with the selected clock source as the count clock.

The basic operation of whole 16-bit timer functions is as bellow.

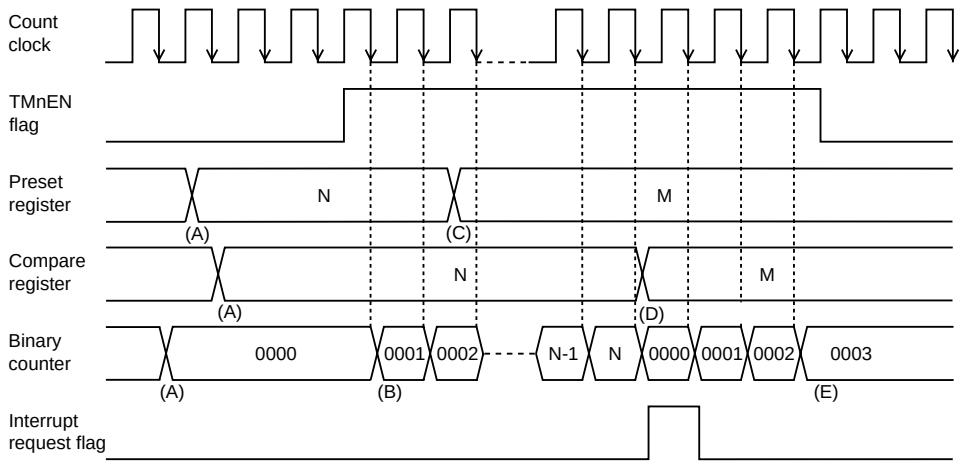


Figure 7-3-1 Count Timing of Timer Operation (Timer 7,Timer 8)

(A) When a data is written to the preset register while the TMnEN flag is stopped ("0"), the same value is loaded during the writing cycle and the binary counter is cleared to x'0000'.

(B) When TMnEN flag is ("1"), the binary counter starts counting. The counting starts at the falling edge of the count clock.

(C) Even if the preset register is rewritten when the TMnEN flag is ("1"), the binary counter is not changed.

(D) When the binary counter reaches value of compare register 1, the set value of the preset register is loaded to the compare register at the next count clock. And the interrupt request flag is set at the next count clock, and the binary counter is cleared to x'0000' to restart counting up.

(E) When the TMnEN flag is ("0"), the binary counter is stopped.

When the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, and the binary counter is cleared. So set the compare register as;
(the set value of the compare register) = (the counts till the interrupt generation - 1)

When timer n compare register 2 match interrupt is generated and TMnOC1 compare match is selected as a binary counter clear source, the set value of the compare register 2 should be smaller than the set value of the compare register 1.

On the interrupt service routine, clear the timer interrupt request flag before the timer is started.

At TMnOC=x'0000', x'0001', the timer n interrupt request generation has the same waveform.

When more than 2 waits is set at access to the special register area by the IOW1, IOW0 flag of the MEMCTR register, write the same value 2 times at setup of the preset register when the timer is stopped. When 1 wait or no wait is set, there is no need to do this.
(This is for the functions of a 16-bit timer.)
[☞ Chapter 2 2-3-2. Control Registers]

7-3-2 Setup Example

■Timer Operation Setup Example (Timer 7,Timer 8)
Timer 7 generates an interrupt constantly for timer function. Fosc/2 (fosc=20 MHz at operation) is selected as a clock source to generate an interrupt every 1000 cycles (100 µs).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the timer clear source. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a binary counter clear source.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(3) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also select 1/2 fosc as a count clock source by TM7PS1-0 flag.
(4) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'03E7	(4) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The cycle is 1000. The set value should be 1000-1=999(x'03E7'). At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(5) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 : TM7LV1-0 = 10	(5) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag may be already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(6) Set the TM7IE flag of the TM7ICR register to "1" to enable the interrupt.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78) bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. When TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock and the TM7BC becomes x'0000' and counts up, again.

When the TMnEN flag of the TMnMD register is changed with other bits, the binary counter may count up by switching operation.

7-4 16-bit Event Count

7-4-1 Operation

Event count operation has 2 types; TMnIO input and synchronous TMnIO input. These can be selected as the count clock. Each type can select 1/1, 1/2, 1/4, 1/16 as a count clock source. Timer 7 can also select the count edge (falling or both edges).

■16-bit Event Count Operation (Timer 7, Timer 8)
The binary counter (TMnBC) counts the external signal input to the TMnIO pin. If the binary counter reaches the set value of the compare register (TMnOC), an interrupt can be generated at the next count clock.

Table 7-4-1 Event Count Input Clock Source

	Timer 7	Timer 8
Event input	TM7IO input (P14)	TM8IO input (P15)
	Synchronous TM7IO input	Synchronous TM8IO input

As an actual count clock, a signal divided by 1, 2, 4, 16 is selected.

■Count Timing of TMnIO Input (When falling edge is selected, Timer 7,Timer 8)
When TMnIO input is selected, TMnIO input signal is input to the timer n count clock. The binary counter counts up at the falling edge of the TMnIO input signal or TMnIO input signal that passed the divider.

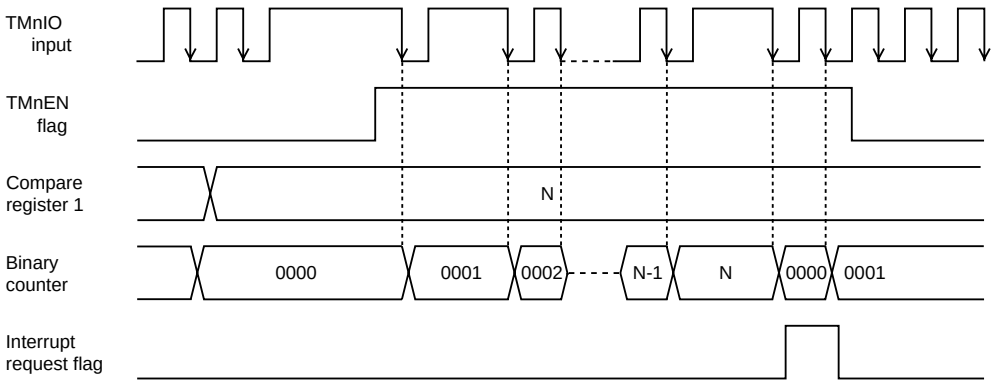


Figure 7-4-1 Count Timing TMnIO Input (Timer 7,Timer 8)

If the binary counter is read out during operation, incorrect data at counting up may be read. To prevent this, use the event count by the synchronous TMnIO input, which is shown in the following page.

■Count Timing of Synchronous TMnIO Input (When falling edge is selected, Timer 7, Timer 8)

If the synchronous TMnIO input is selected, the synchronizing circuit output signal is input to the timer n count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TMnIO input signal is changed. The binary counter counts up at the falling edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the division circuit.

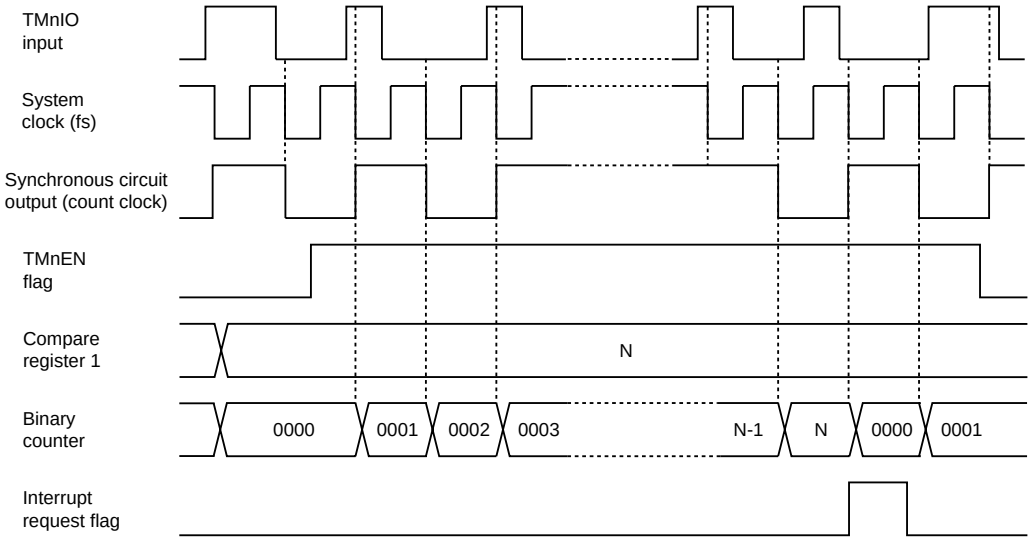


Figure 7-4-2 Count Timing of Synchronous TMnIO Input (Timer 7, Timer 8)

The timer n binary counter counts up the binary counter at the signal in synchronization with the system clock so that correct value is read out from the timer n binary counter. The return from STOP/HALT mode is not possible by the synchronous TMnIO input.

7-4-2 Setup Example

■Event Count Setup Example (Timer 7, Timer 8)

When the falling edge of the TM7IO input pin signal is detected 5 times using timer 7, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to input mode. P1DIR (x'3F31') bp4 : P1DIR4 = 0	(2) Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "0" to set P14 pin to input mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a clear source for the binary counter.
(4) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 10 bp3-2 : TM7PS1-0 = 00	(4) Select the TM7IO input as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1(no division) as a count clock source by the TM7PS1-0 flag.
(5) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'0004'	(5) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The set value should be 4, because the counting is 5 times. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.

Setup Procedure	Description
(6) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 :TM7LV1-0 = 10	(6) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If any interrupt request flag is already set, clear those request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(7) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(7) Set the TM7IE flag of the TM7ICR register to "1" to enable interrupt.
(8) Start the event count. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

Every time TM7BC detects the falling edge of the TM7IO input, it counts up from x'0000'. When the TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock, and the value of TM7BC becomes x'0000' to restart counting up.

7-5 16-bit Timer Pulse Output

7-5-1 Operation

TMnIO pin can output a pulse signal with an arbitrary frequency. The TMnO pin (large current pin) can output it, too.

■16-bit Timer Pulse Output Operation (Timer 7,Timer 8)
These timers can output 2 x cycle signal, compared with the set value of the compare register 1 (TMnOC1) and the 16-bit full count.
Output pins are as follows.

Table 7-5-1 Timer Pulse Output Pin

	Timer 7	Timer 8
Pulse output pin	TM7IO output (P14)	TM8IO output (P15)
	TM7O output (P51)	TM8O output (P53)

Table 7-5-2 shows the timer interrupt generation sources and the flags that control the timer pulse output cycle.

Table 7-5-2 16-bit Timer Interrupt Generation Source and Timer Pulse Output Cycle (Timer 7, Timer 8)

TMnMD2 register		Interrupt source	Timer pulse output cycle
TMnIRS1 flag	TMnBCR flag		
1	1	TMnOC1 compare match	set value of TMnOC1 x 2
0	1	TMnOC1 compare match	set value of TMnOC1 x 2
1	0	TMnOC1 compare match	full count of TMnBC x 2
0	0	full count overflow	full count of TMnBC x 2

■Count Timing of Timer Pulse Output by Compare Match (Timer 7,Timer 8)

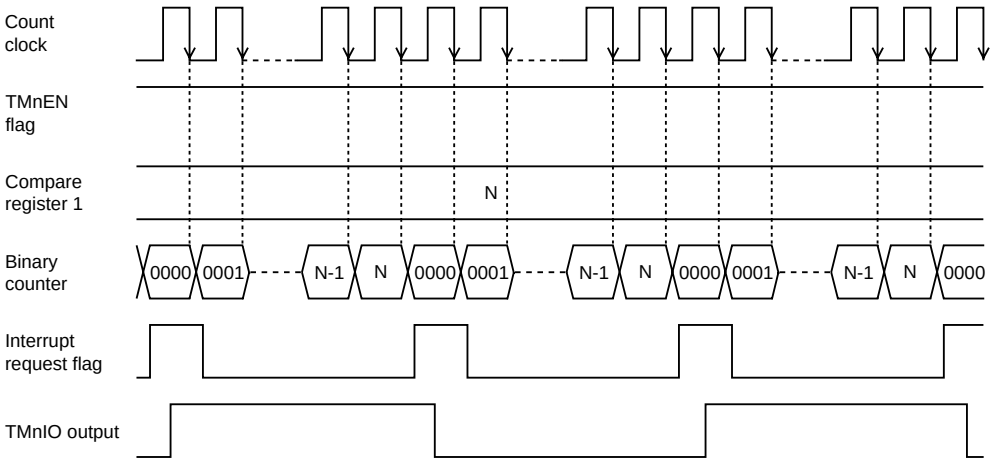


Figure 7-5-1 Count Timing of Timer Pulse Output (Timer 7, Timer 8)

TMnIO output pin outputs 2 x cycle, compared with the value of Compare Register 1 signal. If the binary counter reaches the compare value or full count overflow is occurred, the binary counter is cleared to x'0000', and the TMnIO output (timer output) is inverted. The inversion of the timer output is changed at the count clock at the rising edge. These form the correct output signal and internal waveform.

In the initial state after releasing reset, the timer pulse output is reset, and low output is fixed. Therefore, release the reset of the timer pulse output by setting the TMnCL flag of the TMnMD1 register to "0".

7-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 7, Timer 8)
TM7IO output pin outputs a 50 kHz pulse using timer 7. For this, select fosc as the clock source and set 1/2 cycle (100 kHz) to the timer 7 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set P14 pin as the special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the timer pulse output. TM7MD2 (x'3F79') bp4 : TM7PWM = 0	(3) Set the TMPWM flag of the timer 7 mode register 2 (TM7MD2) to "00" to select the timer pulse output.
(4) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as a clear source of a binary counter .
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency as the count clock source by the TM7PS1-0 flag.

Setup Procedure	Description
(6) Set the timer pulse output cycle. TM7PR1 (X'3F75', X'3F74')=x'00C7'	(6) Set 1/2 cycle of the timer pulse output to the timer 7 preset register 1(TM7PR1). To set 100 kHz by dividing 20 MHz, set as follows: 200 - 1 = 199 (x'C7') The same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Release the reset of the timer pulse output. TM7MD1 (x'3F78') bp5 : TM7CL = 0	(7) Set the TN7CL flag of the TM7MD1 register to "0" to enable the timer pulse output.
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If TM7BC reaches the set value of the TM7OC1 register and TM7BC is cleared to x'0000', the signal of the TM7IO output is inverted and TM7BC counts up from x'0000', again.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example (2), to set the P51 pin as a special function pin and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

At TMnOC1 = x'0000' and x'0001', the timer pulse output have the same waveform.

Regardless of whether the binary counter is stopped or operated, the timer output is "L", when the TMnCL flag of the TMnMD1 register is set to "1".

Compare register value calculation;

$$\text{Compare register value} = \frac{\text{Timer pulse output cycle}}{\text{Selected clock cycle} \times 2} - 1$$

7-6 16-bit Standard PWM Output

(Only duty can be changed consecutively)

The TMnIO pin outputs the standard PWM output, which is determined by the overflow timing of the binary counter, and the match timing of the timer binary counter and the compare register.
It can also be output from the TMnO high current pin.

7-6-1 Operation

■16-bit Standard PWM Output (Timer 7, Timer 8)
PWM waveform with an arbitrary duty is generated by setting a duty of PWM "H" period to the compare register 1 (TMnOC1). Its cycle is the time of the 16-bit timer full count overflow.
Table 7-6-1 shows the PWM output pin.

Table 7-6-1 PWM Output Pin

	Timer 7	Timer 8
PWM output pin	TM7IO output pin (P14)	TM8IO output pin (P15)
	TM7IO output pin (P51)	TM8IO output pin (P53)

■Count Timing of Standard PWM Output (at Normal)(Timer 7, Timer 8)

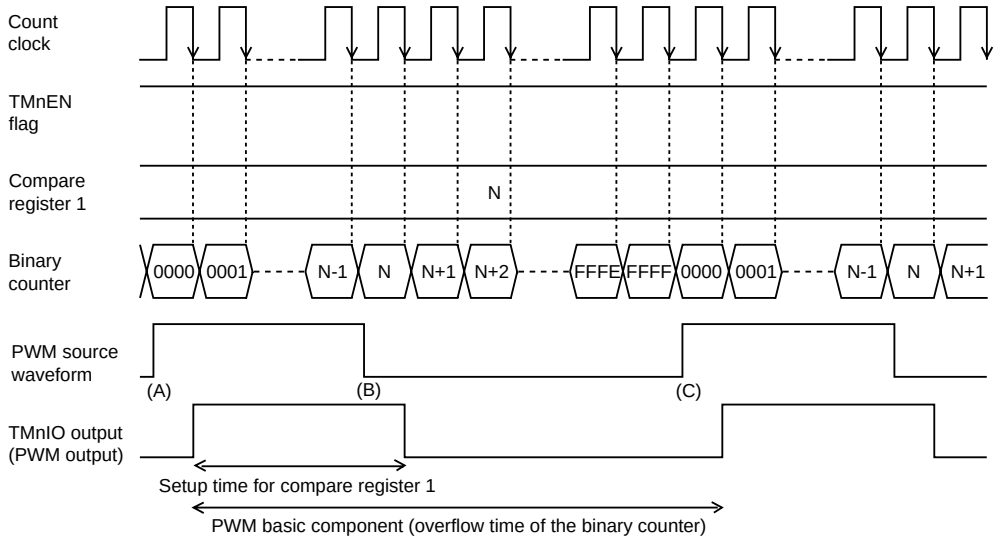


Figure 7-6-1 Count Timing of Standard PWM Output (at Normal)

PWM source waveform,

(A) shows "H" until the binary counter reaches the compare register value from x'0000'.

(B) shows "L" after the compare match, then the binary counter counts up till the overflow.

(C) shows "H" again if the binary counter overflow.

The PWM output form pin is 1 count clock delay of PWM source waveform. This is happened to form waveform inside the microcontroller to correct the output cycle.

■Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')(Timer 7, Timer 8)
Here is the count timing at setting x'0000' to the compare register 1.

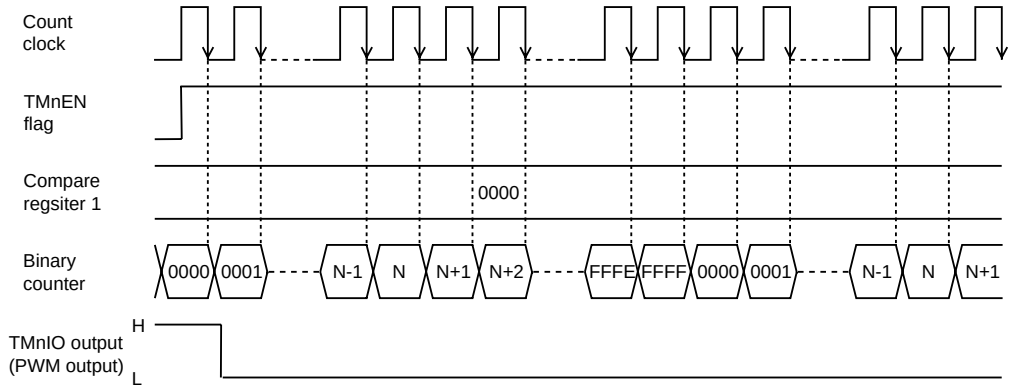


Figure 7-6-2 Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')

PWM output shows "H", when TMnEN flag is stopped (at "0").

■Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')(Timer 7,Timer 8)
Here is the count timing at setting x'FFFF' to the compare register 1.

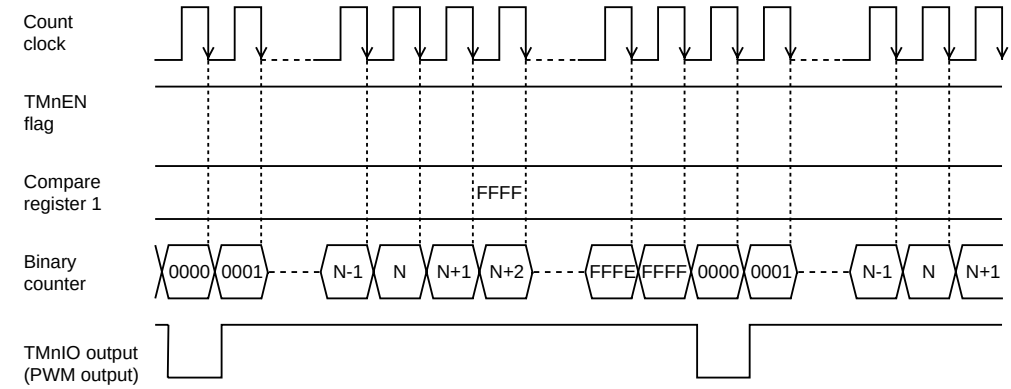


Figure 7-6-3 Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')

To output the standard PWM output, set the TMnBCR flag of the TMnMD2 register to "0" to select the full count overflow as the binary counter clear source and the PWM output set ("H" output) source.

The TM7OC1 compare match or the TM7OC2 compare match can be selected as a PWM output reset ("L" output) source with the T7PWMSL flag of the TM7MD2 register.

7-6-2 Setup Example

■Standard PWM Output Setup Example (Timer 7,Timer 8)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 305.18 Hz with timer 7 (at the high frequency oscillation, fosc=20 MHz). One cycle of the PWM output waveform is decided by the overflow of a binary counter. "H" period of the PWM output waveform is decided by the set value of a compare register 1.

An example setup procedure, with a description of each step is shown below.

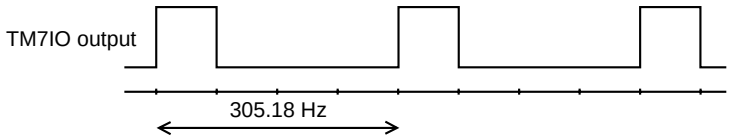


Figure 7-6-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD2 (x'3F79') bp4 : TM7PWM = 1	(3) Set the TMPWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(4) Set the standard PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 0	(4) Set the TM7BCR flag of the TM7MD2 register to "0" to select the full count overflow as the binary counter clear source.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency (no division) at count clock source by the TM7PS1-0 flag.
(6) Set "H" period of the PWM output. TM7PR1 (x'3F75', x'3F74')=x'4000'	(6) Set "H" period of the PWM output to the timer 7 preset register 1 (TM7PR1). To be a 1/4 duty of the full count (65536), set as follows: 65536 / 4 = 16384 (x'4000') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC reaches the set value of the TM7OC1 register, then, after the match it outputs "L". After that, TM7BC continues to count up. Once a overflow occurs, the PWM source waveform outputs "H" again, and TM7BC counts up from x'0000', again. TM7IO pin outputs one count clock delay of the PWM source waveform.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example (2), to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TM7OUT1-0 flag of the TM7MD3 register.
As for timer 8, it can be selected with the TM8PWMF flag of TM8MD3.

7-7 16-bit High Precision PWM Output

(Cycle/Duty can be changed consecutively)

The TMnIO pin outputs high precision PWM output, which is determined by the match timing of the timer binary counter and the compare register 1, and match timing of the binary counter and the compare register 2. It can be also output from the TMnO high current pin.

7-7-1 Operation

■16-bit High Precision PWM Output Operation (Timer 7, Timer 8)

The PWM waveform of an any cycle/duty is generated by setting the cycle of PWM to the compare register 1 (TMnOC1) and setting the duty of the "H" period to the compare register 2 (TMnOC2). The 16-bit timer that provides high precision PWM output function is timer 7.

■Count Timing of High Precision PWM Output (at Normal) (Timer 7, Timer 8)

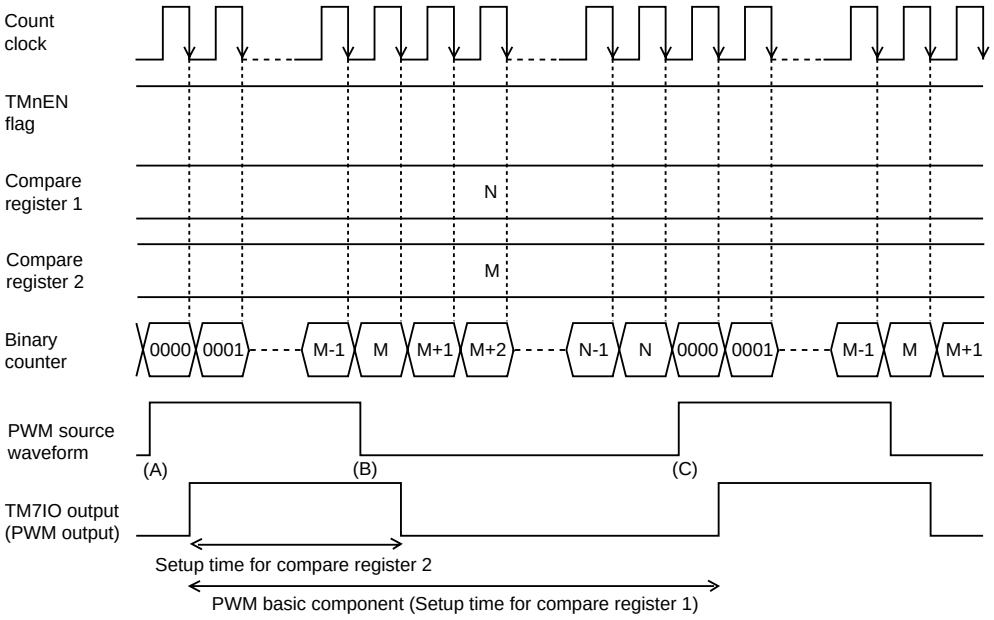


Figure 7-7-1 Count Timing of High Precision PWM Output (at Normal)

PWM source waveform,

(A) shows "H" until the binary counter reaches the compare register from x'0000'.

(B) shows "L" after the TMnOC2 compare match, the binary counter then counts up until the binary counter reaches the TMnOC1 compare register is cleared.

(C) shows "H" again when the binary counter is cleared.

The PWM output from pin is 1 count clock delay of PWM source waveform. This is happened to form waveform inside microcontroller to correct the output cycle.

■Count Timing of High Precision PWM Output (When compare register 2 is x'0000') (Timer 7)
Here is the count timing as the compare register 2 is set to x'0000';

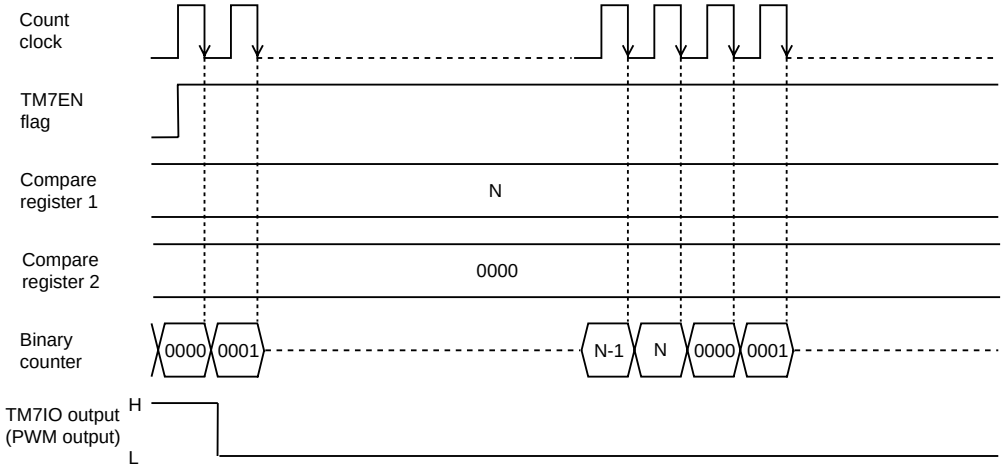


Figure 7-7-2 Count Timing of High Precision PWM Output (When compare register 2 is x'0000')

When the TMnEN flag is stopped (at "0"), the PWM output shows "H".

■Count Timing of High Precision PWM Output (at compare register 2 = compare register 1) (Timer 7)
Here is the count timing as the compare register 2 is set the same value to the compare register 1;

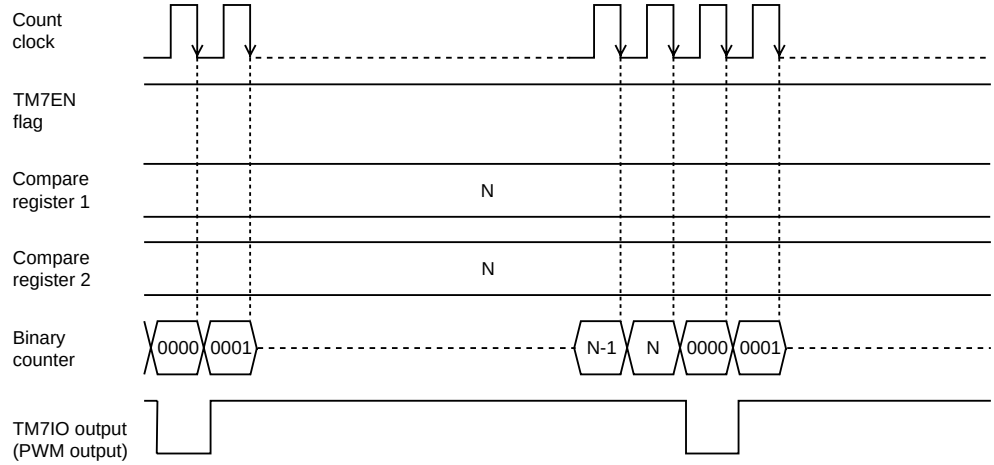


Figure 7-7-3 Count Timing of High Precision PWM Output (at compare register 2=compare register 1)

To output the high precision PWM output, set the TMBCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the clear source for the binary counter, and the set ("H" output) source of the PWM output. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as the reset ("L" output) source of the PWM output.

7-7-2 Setup Example

■High Precision PWM Output Setup Example (Timer 7,Timer 8)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 400 Hz with timer 7. Select fosc/2 (at fosc = 20 MHz) as the clock source. One cycle of the PWM output waveform is decided by the set value of a compare register 1. "H" period of the PWM output waveform is decided by the set value of a compare register 2.

An example setup procedure, with a description of each step is shown below.

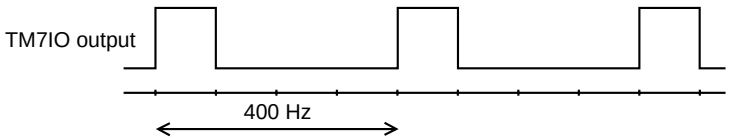


Figure 7-7-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 :P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port1 output mode register (P1OMD) to "1" to set the p14 pin as a special function pin. Set the P1DIR4 flag of the port1 direction control register (P1DIR) to "1" for output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD2 (x'3F79') bp4 : TM7PWM = 1	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(4) Set the high precision PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1 bp6 : T7PWMSL = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as a clear source of binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a duty select source of the PWM output.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(5) Select fosc as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/2 dividing as count clock source by the TM7PS1-0 flag.
(6) Set the PWM output cycle. TM7PR1 (x'3F75',x'3F74') = x'61a7'	(6) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1). To be 400 Hz by dividing 10 MHz, set as follows: 25000 - 1 = 24999 (x'61a7') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Set the "H" period of the PWM output. TM7PR2 (x'3F7D',x'3F7C')=x'186a'	(7) Set the "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2). To be a 1/4 duty of 25000 dividing, set as follows: 25000 / 4 = 6250 (x'186a') At that time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up. Once TM7BC matches the TM7OC1 register to be cleared, the PWM source waveform outputs "H" again and TM7BC counts up from x'0000' again. TM7IO pin outputs one count clock delay of the PWM source waveform.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) at the setup example(2), to "1" to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TMPWM flag of the TM7MD register.

Set as the set value of TM7OC2 ≤ the set value of TM7OC1. If it is set as the set value of TM7OC2 > the set value of TM7OC1, the IGBT output is a "H" fixed output.

7-8 16-bit Timer Synchronous Output

7-8-1 Operation

If the binary counter of the timer reaches the set value of the compare register, port 6 outputs the port 6 output latched data at the next count clock.

■16-bit Timer Synchronous Output Operation (Timer 7)
Port 6 outputs the port 6 output latched data at a TM7OC1 compare register reaches a binary counter or at an interrupt request generation by the full count overflow. Only port 6 can be used in this operation, and each bit can be set individually.

■Count Timing of Synchronous Output (Timer 7)

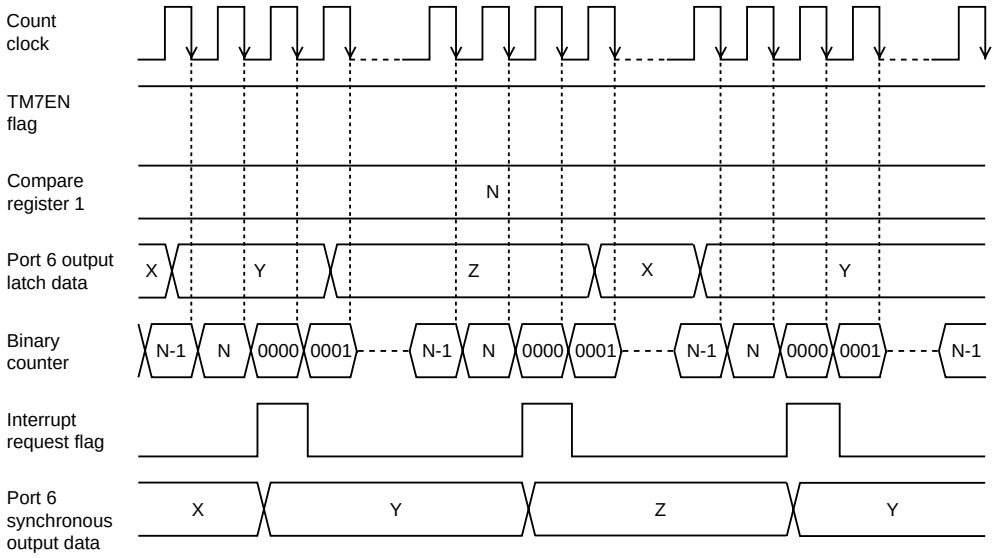


Figure 7-8-1 Count Timing of Synchronous Output (Timer 7)

Output pin outputs the port 6 output latch data at an interrupt request generation by the match of a binary counter and a compare register 1.

7-8-2 Setup Example

■Synchronous Output Setup Example (Timer 7)

Here is an example to output the port 6 latch data from the synchronous output pin constantly (in every 100 µs) with timer 7. As a clock source of timer 7, fs/4 (fosc=8 MHz) is selected.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 : SYOEVS1-0 = 01	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "01" to set the synchronous output event to the timer 7 interrupt.
(3) Set the synchronous output pin. P6SYO (x'3F1E') = x'FF' P6DIR (x'3F36') = x'FF'	(3) Set the port 6 synchronous output control register (P6SYO) to x'FF' to set the synchronous output pin. (P67 to P60 : Synchronous output pin) Set the port6 direction control register (P6DIR) to x'FF' to set port 6 to output pin. Add pull-up resistor, if necessary. [☞ Chapter 4 I/O Ports]
(4) Select the timer clear factor. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the clear source for the binary counter.
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 01 bp3-2 : TM7PS1-0 = 10	(5) Select fs as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/4 dividing as a clock source by the TM7PS1-0 flag.
(6) Set the synchronous output event generation cycle. TM7PR1 (x'3F75',x'3F74')=x'0063'	(6) Set the synchronous output event generation cycle to the timer 7 preset register 1 (TM7PR1). To set 10 kHz by dividing 1 MHz, set as; 100 - 1 = 99 (x'0063') At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and TM7BC is initialized to x'0000'.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If any data is written to the port 6 output register (P6OUT), TM7BC is set to the set value of TM7OC1 register and the synchronous output pin outputs data of port 6 in every time an interrupt request is generated.

7-9 16-bit Timer Capture

7-9-1 Operation

The value of binary counter is read out at the timing of the external interrupt input signal, or at the timing of the writing operation with an any value to the capture register.

■Capture Operation with External Interrupt Signal as a Trigger (Timer 7, Timer 8)
Input capture trigger is generated at the external interrupt signal that passed through the external interrupt interface block. The capture trigger is selected by the timer n mode register 2 (TMnMD2) and the external interrupt control register (IRQ0ICR, IRQ1ICR, IRQ2ICR).
Selectable capture triggers and the interrupt flag setup are shown below.

Table 7-9-1 Capture Trigger

Capture trigger source	Timer 7 mode register 2		External interrupt n control register (IRQnICR)	Both edges interrupt control register (EDGDT)		Interrupt starting edge of external interrupt n
	T7ICT1-0	T7ICEDG	REDGn (bp5)	EDGSEL3	EDGSEL2	
IRQ0 falling edge	00(IRQ0)	1	0	-	-	IRQ0 falling edge
IRQ0 rising edge	00(IRQ0)	1	1	-	-	IRQ0 rising edge
IRQ0 both edges	00(IRQ0)	0	0	-	-	IRQ0 falling edge
			1	-	-	IRQ0 rising edge
IRQ1 falling edge	01(IRQ1)	1	0	-	-	IRQ1 falling edge
IRQ1 rising edge	01(IRQ1)	1	1	-	-	IRQ1 rising edge
IRQ1 both edges	01(IRQ1)	0	0	-	-	IRQ1 falling edge
			1	-	-	IRQ1 rising edge
IRQ2 falling edge	10(IRQ2)	1	0	-	0	IRQ2 falling edge
IRQ2 rising edge	10(IRQ2)	1	1	-	0	IRQ2 rising edge
IRQ2 both edges(*)	10(IRQ2)	0	0	-	0	IRQ2 falling edge
			1	-	0	IRQ2 rising edge

The external interrupt 2 (IRQ2) have the function of both edges interrupt. However, input capture can not be used together with both edges interrupt. [table 7-9-1(*)]

Input capture signals of the 16-bit timers 7 and 8 are generated by fosc or fs. (When the timer's clock source is fosc, they are generated by fosc. Other than that, they are generated by fs.) This requires cautions when external event frequency (TMnIO input) is counted with event frequency higher than fs, as this setting could cause inaccurate counting.
Switching the clock source to use fs as a system clock by dividing oscillation clock fosc requires extra attention.

When setup is as following (1), (2), and external interrupt valid edge is switched by program, interrupt request and capture trigger are generated.

(1) at switching the valid edge from the falling to the rising, when the interrupt pin is "H" level.

(2) at switching the valid edge from the rising to the falling, when the interrupt pin is "L" level.

This does not happen, if the interrupt edge is switched after the generation of an valid edge interrupt set in advance. But when the both edges interrupt function is used, this could happen. The noise influence should be considered when operating the interrupt flag on program.

[☞ Chapter 3 3-3-4. Specified Polarity Edge Interrupt]

■Capture Count Timing as a Both Edges of External Interrupt Signal is selected as a Trigger (Timer 7)

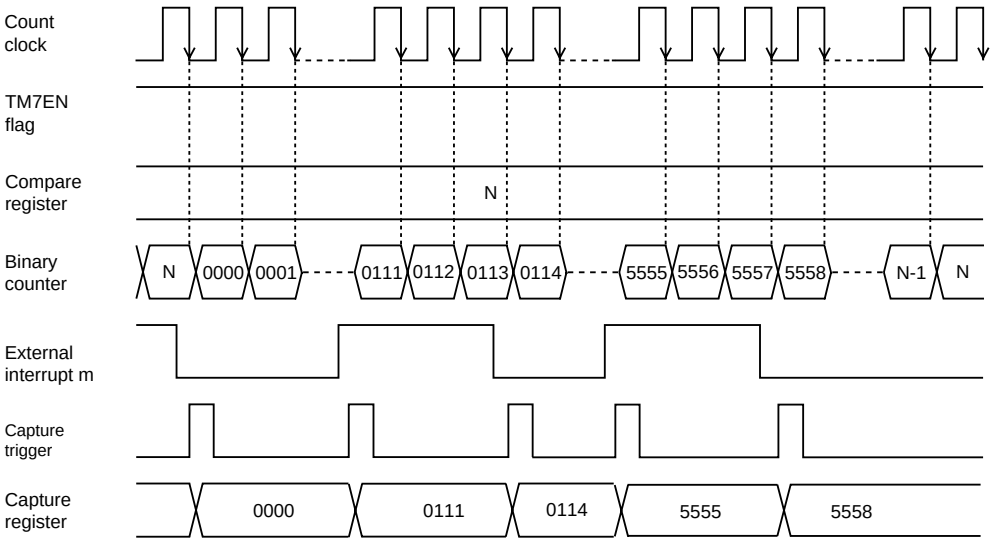


Figure 7-9-1 Capture Count Timing as an External Interrupt Signal is selected as a Trigger (Timer 7, Timer 8)

A capture trigger is generated at the both edges of the external interrupt m input signal. In synchronized with this capture trigger, the value of binary counter is loaded to the input capture register. The value loaded to the capture register is depending on the value of a binary counter at the falling edge of a capture trigger. When the specified edge is selected as a capture trigger source, a capture trigger is generated only at that edge. The other count timing is same as the count timing of the timer operation.

When the binary counter is used as a free counter which counts x'0000' to x'FFFF', set the compare register 1 to x'FFFF', or set the TMnBCR flag of the TM7MD2 to "0".

Even if an event is generated before the value of the input capture register is read out, the value of the input capture register can be rewritten.

In the initial state after releasing the reset, the generation of trigger by the external interrupt signal is disabled. Set the TnICEN flag of the TMnMD2 register to "1" to enable the trigger generation.

■Capture Operation triggered by writing software (Timer 7, Timer 8)

A capture trigger can be generated by writing an arbitrary value to the input capture register (TMnIC). In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register.

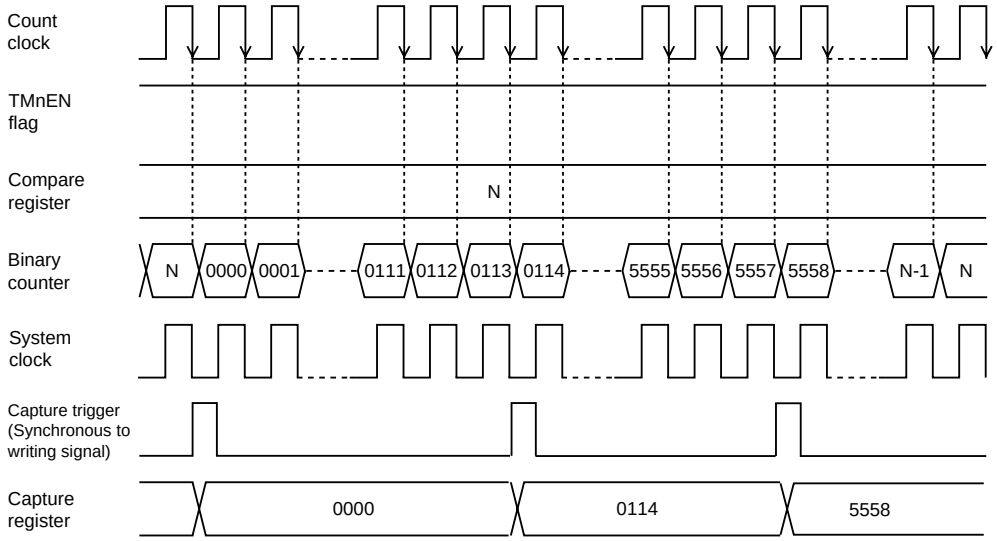


Figure 7-9-2 Capture Count Timing Triggered by Writing Software (Timer 7, Timer 8)

A capture trigger is generated at the writing signal to the input capture register. The writing signal is generated at the last cycle of the writing instruction. In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register. That value is depending on the value of the binary counter at the falling edge of the capture trigger. The other timing is the same as the timer operation.

The writing to the input capture register to generate a capture trigger should be done with a 8-bit access instruction of the TMnICL register or the TMnICH register.
At this time, data is not actually written to the TMnIC register.

On hardware, there is no flag to disable the capture operation triggered by writing software. Capture operation is enabled regardless of the TnICEN flag of the TMnMD2 register.

7-9-2 Setup Example

■Capture Function Setup Example (Timer 7, Timer 8)
Pulse width measurement is enabled by loading the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 input signal with timer 7. In the example setup procedure shown below, rising edge is selected to be an interrupt generation edge.

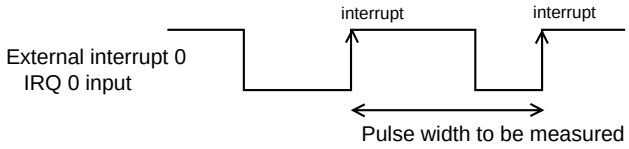


Figure 7-9-3 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the timer clear condition. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as the source to clear the binary counter.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(3) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. And select 1/1 (no dividing) of fosc as the count clock source by the TM7PS1-0 flag.
(4) Select the capture trigger interrupt source. TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(4) Select the external interrupt 0 (IRQ0) input as the generation source of capture trigger by the T7ICT1-0 flag of the TM7MD2 register.
(5) Select the interrupt generation valid edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(5) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation valid edge.

Setup Procedure	Description
(6) Select the capture trigger generation edge. TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(6) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the external interrupt valid edge as a capture trigger source.
(7) Set the compare register. TM7PR1(x'3F75',x'3F74') = x'FFFF'	(7) Set the timer 7 preset register 1 (TM7PR1) to x'FFFF'. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(8) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(8) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0IR register. If any interrupt request flag is set already, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(9) Enable the interrupt by setting the IRQ1IE flag of the IRQ0ICR register to "1".
(10) Enable the capture trigger generation. TM7MD2 (x'3F79') bp2 : T7ICEN = 1	(10) Enable the capture trigger generation by setting the T7ICEN flag of the TM7MD2 register to "1".
(11) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM7BC is loaded to the TM7IC register. At that time, the pulse width between rising edge of the external interrupt input signal can be measured by reading the value of TM7IC register through interrupt service routine, and calculating the difference between the capture values.

7-10 Cascade Connection

7-10-1 Operation

Cascading timers 7 and 8 forms a 32-bit timer.

■16-bit Timer Cascade Connection Operation (Timer 7 + Timer 8)
Timer 7 and timer 8 are combined to be a 32-bit timer. Cascading timer is operated at clock source of timer 7 which are lower 16 bits.

Table 7-13-1 Timer Functions at Cascade Connection

	Timer 7 + Timer 8 (32-bit)
Interrupt source	TM8IRQ
Timer operation	√
Event count	√ (TM7IO input)
Timer pulse output	√ (TM8IO output)
PWM output	-
Synchronous output	-
Capture function	√
Pulse width measurement	√
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16
fosc : Machine clock (High frequency oscillation) fs : System clock [☞ Chapter 2 2-5 Clock Switching]	

At cascade connection, the binary counter and the compare register are operated as a 32 bit register. At operation, set the TM7EN flag of the lower 16-bit timers to "1" to be operated.
Also, select the clock source with the lower 16-bit timer.
Other setup and count timing are the same as the 16-bit timer at independently operation.

When timer 7 and timer 8 are used in cascade connection, timer 8 is used as an interrupt request flag. Timer pulse output of timer 7 is "L" fixed output.
Timer 7 interrupt should be disabled as interrupt request of timer 7 is generated.

7-10-2 Setup Example (Timer Operation)

■Cascade Connection Timer Setup Example (Timer 7+ Timer 8)

Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 7 and timer 8, as a 32-bit timer is shown. An interrupt is generated in every 100000 cycles (40 ms) by selecting source clock to fs/4 (fosc=20 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 :TM7EN = 0 TM8MD1 (x'3F88') bp3 :TM8EN = 0	(1) Set the TM7EN flag of the timer 7 mode register (TM7MD1) to "0", the TM8EN flag of the timer 8 mode register to "0" to stop timer 7 and timer 8 counting.
(2) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 :TM7BCR = TM8MD2 (x'3F89') bp5 :TM8BCR = 1	(2) Set the TM7BCR flag of TM7MD2 register and TM8BCR flag of TM8MD2 register to "1" to se lect compare match as a clear source of the binary counter.
(3) Select the normal lower timer operation. TM7MD2 (x'3F79') bp2 :TM71CEN = 00 bp4 :TM7PWM = 00	(3) Set the TM7ICEN flag and the TM7PWM flag of the TM7MD2 register to "0" to select normal timer operation.
(4) Set the cascade connection. TM8MD1 (x'3F88') bp6 :TM8CAS = 1	(4) Set the TM8CAS flag of the TM8MD1 register to "1" to connect timer 7 and timer 8 in cascade connection.
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 :TM7CK1-0 = 01 bp3-2 :TM7PS1-0 = 10	(5) Select fs as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/4 dividing of fs as the count clock source by the TM7PS1-0 flag.
(6) Set the interrupt generation cycle. TM7PR1(x'3F75', x'3F74')=x'FFFF' TM8PR1(x'3F85', x'3F84')=x'86A0'	(6) Set the timer 7 preset register 1 (TM7PR1) and timer 8 preset register 1 (TM8PR1) to the interrupt generation cycle (100000 cycles - 1). At that time, the same values as the preset registers are loaded to the timer compare register1 (TM7OC1) and timer 8 compare register 1(TM8OC1), and the binary counters are initialized to x'0000'.

Setup Procedure	Description
(7) Disable the lower timer interrupt. TM7ICR (x'3FF1') bp1 :TM7IE = 0	(7) Set the TM7IE flag of the timer 7 interrupt control register (TM7ICR) to "0" to disable the interrupt.
(8) Set the level of the upper timer interrupt. TM8ICR (x'3FF3') bp7-6 :TM8LV1-0 = 10	(8) Set the interrupt level by the TM8LV1-0 flag of the timer 8 interrupt control register (TM8ICR). If any interrupt request flag is already set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the upper timer interrupt. TM8ICR (x'3FF3') bp1 :TM8IE = 1	(9) Set the TM8IE flag of the TM8ICR register to "1" to enable the interrupt.
(10) Start the lower timer operation. TM8MD1 (x'3F88') bp4 :TM8EN = 1	(10) Set the TM8EN flag of the TM8MD1 register to "1" to start timer 8.
(11) Start the lower timer operation. TM7MD1 (x'3F78') bp4 :TM7EN = 1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 0.

TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from x'00000000' as a 32-bit timer.
When TM7BCL + TM7BCH + TM8BCL + TM8BCH reaches the set value of TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H register, the timer 8 interrupt request flag is set at the next count clock, and the value of TM7BCL + TM7BCH + TM8BCL + TM8BCH becomes x'00000000' to restarts count up.

Start upper timer operation before lower timer operation.

Chapter 8 Time Base Timer / 8-bit Free-running Timer

8

8-1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 6).
Time base timer is a 15-bit timer counter, which cannot stop operation, except with a 8-bit free running timer at stand-by mode (STOP mode).

8-1-1 Functions

Table 8-1-1 shows the clock sources and the interrupt generation cycles that timer 6 and time base timer can use.

Table 8-1-1 Clock Source and Generation Cycle

	Time base timer	Timer 6 (8-bit free-running)
8-bit timer operation	-	√
Interrupts	TBIRQ	TM6IRQ
Clock source	fosc fx	fosc fx fs fosc X $1/2^{12}$ (*1) fosc X $1/2^{13}$ (*1) fx X $1/2^{12}$ (*2) fx X $1/2^{13}$ (*2)
Interrupt generation cycle	fosc X $1/2^{7}$ (*1) fosc X $1/2^{8}$ (*1) fosc X $1/2^{9}$ (*1) fosc X $1/2^{10}$ (*1) fosc X $1/2^{13}$ (*1) fosc X $1/2^{15}$ (*1) fx X $1/2^{7}$ (*2) fx X $1/2^{8}$ (*2) fx X $1/2^{9}$ (*2) fx X $1/2^{10}$ (*2) fx X $1/2^{13}$ (*2) fx X $1/2^{15}$ (*2)	The interrupt generation cycle is decided by the arbitrary value written to TM6OC.
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock [☞ Chapter 2 2-4. Clock Switching] - *1 can be used when a clock source of time base timer is selected to 'fosc'. - *2 can be used when a clock source of time base timer is selected to 'fx'. - Time base timer and timer 6 cannot stop timer 6 counting.		

8-1-2 Block Diagram

■Timer 6, Time Base Timer Block Diagram

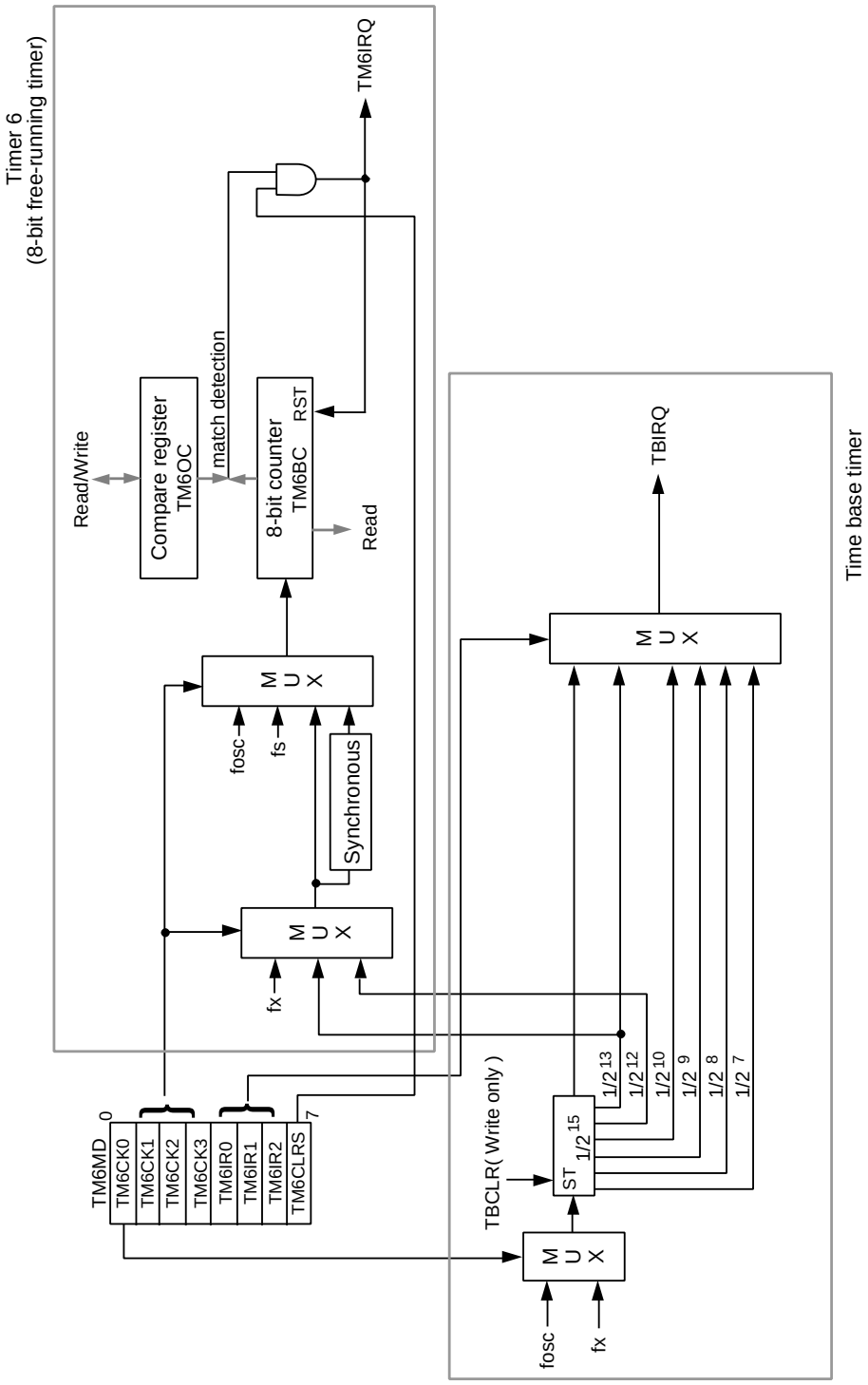


Figure 8-1-1 Block Diagram (Timer 6, Time Base Timer)

8-2 Control Registers

Timer 6 consists of binary counter (TM6BC), compare register (TM6OC), and is controlled by mode register (TM6MD). Time base timer is controlled by mode register (TM6MD) and time base timer clear register (TBCLR).

8-2-1 Control Registers

Table 8-2-1 shows the registers that control timer 6, time base timer.

Table 8-2-1 Control Registers

	Register	Address	R/W	Function	Page
Timer 6	TM6BC	x'03F68'	R	Timer 6 binary counter	VIII - 5
	TM6OC	x'03F69'	R/W	Timer 6 compare register	VIII - 5
	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register	III - 25
Time base timer	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TBCLR	x'03F6B'	W	Time base timer clear control register	VIII - 5
	TBICR	x'03FF0'	R/W	Time base interrupt control register	III - 26

R/W : Readable / Writable
R : Readable only
W : Writable only

8-2-2 Programmable Timer Registers

Timer 6 is a 8-bit programmable counter.
Programmable counter consists of compare register (TM6OC) and binary counter (TM6BC).

Binary counter is a 8-bit up-counter. When the TM6CLRS flag of the timer 6 mode register (TM6MD) is "0" and the interrupt cycle data is written to the compare register (TM6OC), the timer 6 binary counter (TM6BC) is cleared to x'00'.

■Timer 6 Binary Counter (TM6BC)

	7	6	5	4	3	2	1	0	
TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	(At reset : X X X X X X X X)

Figure 8-2-1 Timer 6 Binary Counter (TM6BC : x'03F68', R)

■Timer 6 Compare Register (TM6OC)

	7	6	5	4	3	2	1	0	
TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	(At reset : X X X X X X X X)

Figure 8-2-2 Timer 6 Compare Register (TM6OC : x'03F69', R/W)

Time base timer cannot stop counting but the software can reset its operation. Time base timer can be cleared by writing an arbitrary value to the time base timer clear control register (TBCLR).

■Time Base Timer Clear Control Register (TBCLR)

	7	6	5	4	3	2	1	0	
TBCLR	-	-	-	-	-	-	-	-	(For writing only)

Figure 8-2-3 Time Base Timer Clear Control Register (TBCLR : x'03F6B')

8-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 6 and time base timer.

■Timer 6 Mode Register (TM6MD)

	7	6	5	4	3	2	1	0
TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0

(At reset : 0 0 0 0 0 0 0 0)

TM6CKS0	Time base timer clock source selection
0	fosc
1	fx

TM6CK3	TM6CK2	TM6CK1	Timer 6 clock source selection
0	0	0	fosc
		1	fs
	1	0	fx
		1	Synchronous fx
1	0	0	Time base selection clock × $1/2^{13}$
		1	Synchronous time base selection clock × $1/2^{13}$
	1	0	Time base selection clock ×$1/2^{12}$
		1	Synchronous time base selection clock × $1/2^{12}$

TM6IR2	TM6IR1	TM6IR0	Time base timer interrupt cycle selection
0	0	0	Time base selection clock × $1/2^{7}$
		1	Time base selection clock × $1/2^{8}$
	1	0	Time base selection clock × $1/2^{9}$
		1	Time base selection clock × $1/2^{10}$
1	0	-	Time base selection clock × $1/2^{13}$
	1		Time base selection clock × $1/2^{15}$

TM6CLRS	Timer 6 binary counter clear selection flag
0	Enable the initialization of TM6BC as TM6OC is written
1	Disable the initialization of TM6BC as TM6OC is written

* TM6IRQ is disable as TM6CLRS = 0,
TM6IRQ is enable as TM6CLRS = 1.

Figure 8-2-4 Timer 6 Mode Register (TM6MD : x'03F6A', R/W)

8-3 8-bit Free-running Timer

8-3-1 Operation

■8-bit Free-running Timer (Timer 6)
The generation cycle of the timer interrupt should be set in advance, by the set value of the compare register (TM6OC) and the clock source selection. When the binary counter (TM6BC) reaches the set value of the compare register, an interrupt request is generated at the next count clock and the binary counter is cleared to restart count up from x'00'.
Table 8-3-1 shows selectable clock sources.

Table 8-3-1 Clock Source at Timer Operation (Timer 6)

Clock source	One count time
fosc	50 ns
fx	30.5 µs
fs	100 ns
fosc X $1/2^{12}$	204.8 µs
fosc X $1/2^{13}$	409.6 µs
fx X $1/2^{12}$	125 ms
fx X $1/2^{13}$	250 ms
fosc = 20(MHz) fx = 32.768(kHz) fs = fosc/2 = 10 MHz	

Timer 6 does not stop the operation.

■8-bit Free-running Timer as a 1 minute-timer, a 1 second-timer

Table 8-3-2 shows the clock source selection and the TM6OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table 8-3-2 1 minute-timer, 1 second-timer (Timer 6) Setup

Interrupt Generation Cycle	Clock Source	TM6OC Register
1 min	$fx \times 1/2^{13}$	X'EF'
1 s	$fx \times 1/2^{12}$	X'07'
	$fx \times 1/2^{13}$	X'03'
fx = 32.768(kHz)		

When the 1 minute-timer (1 m.) is set on Table 8-3-2., the bp1 waveform frequency (cycle) of the TM6BC register is 1 Hz (1 s.). So, that can be used for adjusting the seconds.

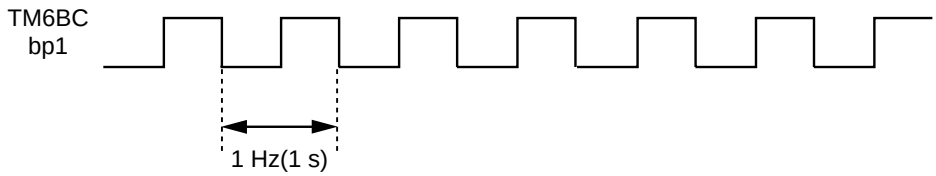


Figure 8-3-1 Waveform of TM6BC Register bp1 (Timer 6)

■Count Timing of Timer Operation (Timer 6)

Binary counter counts up with the selected clock source as a count clock.

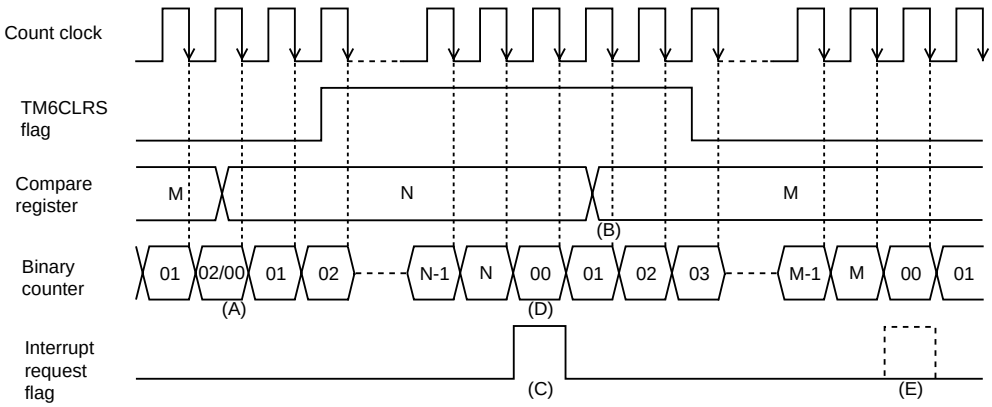


Figure 8-3-2 Count Timing of Timer Operation (Timer 6)

(A) When any data is written to the compare register as the TM6CLRS flag is "0", the binary counter is cleared to x'00'.

(B) Even if any data is written to the compare register as the TM6CLRS flag is "1", the binary counter is not changed.

(C) When the binary counter reaches the value of the compare register as the TM6CLRS flag is "1", an interrupt request flag is set at the next count clock.

(D) When an interrupt request flag is set, the binary counter is cleared to x'00' and restarts the counting.

(E) Even if the binary counter reaches the value of the compare register as the TM6CLRS flag is "0", no interrupt request flag is set.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared at the next count clock.
So set the compare register as :

Compare register setting = (count till the interrupt request -1)

If the fx input is selected as a clock source and the value of timer 6 binary counter is read out at operation, an incorrect value could be read out. To prevent this, select a synchronous fx as the count clock source. But if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

If the smaller value than the binary counter is set to the compare register at counting operation, the binary counter continues counting till overflow.

8-3-2 Setup Example

■Timer Operation Setup (Timer 6)

Timer 6 generates interrupts constantly for timer function. Interrupts are generated in every 250 dividing (25 µs) by selecting fs (fosc = 20 MHz at operation) as clock source.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Enable the binary counter initialization. TM6MD (x'3F6A') bp7 : TM6CLRS = 0	(1) Set the TM6CLRS flag of the timer 6 mode register (TM6MD) to "0". At that time, the initialization of the timer 6 binary counter (TM6BC) is enabled.
(2) Select the clock source. TM6MD (x'3F6A') bp3-1 : TM6CK3-1 = 001	(2) Clock source can be selected by the TM6CK3-1 flag of the TM6MD register. Actually, fx is selected.
(3) Set the interrupt generation cycle. TM6OC (X'3F69') = x'F9'	(3) Set the interrupt generation cycle to the timer 6 compare register (TM6OC). At that time, TM6BC is initialized to x'00'.
(4) Enable the interrupt request generation. TM6MD (x'3F6A') bp7 : TM6CLRS = 1	(4) Set the TM6CLRS flag of the TM6MD register to "1" to enable the interrupt request generation.
(5) Set the interrupt level. TM6ICR (x'3FEF') bp7-6 : TM6LV1-0 = 01	(5) Set the interrupt level by the TM6LV1-0 flag of the timer 6 interrupt control register (TM6ICR). If the interrupt request flag may be already set, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM6ICR (x'3FEF') bp1 : TM6IE = 1	(6) Set the TM6IE flag of the TM6ICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

As TM6OC is set, TM6BC is initialized to x'00' to count up.
When TM6BC matches TM6OC, the timer 6 interrupt request flag is set at the next count clock and TM6BC is cleared to x'00' to restart counting.

If the TM6CLRS flag of the TM6MD register is set to "0", TM6BC can be initialized at every rewriting of TM6OC register, but in that state the timer 6 interrupt is disabled. If the timer 6 interrupt should be used, set the TM6CLRS flag to "1" after rewriting the TM6OC register.

On the timer 6 clock source selection, if the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is necessary.

8-4 Time Base Timer

8-4-1 Operation

■Time Base Timer (Time Base Timer)

Interrupt is constantly generated by a selected clock source and a interrupt generation cycle.

Table 8-4-1 shows the interrupt generation cycle in combination with the clock source ;

Table 8-4-1 Selection of Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fosc	fosc X $1/2^7$	6.4 µs
	fosc X $1/2^8$	12.8 µs
	fosc X $1/2^9$	25.6 µs
	fosc X $1/2^{10}$	51.2 µs
	fosc X $1/2^{13}$	409.6 µs
	fosc X $1/2^{15}$	1.64 ms
fx	fx X $1/2^7$	3.9 ms
	fx X $1/2^8$	7.8 ms
	fx X $1/2^9$	15.6 ms
	fx X $1/2^{10}$	31.2 ms
	fx X $1/2^{13}$	250 ms
	fx X $1/2^{15}$	1 s
fosc = 20(MHz) fx = 32.768(kHz)		

■Count Timing of Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a count clock.

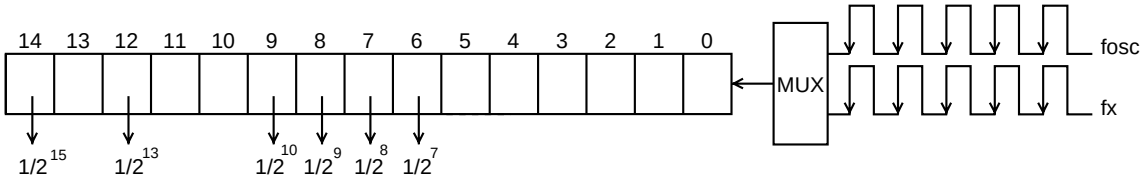


Figure 8-4-1 Count Timing of Timer Operation (Time Base Timer)

When the selected interrupt cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set.

An interrupt may be generated at switching of the clock source. Enable the interrupt after switching the clock source.

Time base timer cannot stop the operation.
The initialization can be done by writing an arbitrary value to the time base timer clear control register (TBCLR).

8-4-2 Setup Example

■Timer Operation Setup (Time Base Timer)

An interrupt can be generated constantly with time base timer in the selected interrupt cycle. The interrupt generation cycle is fosc × $1/2^{13}$(0.977 ms : fosc = 8.38 MHz) to generate interrupts.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the clock source. TM6MD (x'3F6A') bp0 : TM6CK0 = 0	(1) Select fosc as a clock source by the TM6CK0 flag of the timer 6 mode register (TM6MD).
(2) Select the interrupt generation cycle. TM6MD (x'3F6A') bp6-4 : TM6IR2-0 = 100	(2) Select the selected clock × $1/2^{13}$ as an interrupt generation cycle by the TM6IR2-0 flag of the TM6MD register.
(3) Initialize the time base timer. TBCLR (x'3F6B') = x'00'	(3) Write value to the time base timer clear control register (TBCLR) to initialize time base timer.
(4) Set the interrupt level. TBICR (x'3FF0') bp7-6 : TBLV1-0 = 01	(4) Set the interrupt level by the TBLV1-0 flag of the time base interrupt control register (TBICR). If any interrupt request flag may be already set, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(5) Enable the interrupt. TBICR (x'3FF0') bp1 : TBIE = 1	(5) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

When the selected interrupt generation cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 9 Watchdog Timer

9

9-1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. That is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. If the watchdog interrupt is generated twice, consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

9-1-1 Block Diagram

■Watchdog Timer Block Diagram

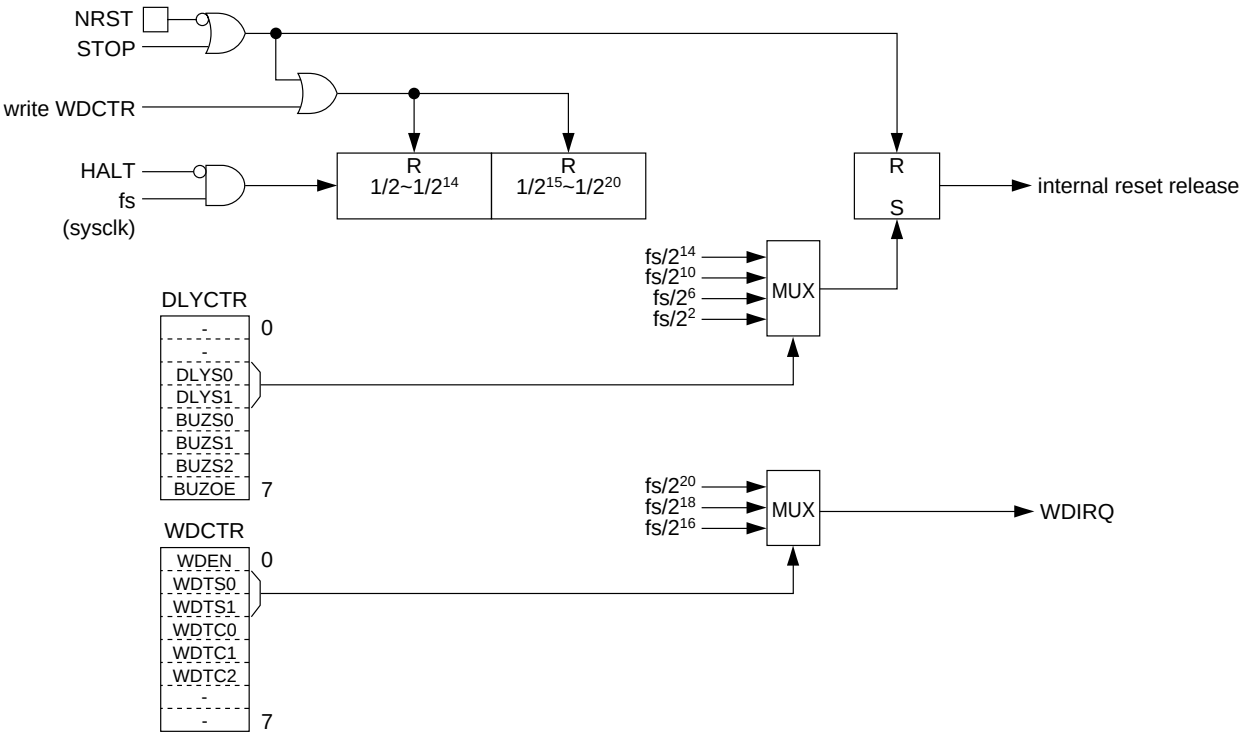


Figure 9-1-1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. This is used as a watchdog timer except at recovering from STOP mode and at reset releasing.
The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (x'0000'). The oscillation stabilization wait time is set by the oscillation stabilization control register (DLYCTR). After the oscillation stabilization wait time is over, counting is continued as a watchdog timer. [☞ Chapter 2 2-6. Reset]

9-2 Control Registers

The watchdog timer is controlled by the watchdog timer control register (WDCTR).

■Watchdog Timer Control Register (WDCTR)

	7	6	5	4	3	2	1	0
WDCTR	-	-	WDTC2	WDTC1	WDTC0	WDTS1	WDTS0	WDEN

(At reset : - - 0 0 0 1 1 0)

WDEN	Watchdog timer enable
0	Watchdog timer is stopped
1	Watchdog timer is operated

WDTS1	WDTS0	Watchdog time-out period setup
0	0	2^{16} of system clock
	1	2^{18} of system clock
1	×	2^{20} of system clock

WDTC2	WDTC1	WDTC0	Watchdog timer can be cleared at the following cycle or more
0	0	0	no limit
		1	2^{7} of system clock
	1	0	2^{9} of system clock
		1	2^{11} of system clock
1	0	0	2^{13} of system clock
		1	2^{15} of system clock
	1	0	2^{17} of system clock
		1	2^{19} of system clock

Figure 9-2-1 Watchdog Timer Control Register (WDCTR : x'03F02', R/W)

9-3 Operation

9-3-1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer is overflowed, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI). At reset, the watchdog timer is stopped, but once the operation is enabled, it cannot be stopped except at reset. The watchdog timer control register (WDCTR) sets when the watchdog timer is released or how long the time-out period should be.

This watchdog timer can detect a runaway such that the watchdog timer clear is repeated in short cycle. If the watchdog timer clear is repeated in shorter cycle than the set time (the lowest value watchdog timer can clear), it is regarded as an error and the watchdog interrupt (WDIRQ) is generated.

If the watchdog interrupt (WDIRQ) is generated twice consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

The watchdog timer cannot stop, once it starts operation.

■Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows to detect errors.

Programming of the watchdog timer is generally done in the last step of its programming.

■How to Detect Incorrect Code Execution

The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. In this LSI, the watchdog timer detects errors when,

(1) the watchdog timer overflows.
(2) the watchdog timer clear is happened in the shorter cycle than the watchdog timer clear possible lowest value, set in the watchdog timer control register (WDCTR).

When the watchdog timer detects any error, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI).

■How to Clear Watchdog Timer

The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). The watchdog timer can be cleared regardless of the writing data to the register. The bit-set (BSET) instruction that does not change the value is recommended.

■Watchdog Time-out Period

The watchdog time-out period is decided by the bp2, 1 (WDTS1-0) of the watchdog timer control register (WDCTR) and the system clock (fs). If the watchdog timer is not cleared by this set value, that is regarded as an error and the watchdog interrupt (WDIRQ) of the non maskable interrupt (NMI) is generated.

Table 9-3-1 Watchdog Time-out Period

WDTS1	WDTS0	Watchdog time-out period
0	0	2^{16} X systemclock
0	1	2^{18} X systemclock
1	X	2^{20} X systemclock

System clock is decided by the CPU mode control register (CPUM).

[☞ Chapter 2 2-4. Clock Switching]

The watchdog time-out period is generally decided from the execution time for main routine of program. That should be set the longer cycle than the value of the execution time for main routine divided by natural number (1, 2, , ,). And set the command of the watchdog timer clear to the main routine so that value makes the same cycle.

■The Lowest Value for Watchdog Timer Clear

The lowest value for watchdog timer clear is decided by the bp5, 4, 3 (WDTC2, WDTC1, WDTC0) of the watchdog timer control register (WDCTR).

Table 9-3-2 The Lowest Value for Watchdog Timer Clear

WDTC2	WDTC1	WATC0	Watchdog timer can be cleared at the following cycle or more
0	0	0	no limit
0	0	1	2^{7} X system clock
0	1	0	2^{9} X system clock
0	1	1	2^{11} X system clock
1	0	0	2^{13} X system clock
1	0	1	2^{15} X system clock
1	1	0	2^{17} X system clock
1	1	1	2^{19} X system clock

■Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features as follows ;

(1) In NORMAL, IDLE, SLOW mode, the system clock is counted.
(2) The counting is continued regardless of switching at NORMAL, IDLE, SLOW mode.
(3) In HALT mode, the watchdog timer is stopped.
(4) In STOP mode, the watchdog timer is cleared automatically.
(5) In STOP mode, the watchdog interrupt cannot be generated.
(6) After releasing reset or recovering from STOP, the counting is executed for the period of the oscillation stabilization wait time.

Generally, in the system using STOP mode, if the STOP mode is done or not is divided on the program execution, but, in this case, the counting value of the watchdog timer differs. So, the watchdog interrupt should be prevented by setting the lowest value for watchdog timer clear.

9-3-2 Setup Example

The watchdog timer detects errors. On the following example, the time-out period is set to $2^{18} \times$ system clock, the lowest value for watchdog timer clear is set to $2^{9} \times$ system clock.
An example setup procedure, with a description of each step is shown below.

■Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Set the time-out period. WDCTR (x'03F02') bp2-1 : WDTS1-0 = 01	(1) Set the WDTS1-0 flags of the watchdog timer control register (WDCTR) to "01" to select the time-out period to $2^{18} \times$ system clock.
(2) Set the lowest value for clear. WDCTR (x'03F02') bp5-3 : WDTC2-0 = 010	(2) Set the WDTC2-0 flag of the WDCTR register to "010" to select the lowest value for clear to $2^{9} \times$ system clock.
(3) Start the watchdog timer operation. WDCTR (x'03F02') bp0 : WDEN = 1	(3) Set the WDEN flag of the WDCTR register to start the watchdog timer operation.

The command of setting the WDEN flag to "1" should be done on the last step of the initial setting. If the watchdog control register (WDCTR) is changed after starting the operation, the watchdog interrupt may be generated depending on the setting of the lowest value for clear.

■Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the watchdog timer for the constant clear. Writing to WDCTR (x'03F02') (cf.) BSET (WDCTR) WDEN (bp0 : WDEN = 1)	(1) Clear the watchdog timer by the cycle from $2^{9} \times$ system clock up to $2^{18} \times$ system clock. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. The recommended instruction is the bit-set (BSET), does not change value, for clear.

■Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine. NMICR (x'03FE1') TBNZ (NMICR) WDIR, WDPRO	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt control register (NMICR) is "1" on the interrupt service routine to manage the suitable execution.

The operation, just before the WDOG interrupt may be executed wrongly. Therefore, if the WDOG interrupt is generated, initialize the system.

Chapter 10 Buzzer

10

10-1 Overview

This LSI has a buzzer. It can output the square wave, that multiply by $1/2^9$ to $1/2^{14}$ of the high frequency oscillation clock, or by $1/2^3$ to $1/2^4$ of the low frequency oscillation clock.

10-1-1 Block Diagram

■Buzzer Block Diagram

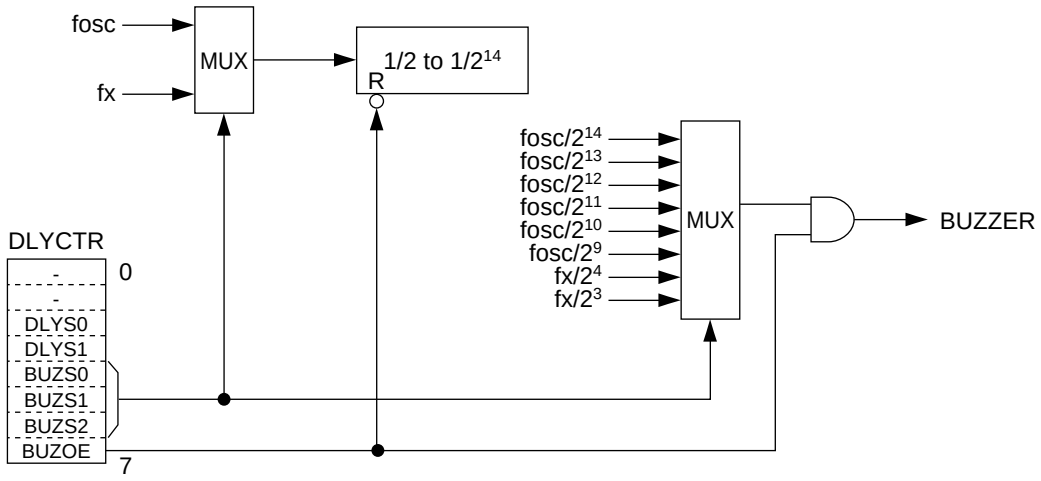


Figure 10-1-1 Block Diagram (Buzzer)

10-2 Control Register

■Oscillation Stabilization Wait Time Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-

(At reset : 0 0 0 0 0 1 - -)

DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	$fs/2^{14}$
	1	$fs/2^{10}$
1	0	$fs/2^{6}$
	1	$fs/2^{2}$

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{10}$.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	P06 port output
1	P06 buzzer output

Figure 10-2-1 Oscillation Stabilization Wait Time Control Register (DLYCTR : x'03F03', R/W)

10-3 Operation

10-3-1 Operation

■Buzzer

Buzzer outputs the square wave, having frequency $1/2^9$ to $1/2^{14}$ of the high oscillation clock (fosc), or $1/2^3$ to $1/2^4$ of the low oscillation clock (fx). The BUZS 2, 1, 0 flag of the oscillation stabilization wait control register (DLYCTR) set the frequency of buzzer output. The BUZOE flag of the oscillation stabilization wait control register (DLYCTR) sets buzzer output ON / OFF.

■Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the high oscillation clock (fosc) or the low oscillation clock (fx) and the bit 6, 5, 4 (BUZS2, BUZS1, BUZS0) of the oscillation stabilization wait control register (DLYCTR).

Table 10-3-1 Buzzer Output Frequency

fosc	fx	BUZS2	BUZS1	BUZS0	Buzzer output frequency
20 MHz	-	0	0	0	1.22 kHz
20 MHz	-	0	0	1	2.44 kHz
20 MHz	-	0	1	0	4.88 kHz
8.38 MHz	-	0	1	0	2.05 kHz
8.38 MHz	-	0	1	1	4.09 kHz
2 MHz	-	1	0	0	1.95 kHz
2 MHz	-	1	0	1	3.91 kHz
-	32 kHz	1	1	0	2 kHz
-	32 kHz	1	1	1	4 kHz

10-3-2 Setup Example

Buzzer outputs the square wave of 2 kHz from P06 pin. It is used 8.38 MHz as the high oscillation clock (fosc).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency. DLYCTR (x'3F03') bp6-4 : BUZS2-0 = 010	(1) Set the BUZS2-0 flag of the oscillation stabilization wait control register (DLYCTR) to "010" to select fosc/2^{12} to the buzzer frequency. When the high oscillation clock fosc is 8.38 MHz, the buzzer output frequency is 2.05 kHz.
(2) Set P06 pin. P0OUT (x'3F10') bp6 : P0OUT6 = 0 P0DIR (x'3F30') bp6 : P0DIR6 = 1	(2) Set the output data P0OUT6 of P06 pin to "0", and set the direction control P0DIR6 of P06 pin to "1" to select output mode. Port 06 pin outputs low level.
(3) Buzzer output ON. DLYCTR (x'3F03') bp7 : BUZOE = 1	(3) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by P06 pin.
(4) Buzzer output OFF. DLYCTR (x'3F03') bp7 : BUZOE = 0	(4) Set the BUZOE flag of the oscillation stabilization wait control register to (DLYCTR) "0" to clear, and P06 pin outputs low level.

Chapter 11 Serial Interface 0

11

11-1 Overview

This LSI contains a serial interface 0 that can be used for both communication types of clock synchronous and UART (duplex).

11-1-1 Functions

Table 11-1-1 shows functions of serial interface 0.

Table 11-1-1 Serial Interface 0 Functions

Communication style	clock synchronous	UART (duplex)
Interrupt	SC0TIRQ	SC0TIRQ (on transmission completion) SC0RIRQ (on reception completion)
Used pins	SBO0,SBI0,SBT0	TXD,RXD
3 channels type	√	-
2 channels type	√ (SBO0, SBT0)	√
1 channel type	-	√ (TXD)
Specification of transfer bit count / Frame selection	1 to 8 bits	7 bits + 1STOP 7 bits + 2STOPs 8 bits + 1STOP 8 bits + 2STOPs
Selection of parity bit	-	√
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	√	only "enable start condition" is available
Specify of the first transfer bit	√	√
Specify of input edge / output edge	√	-
Continuous operation	√	√
Internal clock 1/8 dividing	√	only 1/8 dividing is available
Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 3 output External clock	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 3 output
Maximum transfer rate	2.5 MHz	300 kbps (standard 300 bps to 38.4 kbps) (timer 3 output)
fosc : Machine clock (High speed oscillation) fs : System clock [☞ Chapter 2 2-5. Clock Switching]		

11-1-2 Block Diagram

■Serial Interface 0 Block Diagram

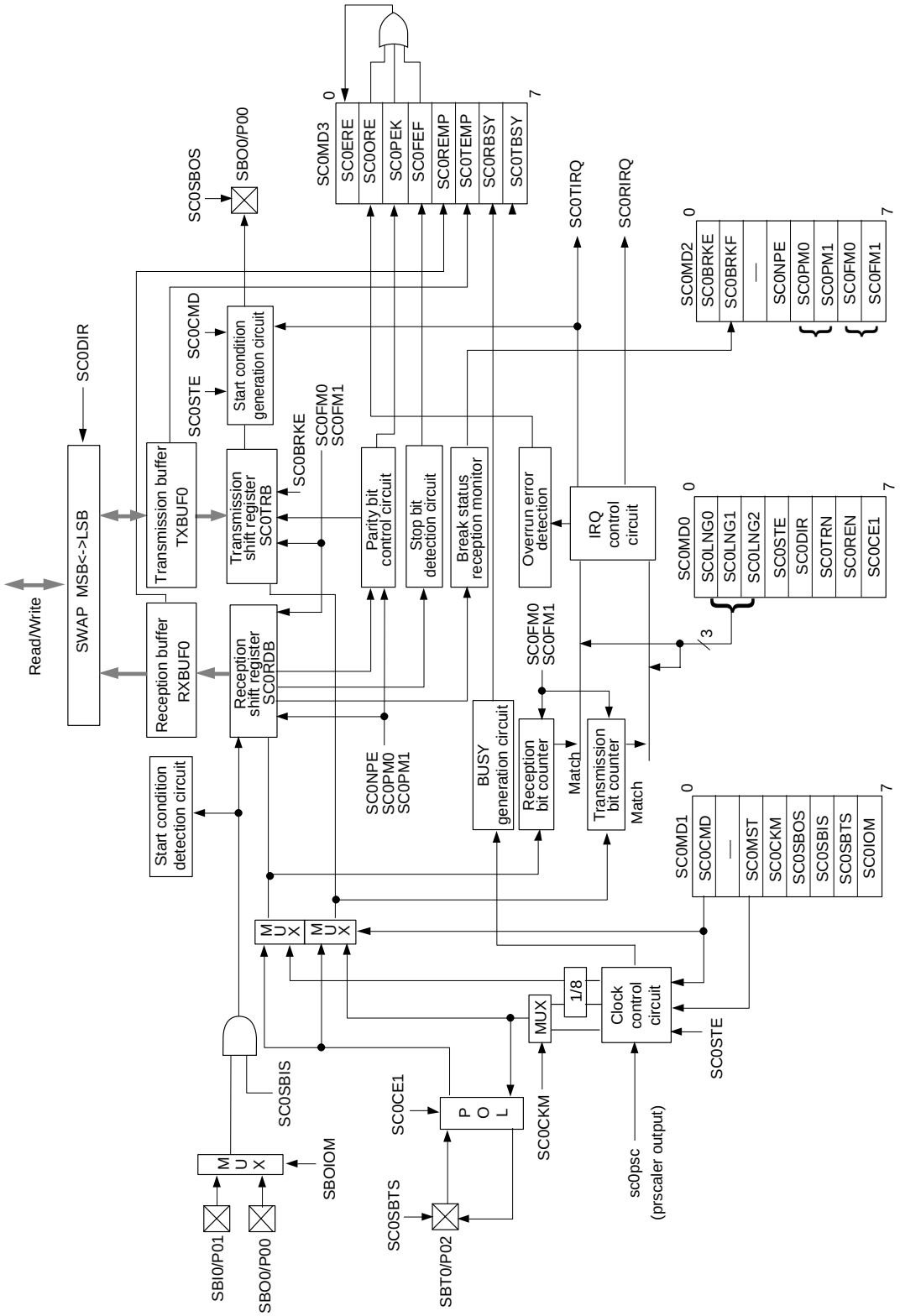


Figure 11-1-1 Serial Interface 0 Block Diagram

11-2 Control Registers

11-2-1 Registers

Table 11-2-1 shows registers to control serial interface 0.

Table 11-2-1 Serial Interface 0 Control Registers

	Regoster	Address	R/W	Function	Page
Serial 0	SC0MD0	X'03F90'	R/W	Serial interface 0 mode register 0	XI - 6
	SC0MD1	X'03F91'	R/W	Serial interface 0 mode register 1	XI - 7
	SC0MD2	X'03F92'	R/W	Serial interface 0 mode register 2	XI - 8
	SC0MD3	X'03F93'	R	Serial interface 0 mode register 3	XI - 9
	RXBUF0	X'03F94'	R	Serial interface 0 reception data buffer	XI - 5
	TXBUF0	X'03F95'	R/W	Serial interface 0 transmission data buffer	XI - 5
	SC0ODC	X'03F96'	R/W	Serial interface 0 port control register	XI - 10
	SC0CKS	X'03F97'	R/W	Serial interface 0 transfer clock selection register	V - 9, XI - 11
	PSCMD	X'03F6F'	R/W	Prescaler control register	V - 6
	P0DIR	X'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLU	X'03F40'	R/W	Port 0 pull-up control register	IV - 7
	SC0RICR	X'03FF5'	R/W	Serial interface 0 reception interrupt control register	III - 30
	SC0TICR	X'03FF6'	R/W	Serial interface 0 transmission interrupt control register	III - 31

R/W : Readable / Writable

R : Readable only

11-2-2 Data Buffer Registers

Serial Interface 0 has each 8-bit data buffer register for transmission, and for reception.

■Serial Interface 0 Received Data Buffer (RXBUF0)

	7	6	5	4	3	2	1	0	
RXBUF0	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00	(At reset : X X X X X X X X)

Figure 11-2-1 Serial Interface 0 Received Data Buffer (RXBUF0 : x'03F94', R)

■Serial Interface 0 Transmissin Data Buffer (TXBUF0)

	7	6	5	4	3	2	1	0	
TXBUF0	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00	(At reset : X X X X X X X X)

Figure 11-2-2 Serial Interface 0 Transmission Data Buffer (TXBUF0 : x'03F95', R/W)

11-2-3 Mode Registers

■Serial Interface 0 Mode Register 0 (SC0MD0)

	7	6	5	4	3	2	1	0
SC0MD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0

(At reset : 0 0 0 0 0 1 1 1)

SC0LNG2	SC0LNG1	SC0LNG0	Synchronous serial transfer bit count
0	0	0	1 bits
		1	2 bits
	1	0	3 bits
		1	4 bits
1	0	0	5 bits
		1	6 bits
	1	0	7 bits
		1	8 bits

SC0STE	Start condition selection
0	Disable start condition
1	Enable start condition

SC0DIR	First bit to be transfered
0	MSB first
1	LSB first

SC0TRN	Transmission data polarity selection
0	Positive polrity
1	Negative polrity

SC0REN	Received data polarity selection
0	Positive polrity
1	Negative polrity

SC1CE1	Transmission data output edge	Received data input edge
0	falling	rising
1	rising	falling

Figure 11-2-3 Serial Interface 0 Mode Register 0 (SC0MD0 : x'03F90', R/W)

■Serial Interface 0 Mode Register 1 (SC0MD1)

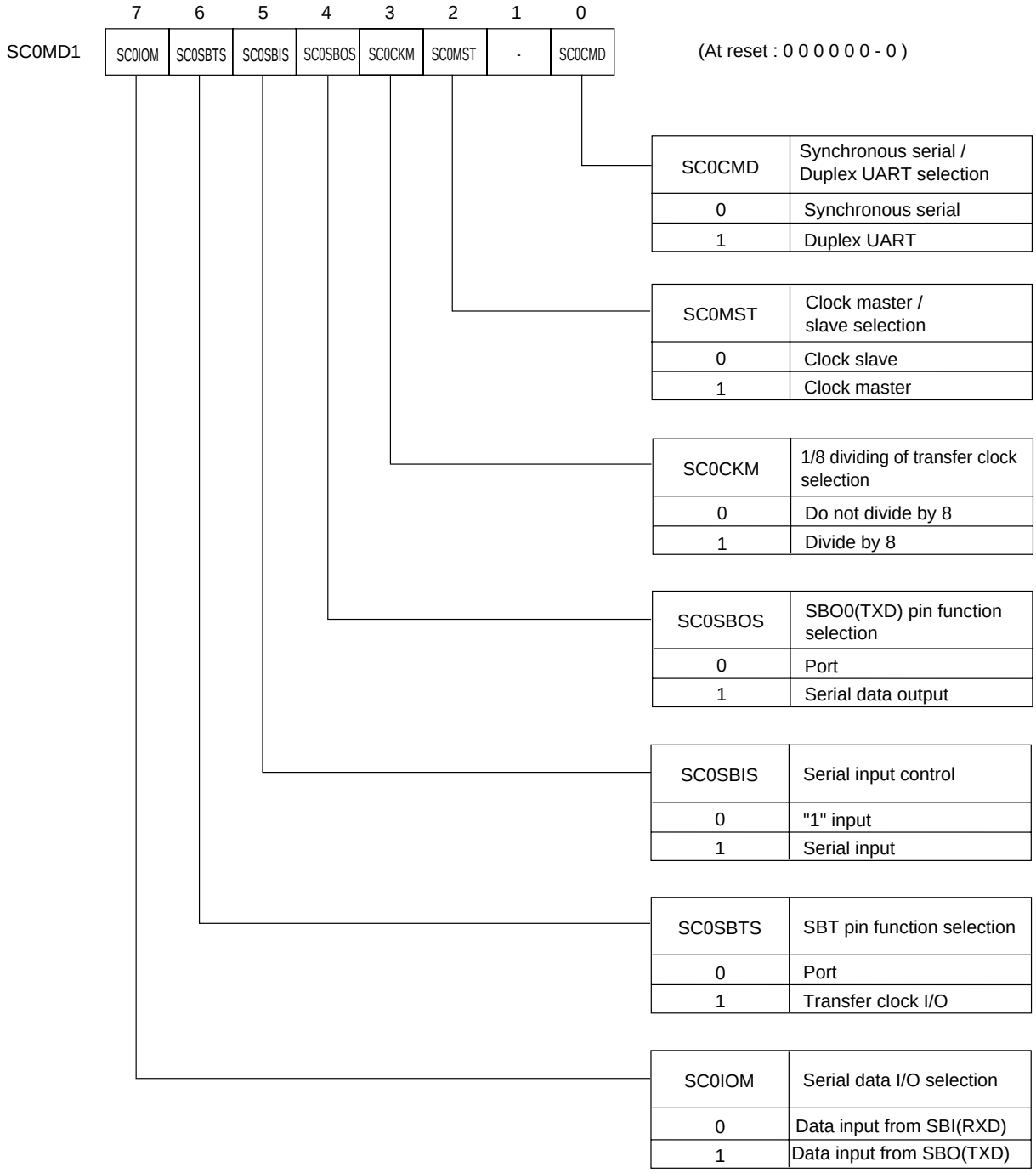
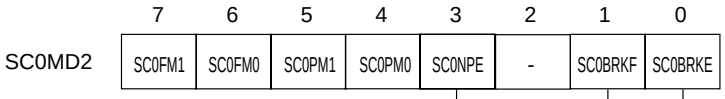

7 6 5 4 3 2 1 0
SC0MD1
SC0IOM SC0SBTS SC0SBIS SC0SBOS SC0CKM SC0MST - SC0CMD
(At reset : 0 0 0 0 0 0 - 0)
SC0CMD | Synchronous serial / Duplex UART selection
0 | Synchronous serial
1 | Duplex UART
SC0MST | Clock master / slave selection
0 | Clock slave
1 | Clock master
SC0CKM | 1/8 dividing of transfer clock selection
0 | Do not divide by 8
1 | Divide by 8
SC0SBOS | SBO0(TXD) pin function selection
0 | Port
1 | Serial data output
SC0SBIS | Serial input control
0 | "1" input
1 | Serial input
SC0SBTS | SBT pin function selection
0 | Port
1 | Transfer clock I/O
SC0IOM | Serial data I/O selection
0 | Data input from SBI(RXD)
1 | Data input from SBO(TXD)

Figure 11-2-4 Serial Interface 0 Mode Register 1 (SC0MD1 : x'03F91', R/W)

■Serial Interface 0 Mode Register 2 (SC0MD2)

SC0BRKF flag is only for reading.



SC0BRKE	Break status transmit control
0	Data
1	Break

SC0BRKF (*)	Break status receive monitor
0	Data
1	Break

(*) Only read access is available.

SC0NPE	Parity enable
0	Enable parity bit
1	Disable parity bit

SC0PM1	SC0PM0	Added bit specification	
		Transmission	Reception
0	0	Add "0"	Check for 0
	1	Add "1"	Check for 1
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC0FM1	SC0FM0	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bit
	1	8 data bits + 2 stop bits

Figure 11-2-5 Serial Interface 0 Mode Register 2 (SC0MD2 : x'03F92', R/W)

■Serial Interface 0 Mode Register 3 (SC0MD3)

All flags are only for reading.

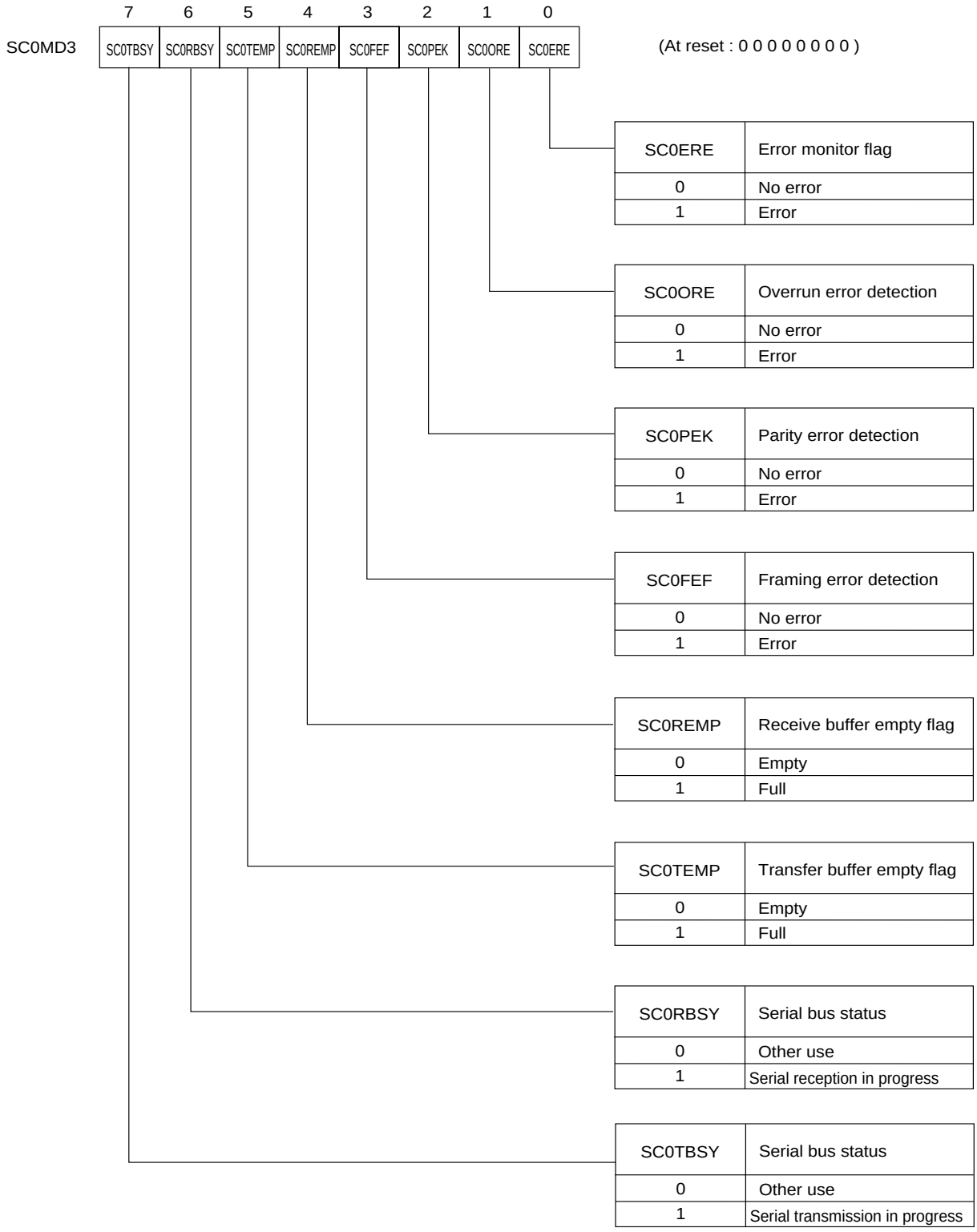


Figure 11-2-6 Serial Interface 0 Mode Register 3 (SC0MD3: x'03F93', R)

■Serial Interface 0 Port Control Register (SC0ODC)

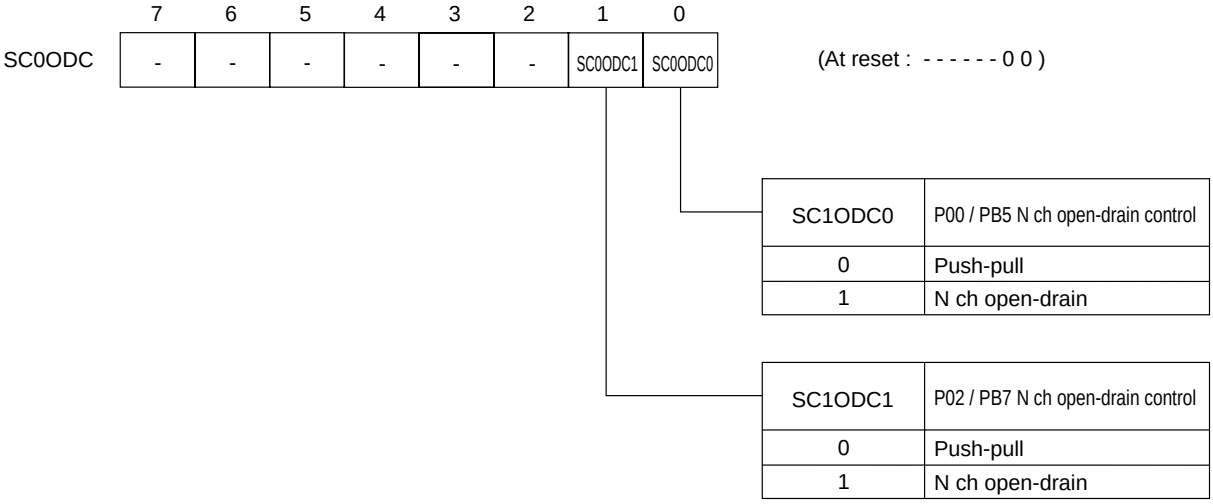


Figure 11-2-7 Serial Interface 0 Port Control Register (SC0ODC : x'03F96', R/W)

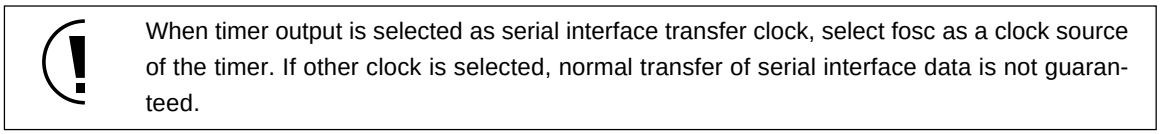
■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)

	7	6	5	4	3	2	1	0
SC0CKS	—	—	—	—	—	SC0PSC2	SC0PSC1	SC0PSC0

(At reset : - - - - - X X X)

SC0PSC2	SC0PSC1	SC0PSC0	Clock selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/64
1	0	0	fs/2
		1	fs/4
	1	0	Forbidden
		1	Timer 3 output

Figure 11-2-8 Serial Interface 0 Tranfer Clock Selection Register (SC0CKS : x'03F97', R/W)



When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

11-3 Operation

Serial Interface 0 can be used for both clock synchronous and duplex UART.

11-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 11-3-1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF0, or by receiving a start condition. Except during communication, the input signal from SBT pin is masked to prevent errors by noise or so. This mask can be released automatically by setting a data to TXBUF0(access to the TXBUF0 register), or by inputting a start condition to the data input pin. Therefore, at slave communication, set data to TXBUF0, or input an external clock after a start condition is input.

Table 11-3-1 Synchronous Serial Interface Activation Factor

<table>
<tr><td rowspan="2"></td><td colspan="2">Activation factor</td></tr>
<tr><td>Transmission</td><td>Reception</td></tr>
<tr><td rowspan="2">at master</td><td rowspan="2">Set transmission data</td><td>Set dummy data</td></tr>
<tr><td>Input start condition</td></tr>
<tr><td rowspan="2">at slave</td><td rowspan="2">Input clock after
transmission data is set</td><td>Input clock
after dummy data is set</td></tr>
<tr><td>Input clock
after start condition is input</td></tr>
</table>

■Transfer bit Setup

The transfer bit count is selected from 1 bit to 8 bits. Set them by the SC0LNG 2 to 0 flag of the SC0MD0 register (at reset : 111). The SC0LNG 2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT pin is masked to prevent errors by noise. At slave communication, set data to TXBUF0 or input a clock to SBT pin after a start condition is input.

■Start Condition Setup

The SC0STE flag of the SC0MD0 register sets if a start condition is enabled or not. If a start condition is selected, and input at communication, a bit counter is cleared to restart the communication. The start condition is regarded that when a clock line (SBT pin) is "H", data line (SBI pin (with 3 lines) or SBO pin (with 2 lines)) is changed from "H" to "L". Both the SC0SBOS flag and the SC0SBIS flag of the SC0MD1 register should be set to "0", before the start condition setup is changed.

■First Transfer bit Setup

The SC0DIR flag of the SC0MD0 register can set the transfer first bit. MSB first or LSB first can be selected.

■Transmission Data Buffer

The transmission data buffer, TXBUF0 is a buffer of reserve that stores data to load the internal shift register. Data to be transfered should be set to the transmission data buffer, TXBUF0, to be loaded to the internal shifr register automatically. The first data loading to the internal shift register is done at the same timing of the data setting to TXBUF0.

■Received Data Buffer

The received data buffer RXBUF0 is a buffer of reserve that pushed the received data in the internal shift register. After the communication complete interrupt SC0TIRQ is generated, all data stored in the internal shift register are stored to the received data buffer RXBUF0 automatically. RXBUF0 can store data up to 1 byte. RXBUF0 is rewritten in everytime when communication is completed, so read out data of RXBUF0 till the next receive is completed. The received data buffer empty flag SC0REMP is set to "1" at the same time SC0TIRQ is generated. SC0REMP is cleared to "0" after RXBUF0 is read out.

If a start condition is input to restart during communication, the transmission data is not valid. Set the transmission data to TXBUF0 again to operate the transmission again.

Start condition should be switched after both the SC0SBOS and the SC0SBIS flags of the SC0MD1 register are set to "0". If they are not set to "0", the switching is not valid.

RXBUF0 is rewritten everytime when communication is completed. At continuous communication, data of RXBUF0 should be read out until the next reception is completed.

■Tranfer bit Count and First Transfer bit

When the transfer bit is 1 bit to 7 bits, the data storing method to the transmission data buffer TXBUF0 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0 for storing. When there are 6 bits to be transfered, as shown on figure 11-3-1, if data "A" to "F" are stored to bp2 to bp7 of TXBUF0, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUF0 for storing. When there are 6 bits to be transfered, as shown on figure 11-3-2, if data "A" to "F" are stored to bp0 to bp5 of TXBUF0, the transmission is operated from "A" to "F".

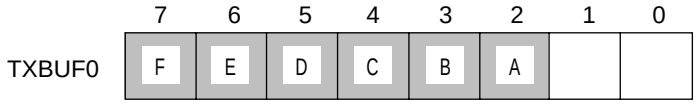


Figure 11-3-1 Transfer bit Count and First Transfer bit (starting with MSB)

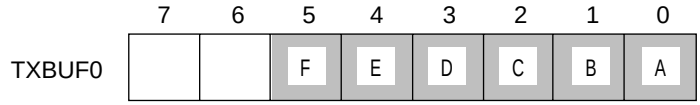


Figure 11-3-2 Transfer bit Count and First Transfer bit (starting with LSB)

■Receive bit Count and First Transfer bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit. At MSB first, data are stored to the lower bits of RXBUF0. When there are 6 bits to be transfered, as shown on figure 11-3-3, if data "A" to "F" are stored to bp0 to bp5 of RXBUF0, the transmission is operated from "F" to "A". At LSB first, data are stored to the upper bits of RXBUF0. When there are 6 bits to be transfered, as shown on figure 11-3-4, if data "A" to "F" are stored to bp2 to bp7 of RXBUF0, the transmission is operated from "A" to "F".

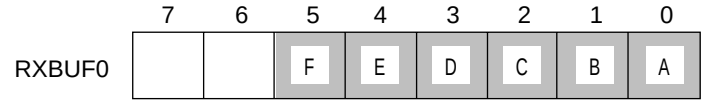


Figure 11-3-3 Receive bit Count and Transfer First bit (starting with MSB bit)

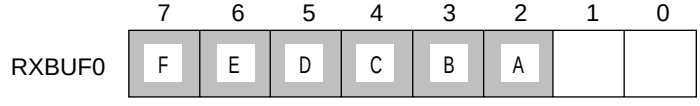


Figure 11-3-4 Receive bit Count and Transfer First bit (starting with LSB bit)

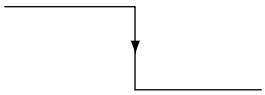
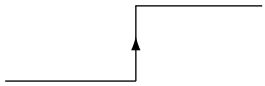
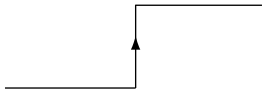
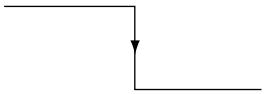
■Continuous Communication

This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is automatically set to communicate continuously. Data setup to TXBUF0 should be done till the communication complete interrupt SC0TIRQ is generated after the former data is set. At master communication, there is a suspension of communication for 3 transfer clocks till the next transmission clock is output after the SC0TIRQ generation.

■Input Edge / Output Edge Setup

The SC0CE 1 flag of the SC0MD0 register set an output edge of the transmission data, an input edge of the received data. As the SC0CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC0CE1="0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table 11-3-2 Transmission Data Output Edge and Received Data Input Edge

SC0CE1	Transmission data output edge	Received data input edge
0		
1		

■Change of Polarity of Transmission / Reception Data

It is possible to change the polarity of the transmission / reception data. When the SC0REN flag of SC0MD0 register is set to "1", the polarity inverted input signals from the data input pins are loaded to reception shift register. When the SC0TRN flag of SC0MD0 register is set to "1", the inverted signals of the data set in the transmission buffer TXBUF0 is output to the data output pins.

■Clock Setup

The SC0CKS register selects a clock source from the special prescaler and timer output. The special prescaler starts its operation after the PSCMD (x'03F6F') register selects "prescaler operation". The SC0MST flag of the SC0MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or below to the external clock, by the SC0CKS register. That is happened, because the interrupt flag SC0TIRQ is generated by the internal clock. Here is the internal clock source that can be set by the SC0CKS register. Also, the SC0CKM flag of the SC0MD1 register can divide the internal clock by 8.

Table 11-3-3 Synchronous Serial Interface Internal Clock Source

	Serial 0
Internal clock	fosc/2
	fosc/4
	fosc/16
	fosc/64
	fs/2
	fs/4
	Timer 3 output

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

■Data Input Pin Setup

3 channels type (clock pin (SBT pin), data output pin (SBO pin), data input pin (SBI pin)) or 2 channels type (clock pin (SBT pin), data I/O pin (SBO pin)) can be selected as a communication mode. SBI pin can be used for only serial data input. SBO pin can select serial data input or output. The SC0IOM flag of the SC0MD1 register can select if the serial data is input to SBI pin or SBO pin. When "data input from SBO pin" is selected to set the 2 lines type, the P0DIR0 flag of the P0DIR register controls direction of SBO pin to switch transmission / reception. At this time, SBI pin can be used as a general port, too.

The transfer speed should be up to 2.5 MHz. If the transfer clock is over 2.5 MHz, the transmission data may not be sent correctly.

At reception, if SC0IOM of the SC0MD1 register is set to "1" and "serial data input from SBO" is selected, SBI pin can be used as a general port.

■Reception Buffer Empty Flag

When SC0TIRQ is generated, data is automatically stored to RXBUF0 from the internal shift register. If data is stored to the shift register RXBUF0, the reception buffer empty flag SC0REMP of the SC0MD3 register is set to "1". This indicates that the received data is going to read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■Transmission Buffer Empty Flag

If any data is set to TXBUF0 again, during communication (after setting data to TXBUF0 and before the communication complete interrupt SC0TIRQ is generated), the transmission buffer empty flag SC0TEMP of the SC0MD3 register is set to "1". This indicates that the next transmission data is going to be loaded. Data is loaded to the inside shift register from TXBUF0 by generation of SC0TIRQ, and the next transfer is started as SC0TEMP is cleared to "0".

■Overrun Error and Error Monitor Flag

If, after reception complete, the next data has been already received before reading out of the data of the received data buffer RXBUF0, overrun error is generated and the SC0ORE flag of the SC0MD3 register is set to "1". And at the same time, the error monitor flag SC0RE is set to indicate that error is occurred on reception. The SC0ORE flag holds the status unless the data of RXBUF0 is read out. SC0ERE is cleared as SC0ORE flag is cleared. These error flags have no effect on communication operation.

■Reception BUSY Flag

When any data is set to TXBUF0 or when the SC0SBIS flag of the SC0MD1 register is "1" as start condition is input, the SC0RBSY flag of the SC0MD3 register is set to "1". And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared to "0". And, during continuous communication, the SC0RBSY flag is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated, SC0RBSY is cleared to "0". If the SC0SBIS flag is set to "0" during communication, the SC0RBSY flag is cleared to "0".

■Transmission BUSY Flag

When any data is set to TXBUF0 or when the SC0SBOS flag of the SC0MD1 register is "1" as start condition is input, the SC0TBSY flag of the SC0MD3 register is set to "1". And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared to "0". And, during continuous communication, the SC0TBSY falg is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated, SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0" during communication, the SC0TBSY flag is cleared to "0".

■Emergency Reset

This serial interface contains emergency reset for abnormal operation. For emergency reset, the SC0SBOS flag and the SC0SBIOS flag of the SC0MD1 register should be set to "0" (SBO pin : port, input data : "1" input). At emergency reset, the status registers (the SC0BRKF flag of the SC0MD2 register, all flags of the SC0MD3 register) are initialized as they are set at reset, but the control register holds the set value.

■Last bit of Transfer Data

Table 11-3-4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. After data output holding period of the last bit, "H" is output.

Table 11-3-4 Last bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	1 bit data length × 1 to 1.5	

■Other Control Flag Setup

Table 11-3-5 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table 11-3-5 Other Control Flag

Register	Flag	Detail
SC0MD2	SC0BRKF	Brake status reception monitor
	SC0NPE	Parity is enabled
	SC0PM1 to 0	Added bit specification
	SC0FM1 to 0	Frame mode specification
SC0MD3	SC0PEK	Parity error detection
	SC0FEF	Frame error detection

■Trasnmission Timing

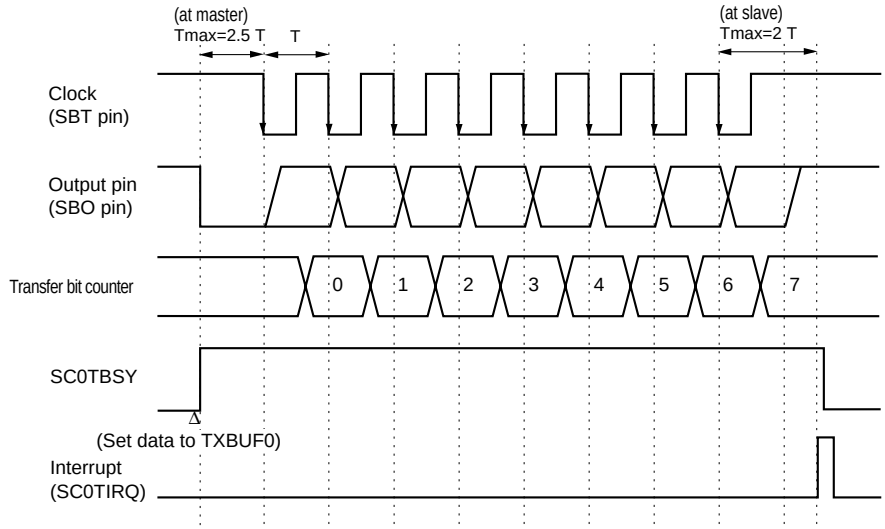


Figure 11-3-5 Transmission Timing (at falling edge, start condition is enabled)

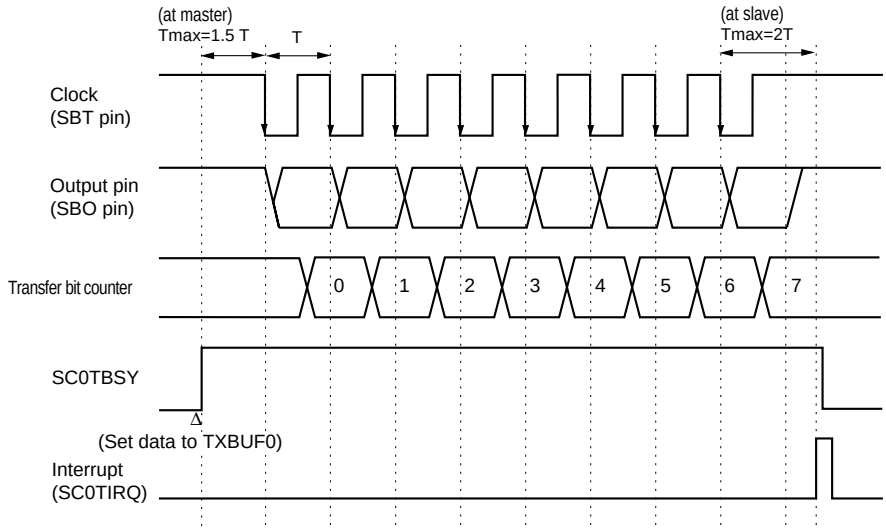


Figure 11-3-6 Transmission Timing (at falling edge, start condition is disabled)

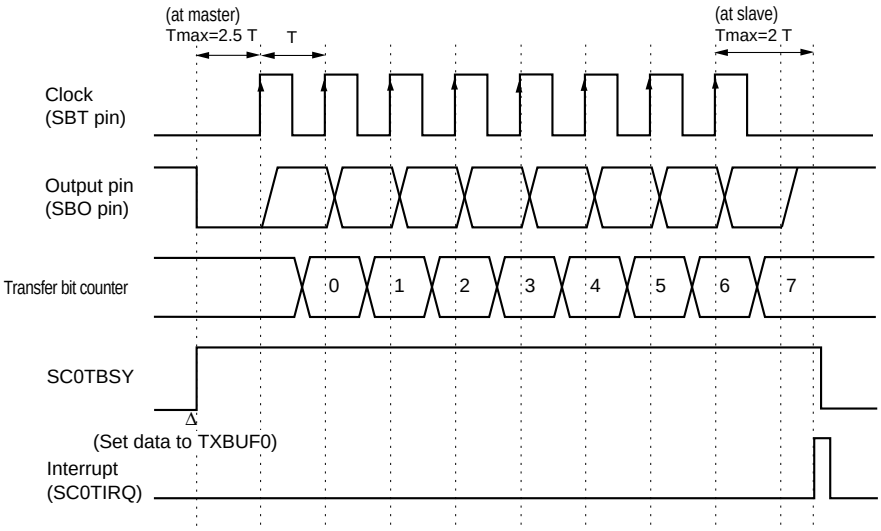


Figure 11-3-7 Transmission Timing (at rising edge, start condition is enabled)

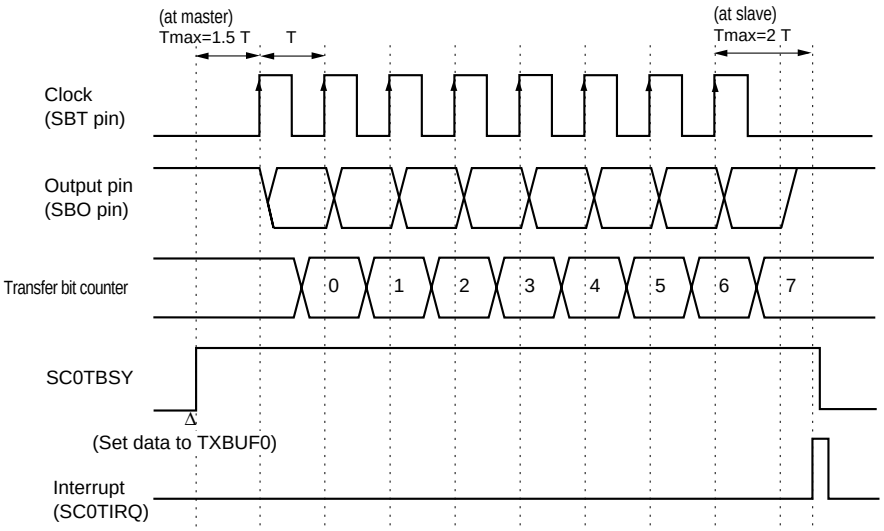


Figure 11-3-8 Transmission Timing (at rising edge, start condition is disabled)

■Reception Timing

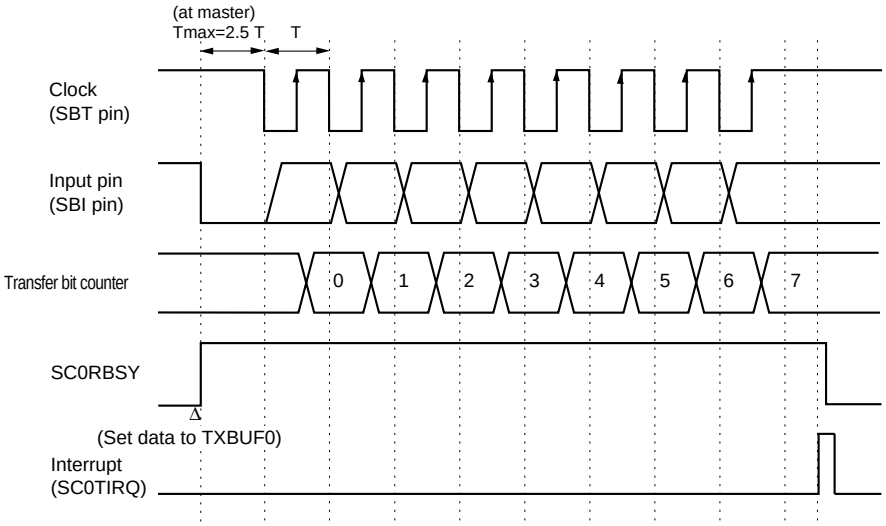


Figure 11-3-9 Reception Timing (at rising edge, start condition is enabled)

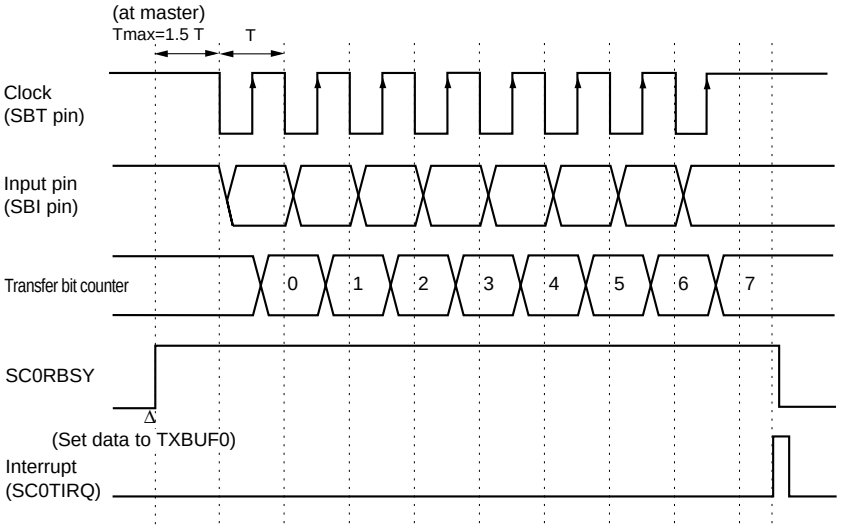


Figure 11-3-10 Reception Timing (at rising edge, start condition is disabled)

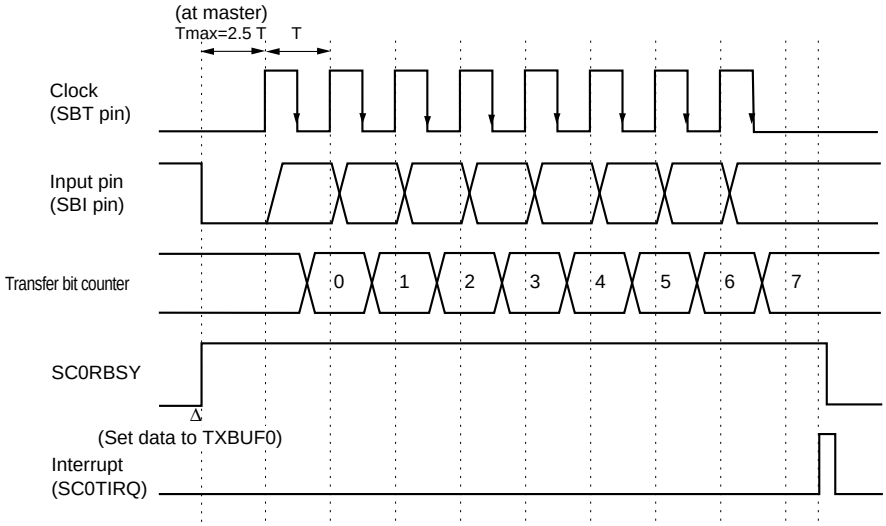


Figure 11-3-11 Reception Timing (at falling edge, start condition is enabled)

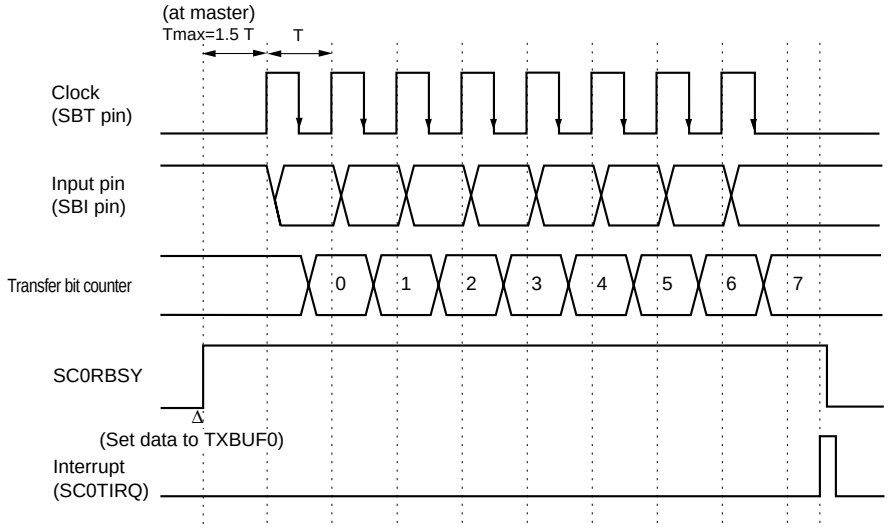


Figure 11-3-12 Reception Timing (at falling edge, start condition is disabled)

■Transmission / Reception Timing

When transmission and reception are operated at the same time, set the SC0CE1 flag of the SC0MD0 register to "0" or "1". Data is received at the opposit output edge of the transmission data, so that the input edge of the received data should be the opposide output edge of the transmission data from the other side.

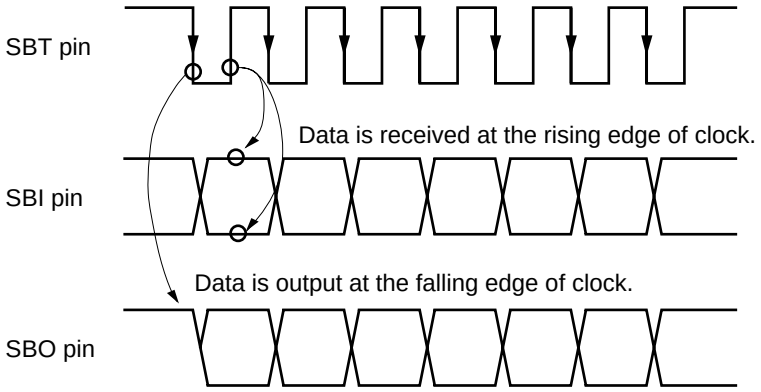


Figure 11-3-13 Transmission / Reception Timing
(Reception : at rising edge, Transmission : at falling edge)

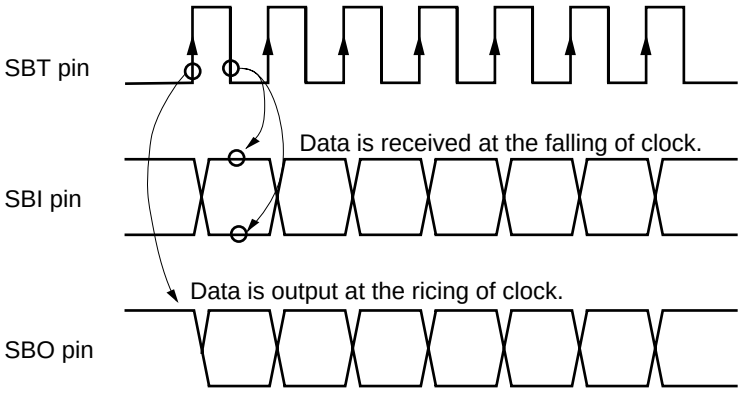


Figure 11-3-14 Transmission / Reception Timing
(Reception : at falling edge, Transmission : at rising edge)

■Pins Setup (with 3 channels, at transmission)

Table 11-3-6 shows the setup for synchronous serial interface pin with 3 channels (SBO pin, SBI pin, SBT pin) at transmission.

Table 11-3-6 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Port pin	P00	P01	P02	
SBI / SBO pin	SBI / SBO independent		-	
	SC0MD1(SC1IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up / Pull-down	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

■Pins Setup (with 3 channels, at reception)

Table 11-3-7 shows the setup for synchronous serial interface pin with 3 channels (SBO7 pin, SBI pin, SBT pin).

Table 11-3-7 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Port pin	P00	P01	P02	
SBI / SBO pin	SBI / SBO independent		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR(P0DIR1)	P0DIR(P0DIR2)	
Pull-up / Pull-down	-	-	Added / Not added	Added / Not added
			P0PLU(P0PLU2)	

■Pins Setup (with 3 channels, at transmission / reception)

Table 11-3-8 shows the setup for synchronous serial interface pin with 3 channels (SBO pin, SBI pin, SBT pin) at transmission / reception.

Table 11-3-8 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Port pin	P00	P01	P02	
SBI / SBO pin	SBI / SBO independent		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR0)	P0DIR(P0DIR1)	P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

■Pins Setup (with 2 channels, at transmission)

Table 11-3-9 shows the setup for synchronous serial interface pin with 2 channels (SBO pin, SBT pin) at transmission. SBI pin can be used as a port.

Table 11-3-9 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin		Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Port pin	P00		P02	
SBI / SBO pin	SBI/SBO connected		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

■Pins Setup (with 2 channels, at reception)

Table 11-3-10 shows the setup for synchronous serial interface pin with 2 channels (SBO pin, SBT pin) at reception. SBI pin can be used as a port.

Table 11-3-10 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO pin	SBI pin	SBT pin	
			Internal clock	External clock
Port pin	P00		P02	
SBI / SBO pin	SBI / SBO connected		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	Input mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	-	-	Added / Not added	Added / Not added
			P0PLU(P0PLU2)	

11-3-2 Setup Example

■Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 0 is shown. Table 11-3-11 shows the conditions at transmission / reception.

Table 11-3-11 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	set to		Setup item	set to
SBI / SBO pin	Independent (with 3 channels)		Clock source	fs/2
Transfer bit count	8 bits		Clock source 1/8 dividing	divided by 8
Start condition	none		SBT / SBO pin style	Nch open-drain
First transfer bit	MSB		SBT pin pull-up resistor	Added
Input edge	falling edge		SBO pin pull-up resistor	Added
Output edge	rising edge		Serial 0 communication complete interrupt	Enable
Clock	Internal clock			

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select "prescaler operation".
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0= 100 bp3 : SC0TMSEL= 0	(2) Select the clcok source by the SC0CKS register. Set bp3-0 to "0100" to select "fs/2".
(3) Control the pin type. SC0ODC (x'3F96') bp1-0 : SC0ODC1-0= 11 P0PLUD (x'3F40') bp2, 0 : P0PLUD2, 0= 1, 1	(3) Set the SC0ODC1-0 flag of the SC0ODC register to "11" to select "N-ch open drain" to the SBO/SBT pin. Set the P0PLUD2, 0 flag of the P0PLUD register to "1, 1" to add pull-up/ pull-down resistor.
(4) Control the pin direction. P0DIR (x'3F30') bp2-0 : P0DIR2-0 = 101	(4) Set the P0DIR2-0 flag of the port 0 pindirection control register (P0DIR) to "101" to set P00, P02 "output mode", and to set P01 "input mode".
(5) Set the SC0MD0 register. Select the transfer bit count. SC0MD0 (x'3F90') bp2-0 : SC0LNG2-0= 111	(5) Set the SC0LNG2-0 flag of the serial 0 mode register (SC0MD0) to "111" to set the transfer bit count "8 bits".

Setup Procedure	Description
(6) Select the start condition. SC0MD0 (x'3F90') bp3 : SC0STE = 0	(6) Set the SC0STE flag of the SC0MD0 register to "0" to disable start condition.
(7) Select the first bit to be transfered. SC0MD0 (x'3F90') bp4 : SC0DIR = 0	(7) Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
(8) Select the transfer edge. SC0MD0 (x'3F90') bp7 : SC0CE1 = 1	(8) Set the SC0CE1 flag of the SC0MD0 register to "1" to set the transmission data output edge "rising" and the received data input edge "falling".
(9) Set the SC0MD2 register Control the output data. SC0MD2 (x'3F92') bp0 : SC0BRKE = 0	(9) Set the SC0BRKE flag of the SC0MD2 register to "0" to select "serial data transmission".
(10) Set other mode registers. SC0MD2 (x'3F92') bp7-3	(10) No need at synchronous serial communication.
(11) Set the SC0MD1 register. Select the communication type. SC0MD1 (x'3F91') bp0 : SC0CMD = 0	(11) Set the SC0CMD flag of the SC0MD1 register to "0" to select "synchronous serial".
(12) Select the transfer clock. SC0MD1 (x'3F91') bp2 : SC0MST = 1 bp3 : SC0CKM = 1	(12) Set the SC0MST flag of the SC0MD1 register to "1" to select clock master (inside clock). Set the SC0CKM flag to "1" to select "divide by 8" for source clock.
(13) Control the pin function. SC0MD1 (x'3F91') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp6 : SC0SBTS = 1 bp7 : SC0IOM = 0	(13) Set the SC0SBOS, SC0SBIS, SC0SBTS flag of the SC0MD1 register to "1" to set SBO pin "serial data output", SBI pin "serial data input", and SBT pin "serial clock I/O". Set the SC0IOM flag "0" to set serial data input from SBI pin.
(14) Set the interrupt level. SC0TICR (x'3FF6') bp7-6 : SC0TLV1-0= 10	(14) Set the interrupt level by the SC0TLV1-0 flag of the serial 0 transmission interrupt control register (SC0TICR). (Set level 2.)

Setup Procedure	Description
(15) Enable the interrupt. SC0TICR (x'3FF6') bp1 : SC0TIE = 1	(15) Set the SC0TIE flag of the SC0TICR register to "1" to enable interrupts. If any interrupt request flag (SC0TIR of the SC0TICR register) is already set, clear SC0TIR before an interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(16) Start serial transmission. Transmission data→TXBUF0 (x'3F95') Received data→input to SBI pin.	(16) Set the transmission data to the serial transmission data buffer TXBUF0. Then, an internal clock is generated to start transmission / reception. After the transmission is finished, serial0 transmission interrupt SC0TIRQ is generated.

Note : Each procedure (5) to (8), (9) to (11), and (11) to (13) can be set at the same time.

When only reception with 3 channels are operated, set SC0SBOS of the SC0MD1 register to "0" and select a port. The SBO pin can be used as a general port.

When SBO / SBI pin are connected for communication with 2 lines, the SBO pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIS of the SC0MD1 register to "1", always, to select "serial data input". The SBI pin can be used as a general port.

This serial interface contains a emergency reset function. If the communication should be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (except Table 11-2-1 : TXBUF0, RXBUF0) are set.

Transfer rate of transfer clock set by SC0CKS register should be under 2.5 MHz.

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

11-3-3 UART Serial Interface

Serial 0 can be used for duplex UART communication. Table 11-3-12 shows UART serial interface functions.

Table 11-3-12 UART Serial Interface Functions

Communication style	UART(duplex)
Interrupt	SC0TIRQ(transmission), SC0RIRQ(reception)
Used pins	TXD(output, input) RXD(input)
Specification the first transfer bit	MSB / LSB
Selection of parity bit	√
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOPs 8 bits + 1 STOP 8 bits + 2 STOPs
Continuous operation	√
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

■Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer TXBUF0, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■Transmission

Data transfer is automatically started by setting data to the transmission data buffer TXBUF0. When the transmission is completed, the serial 0 transmission interrupt SC0TIRQ is generated.

■Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial 0 reception interrupt SC0RIRQ is generated.

■Duplex communication

On duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■Transfer bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC0FM1 to 0 flag of the SC0MD2 register. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial transfer bit count selection flag SC0LNG2 to 0 is no more valid.

■Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD pin), data input pin (RXD pin)), or with 1 channel (data I/O pin TXD pin). The RXD pin can be used only for serial data input. The TXD pin can be used for serial data input or output. The SC0IOM flag of the SC0MD1 register can specify which pin, RXD or TXD inputs the serial data. If "data input from TXD pin" is selected to be with 1 line communication, transmission / reception is switched by controlling TXD pin's direction by the P0DIR0 flag of the P0DIR register. At that time, the RXD pin can be used as a general port.

■Reception Buffer Empty Flag

When SC0RIRQ is generated, data is stored to RXBUF0 from the internal shift register, automatically. If data is stored to the shift register RXBUF0, the reception buffer empty flag SC0REMP of the SC0MD3 register is set to "1". That indicates that the received data is going to be read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■Reception BUSY flag

When the start condition is reagrded, the SC0RBSY flag of the SC0MD3 register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SC0RIRQ. If the SC0SBIS flag is set to "0" during receptin, the SC0RBSY flag is reset to "0".

■Transmission BUSY flag

When any data is set to TXBUF0, the SC0TBSY flag of the SC0MD3 register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SC0TIRQ. During continuous communication the SC0TBSY flag is always set. If the transmission buffer empty flag S0TEMP is set to "0" as the transmission complete interrupt SC0TIRQ is generated, the SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0", the SC0TBSY flag is reset to "0".

■Frame Mode and Parity Check Setup

Figure 11-3-15 shows the data format at UART communication.

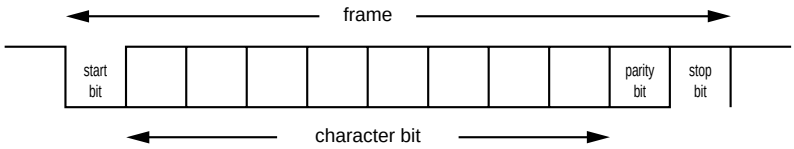


Figure 11-3-15 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit.
Table 11-3-13 shows its kinds to be set.

Table 11-3-13 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7, 8 bits
Parity bit	fixed to 0, fixed to 1, even, odd, none
Stop bit	1, 2 bits

The SC0FM1 to 0 flag of the SC0MD2 register sets the frame mode. Table 11-3-14 shows the UART serial interface frame mode settings. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the transfer bit count on the SC0LNG2 to 0 flag of the SC0MD0 register is no more valid.

Table 11-3-14 UART Serial Interface Frame Mode

SC0MD2 register		Frame mode
SC0FM1	SC0FM0	
0	0	Character bit 7 bits + Stop bit 1 bit *
0	1	Character bit 7 bits + Stop bit 2 bits *
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data.
Table 11-3-15 shows kinds of parity bit. The SC0NPE, SC0PM1 to 0 flag of the SC0MD2 register set parity bit.

Table 11-3-15 Parity bit of UART Serial Interface

SC0MD2 register			Parity bit	Setup
SC0NPE	SC0PM1	SC0PM0		
0	0	0	fixed to 0	Set parity bit to "0".
0	0	1	fixed to 1	Set parity bit to "1".
0	1	0	odd parity	Control that the total of "1" of parity bit and character bit should be odd.
0	1	1	even parity	Control that the total of "1" of parity bit and character bit should be even.
1	-	-	none	Do not add parity bit.

Do not set following flame modes when SC0NPE flag is "1" and parity bit is disabled,
Character 7 bits + Stop 2 bits of the flame mode
(Set the SC0FM1, SC0FM0 flags to "0, 1".)
Character 7 bits + Stop 1 bit of the flame mode
(Set the SC0FM1, SC0FM0 flags to "0, 0".)

■Brake Status Transmission Control Setup
The SC0BRKE flag of the SC0MD2 register generates the brake status. If SC0BRKE is set to "1" to select the brake transmission, all bits from start bits to stop bits transfer "0".

■Reception Error

At reception , there are 3 types of error ; overrun error, parity error and framing error. Reception error can be determined by the SC0ORE, SC0PEK, SC0FEF flag of the SC0MD3 register. Even one of those errors is detected, the SC0ERE flag of the SC0MD3 register is set to "1". The SC0PEK, the SC0FEF flags in recepption error flag are renewed at generation of the reception complete interrupt SC0RIRQ. The SC0ORE flag holds the status unless data of RXBUF0 is read out. The decision of the received error flag should be operated until the next communication is finished. Those error flag has no effect on communication operation. Table 11-3-16 shows the list of reception error source.

Table 11-3-16 Reception Error Source of UART Serial Interface

Flag	Error	Error source	
SC0ORE	Overrun error	Next data is received before reading the receive buffer.	
SC0PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	when parity bit is "0"
		odd parity	The total of "1" of parity bit and character bit is even.
		even parity	The total of "1" of parity bit and character bit is odd.
SC0FEF	Framing error	Stop bit is not detected.	

■Judgement of Brake Status Reception

Reception at brake status can be judged. If all received data from start bit and stop bit is "0", the SC0BRKF flag of the SC0MD2 register is set and regards the brake status. The SC0BRKF flag is set at generation of the reception complete interrupt SC0RIRQ.

■Continuous Communication

This serial interface has continuous communication function. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is set to continue automatic communication. This does not generate any blank in communication. Set data to TXBUF0 between previous data setup and generation of the communication complete interrupt SC0TIRQ.

■Changing Polarity of Transmission / Reception Data

The polarity of the transmission / reception data can not be swtched during UART communication, Therefore, setting SC0TRN and SC0REN flags of the SC0MD0 register has no effect during UART communication.

■Clock Setup

Transfer clock is not necessary for UART communication itself, but necessary for setup of data transmission / reception timing in the serial interface.

Select the timer to be used as a baud rate timer by the SC0CKS register, and set the SC0MST flag of the SC0MD1 register to "1" to select the internal clock (clock master).

At UART communication, set the SC0MST flag of the SC0MD1 register to "1". If "0" is set, the communication is disabled.

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

■Tranfer Bit Count and First Transfer Bit

When the transfer bit is 7 bits, the data storing method to the transmission data buffer TXBUF0 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0 for storing. When there are 7 bits to be transfered, as shown on figure 11-3-16, if data "A" to "G" are stored to bp1 to bp7 of TXBUF0, the transmission is operated from "G" to "A". At LSB first, use the lower bits of TXBUF0 for storing. When there are 7 bits to be transfered, as shown on figure 11-3-17, if data "A" to "G" are stored to bp0 to bp6 of TXBUF0, the transmission is operated from "A" to "G".

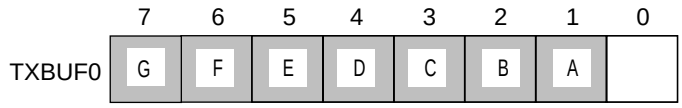


Figure 11-3-16 Transfer Bit Count and First Transfer Bit (starting with MSB)

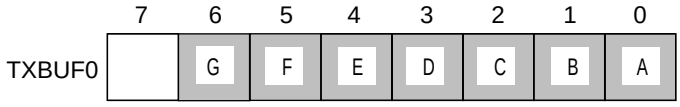


Figure 11-3-17 Transfer Bit Count and First Transfer Bit (starting with LSB)

■Receive Bit Count and First Transfer Bit

When the transfer bit count is 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit selection. At MSB first, data are stored to the upper bits of RXBUF0. When there are 7 bits to be transfered, as shown on figure 11-3-18, if data "G" to "A" are stored to bp7 to bp1 of RXBUF0. At LSB first, data are stored to the lower bits of RXBUF0. When there are 7 bits to be transfered, as shown on figure 11-3-19, if data "A" to "G" are stored to bp0 to bp6 of RXBUF0.

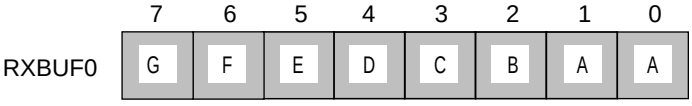


Figure 11-3-18 Receive Bit Count and Transfer First Bit (starting with MSB bit)

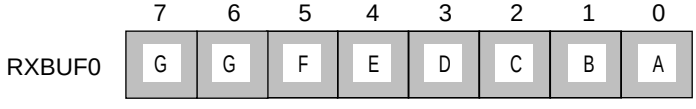


Figure 11-3-19 Receive Bit Count and Transfer First Bit (starting with LSB bit)

The following items are same as clock synchronous serial.
Reference as follows ;

■First Transfer bit Setup
Refer to : XI-13

■Transmission Data Buffer
Refer to : XI-13

■Received Data Buffer
Refer to : XI-13

■Transmission Buffer Empty Flag
Refer to : XI-17

■Emergency Reset
Refer to : XI-18

■Transmission Timing

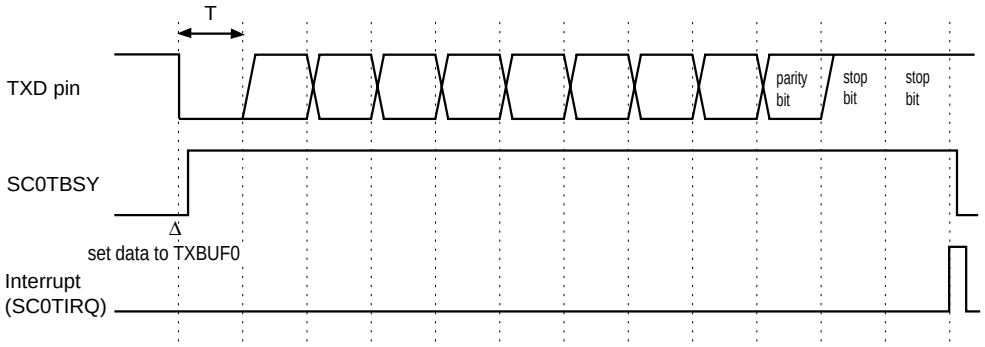


Figure 11-3-20 Transmission Timing (parity bit is enabled)

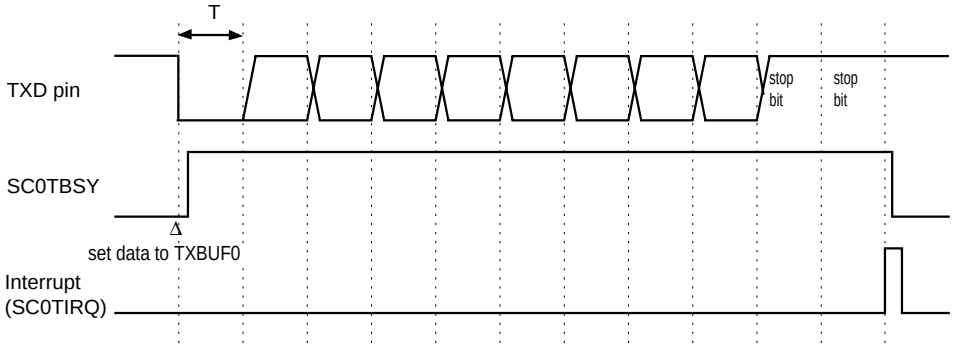


Figure 11-3-21 Transmission Timing (parity bit is disabled)

■Reception Timing

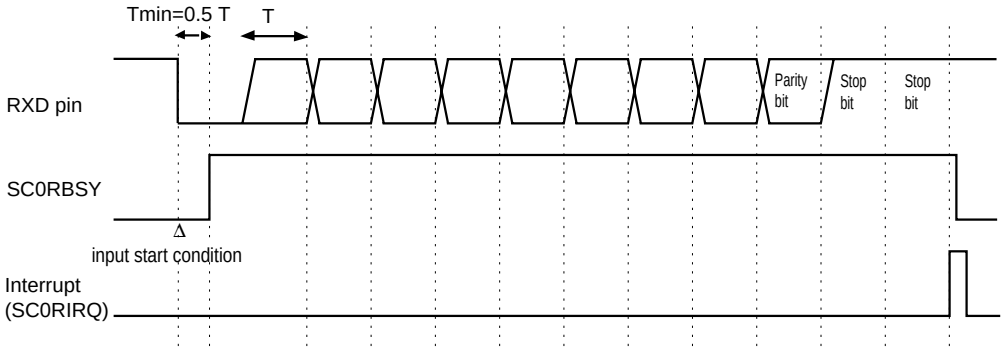


Figure 11-3-22 Reception Timing (parity bit is enabled)

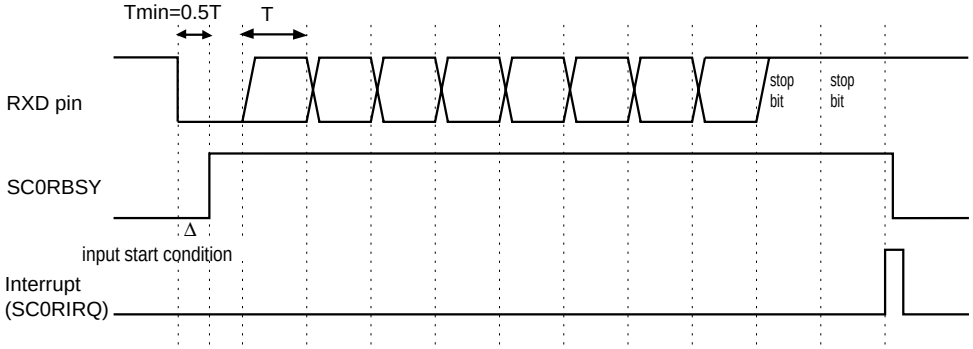


Figure 11-3-23 Reception Timing (parity bit is disabled)

■Transfer Speed Setup

Baud rate timer can set any transfer rate.

Table 11-3-17 shows the setup example of the transfer speed. Refer to chapter 6. 8-bit Timer for baud rate timer setup.

Table 11-3-17 UART Serial Interface Transfer Speed Setup Register

Setup	Register	Page
Serial 0 clock source (timer output)	SC0CKS	XI - 11
Timer clock source	TMnMD	VI - 10 to 13
Timer compare register	TMnOC	VI - 8

Timer compare register is set as follows ;

overflow cycle = (set value of compare register + 1) x timer clock cycle

baud rate = 1 / (overflow cycle x 2 x 8) ("8" means that clock source is divided by 8)

therefore,

set value of compare register = timer clock frequency / (baud rate x 2 x 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows ;

Set value of comapre register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= x'CF'

Timer clock source and the set value of timer comapre register at the standard rate are shown in the following page.

Transfer rate should be selected under 300 kbps.

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

Table 11-3-18-1 Setup Value of UART Serial Interface Transfer Speed (decimal)

fosc (MHz)	Clock source (timer)	Transfer rate (bps)									
		300		960		1200		2400		4800	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
16.76	fosc	-	-	-	-	-	-	-	-	-	-
20.00	fosc	-	-	-	-	-	-	-	-	-	-

Table 11-3-18-2 Setup Value of UART Serial Interface Transfer Speed (decimal)

fosc (MHz)	Clock source (timer)	Transfer rate (bps)									
		9600		19200		28800		31250		38400	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
16.76	fosc	108	9610	54	19045	-	-	-	-	-	-
20.00	fosc	129	9615	64	19231	-	-	39	31250	-	-

■Pin Setup (with 1, 2 channels, at transmission)

Table 11-3-19 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD pin, RXD pin, regardless of those pins are independednt / connected.

Table 11-3-19 UART Serial Interface Pin Setup (with 1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Port pin	P00	P01
TXD / RXD pins	TXD / RXD pins connected or independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	Output mode	-
	P0DIR(P0DIR0)	
Pull-up	Added / Not added	-
	P0PLU(P0PLU0)	

■Pin Setup (with 2 channels, at reception)

Table 11-3-20 shows the pins setup at UART serial interface reception with 2 channels (TXD pin, RXD pin).

Table 11-3-20 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Port pin	P00	P01
TXD / RXD pin	TXD / RXD pins connected or independent	
	SC0MD1(SC0IOM)	
Function	port	serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	input mode
	-	P0DIR(P0DIR1)
Pull-up	-	-

■Pin Setup (with 1 channel, at reception)

Table 11-3-21 shows the pin setup at UART serial interface reception with 1 channel (TXD pin). The RXD pin is not used, so can be used as a port.

Table 11-3-21 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Port pin	P00	P01
TXD / RXD pin	TXD / RXD pins connected	
	SC0MD1(SC0IOM)	
Function	Port	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	Input mode	-
	P0DIR(P0DIR0)	-
Pull-up	-	-

■Pin Setup (with 2 channels, at transmission / reception)

Table 11-3-22 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXD pin, RXD pin).

Table 11-3-22 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Port pin	P00	P01
TXD / RXD pins	TDX / RXD pins independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	Output mode	Input mode
	P0DIR(P0DIR0)	P0DIR(P0DIR1)
Pull-up	Added / Not added	-
	P0PLU(P0PLU0)	

11-3-4 Setup Example

■Transmission / Reception Setup

The setup example at UART transmission / reception with serial 0 is shown.

Table 11-3-23 shows the conditions at transmission / reception.

Table 11-3-23 UART Interface Transmision Reception Setup

Setup item	set to
TXD / RXD pin	independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	timer 3
TXD0 / RXD0 pin type	Nch open-drain
Pull-up resistor of TXD pin	added
Parity bit add / check	"0"add / check
Serial 0 transmission complete interrupt	Enable.
Serial 0 reception complete interrupt	Enable.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0= 111 bp3 : SC0TMSEL= 0	(2) Set the bp3-0 flag of the SC0CKS register to "0111" to select timer 3 output as a clock source.
(3) Control the pin type. SC0ODC (x'3F96') bp0 : SC0ODC0 = 1 P0PLU (x'3F40') bp0 : P0PLU0 = 1	(3) Set the SC0ODC0 flag of the SC0ODC register to "1" to select N-ch open drain for the TXD pin. Set the P0PLU0 flag of the P0PLU register to "1" to add pull-up resistor.
(4) Control the pin direction. P0DIR (x'3F30') bp1-0 : P0DIR1-0 = 01	(4) Set the P0DIR1-0 flag of the port 0 pin direction control register (P0DIR) to "01" to set P00 to output mode, and P01 to input mode.
(5) Set the SC0MD0 register. Select the start condition. SC0MD0 (x'3F90') bp3 : SC0STE = 1	(5) Set the SC0STE flag of the SC0MD0 register to "1" to enable start condition.

Setup Procedure	Description
(6) Select the first bit to be transfered. SC0MD0 (x'3F90') bp4 : SC0DIR = 0	(6) Set the SC0DIR flag of the SC0MD0 register to "0" to select MSB as first transfer bit.
(7) Set the SC0MD2 register. Control the output data. SC0MD2 (x'3F92') bp0 : SC0BRKE = 0	(7) Set the SC0BRKE flag of the SC0MD2 register to "0" to select serial data transmission.
(8) Select the added parity bit. SC0MD2 (x'3F92') bp3 : SC0NP = 0 bp5-4 : SC0PM1-0 = 00	(8) Set the SC0PM1-0 flag of the SC0MD2 register to "00" to select 0 parity, and set the SC0NPE flag to "0" to add parity bit.
(9) Specify the flame mode. SC0MD2 (x'3F92') bp7-6 : SC0FM1-0 = 11	(9) Set the SC0FM1-0 flag of the SC0MD2 register to "11" to select 8 bits + 2 stop bits at the flame mode.
(10) Set the SC0MD1 register. Select the communication type. SC0MD1 (x'3F91') bp0 : SC0CMD = 1	(10) Set the SC0CMD flag of the SC0MD1 register to "1" to select duplex UART.
(11) Select the clock frequency. SC0MD1 (x'3F91') bp3 : SC0CKM = 1 bp2 : SC0MST = 1	(11) Set the SC0CKM flag of the SC0MD1 register to "1" to select "divided by 8" at source clock. And, the SC0MST flag should be always set to "1" to select colck master.
(12) Control the pin function. SC0MD1 (x'3F91') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp7 : SC0IOM = 0	(12) Set the SC0SBOS, SC0SBIS flag of the SC0MD1 register to "1" to set the TXD pin to serial data output and the RXD pin to serial data input.
(13) Enable the interrupt. SC0RICR (x'3FF5') bp1 : SC0RIE = 1 SC0TICR (x'3FF6') bp1 : SC0TIE = 1	(13) Set the SC0RIE flag of the SC0RICR register to "1", and set the SC0TIE flag ot the SC0TICR register to "1" to enable the interrupt request. If any interrupt request flag is already set, clear them. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]

Setup Procedure	Description
(14) Set the baud rate timer.	(14) Set the baud rate timer by the TM3MD register, the TM3OC register. Set the TM3EN flag to "1" to start timer 3. [☞ Chapter 6. 8-bit Timer]
(15) Start serial communication. The transmission data → TXBUF0 (x'3F95') The received data → input to RXD	(15) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF0). When the transmission is finished, the serial 0 transmission interrupt (SC0TIRQ) is generated. After the serial data is input from the RXD pin and the start condition is recognized, the received data is stored. When the reception is finished, the received data is stored to the serial received data buffer RXBUF0 and the serial 0 reception data buffer interrupt SC0RICR is generated.

Note : (5) to (6), (7) to (9), (10) to (12) can be set at the same time.

When the TXD / RXD pin are connected for communication with 1 channel, the TXD pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIOS of the SC0MD1 register to "1" to select serial data input. The RXD pin can be used as a general port.

This serial interface contains emergency reset function. If communication need to be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as the setup procedure in order. Activation of communication should be operated after all control registers (except Table 11-2-1 : TXBUF0, RXBUF0) are set.

Only timer 3 can be used as a baud rate timer.
Refer to Chapter 6. 8-bit Timer for baud rate setup.

When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.

In full-duplex UART communication using serial interface 0, abnormal reception may occur if data transmission is started during data reception (transmission data is set to transmission data buffer). Therefore, run the following program under the condition that data reception may occur.
However, do not use full-duplex UART communication for sequence communication, as the software countermeasure cannot be used.

[Basic flow of countermeasure program]

(1) Confirm reception status by SC0RBSY flag of SC0STR register before transmission data is set.
(2) At SC0RBSY = 0(other use), set transmission data to TXBUF0.
(3) At SC0RBSY = 1(serial reception in progress), wait untill SC0RBSY = 0(other use).

[Examples of recommended program]

```
Label 1 tbnz  (x'03F93') 6, Label 2     :(1) Branches to Label2 at SC0RBSY = 1
              mov '55', (x'03F95')      :(2) Set transfer data (x'55') to TXBUF0
              jmp Label 3               :    Branches to Label3
Label 2 tbz   (x'03F93') 6, Label 1     :(3) Branches to Label1 at SC0RBSY = 0
        loop  Label 2
Label 3
```

[*1] To prevent abnormal operation, UART transfer rate must be set as follows even when data reception is started "after reception status is confirmed" (1), "before transmission data is set" (2).
transfer rate = selected clock frequency/8 ≤ fs/10 (fs:system clock frequency)
Selectable transfer clock sources are shown in following table.

[*2] Operation (2) needs to be executed right after the operation (1) is completed. During these procedure, prevent branching by disable interrupts or other methods.

System clock(fs)	Selectable serial interface 0 transfer clock source
fs=fosc	All clock sources
fs=fosc/2	fosc/4,fosc/16,fosc/64,fs/2,fs/4, baud rate timer output fulfill (*1)
fs=fosc/4	fosc/16,fosc/64,fs/4, baud rate timer output fulfill (*1)
fs=fosc/8	fosc/16,fosc/64, baud rate timer output fulfill (*1)
fs=fosc/16	fosc/64, baud rate timer output fulfill (*1)
fs=fosc/32	fosc/64, baud rate timer output fulfill (*1)
fs=fosc/64	baud rate timer output fulfill (*1)

Chapter 12 A/D Converter

12

12-1 Overview

This LSI has an A/D converter with 10 bits resolution. It contains a built-in sample hold circuit. The channels 0 to 3 (AN0 to AN3) of analog input can be switced by software. When A/D converter is stopped, the power consumption can be reduced by turning the built-in ladder resistance OFF. A/D conversion is activated by a register setup.

12-1-1 Functions

Table 12-1-1 shows the A/D converter functions.

Table 13-1-1 A/D Converter Functions

A/D Input Pins	4 pins
Pins	AN3 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion Time (Min.)	9.6 µs(TAD = as 800 ns)
Input range	V_{ref-} to V_{ref+}
Power Consumption	Built-in Ladder Resistance (ON/OFF)

12-1-2 Block Diagram

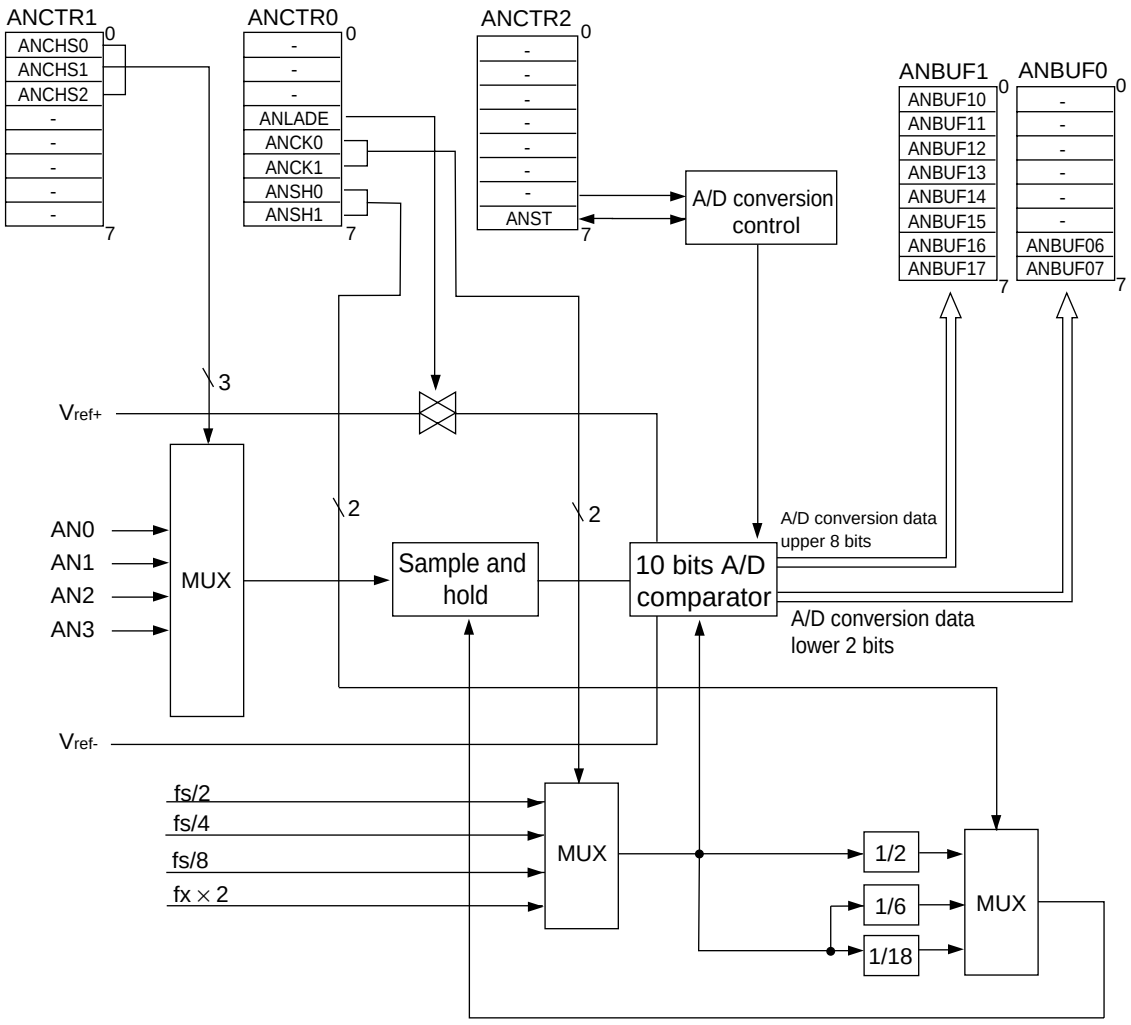


Figure 12-1-1 A/D Converter Block Diagram

12-2 Control Registers

A/D converter consists of the control register (ANCTRn) and the data storage buffer (ANBUFn).

12-2-1 Registers

Table 12-2-1 shows the registers used to control A/D converter.

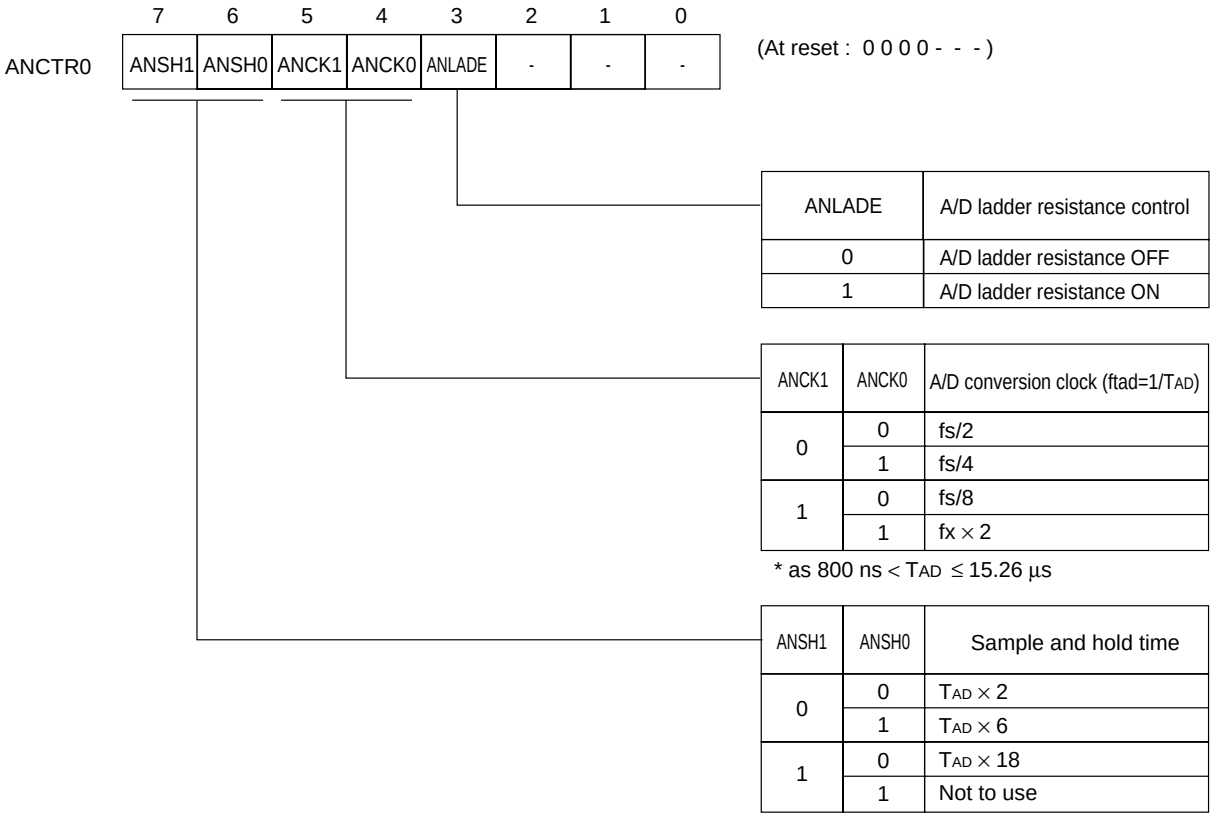
Table 12-2-1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	x'03FB0'	R/W	A/D converter control register 0	XII - 5
ANCTR1	x'03FB1'	R/W	A/D converter control register 1	XII - 6
ANCTR2	x'03FB2'	R/W	A/D converter control register 2	XII - 6
ANBUF0	x'03FB3'	R	A/D converter data storage buffer 0	XII - 7
ANBUF1	x'03FB4'	R	A/D converter data storage buffer 1	XII - 7
ADICR	x'03FFA'	R/W	A/D converter interrupt control register	III - 32
PAIMD	x'03F3A'	R/W	Port A input mode register	IV - 40
PAPLUD	x'03F4A'	R/W	Port A pull-up/pull-down resistance control register	IV - 40

R/W : Readable/Writable
R : Readable only

12-2-2 Control Registers

■A/D Converter Control Register 0 (ANCTR0)



ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF
1	A/D ladder resistance ON

ANCK1	ANCK0	A/D conversion clock (ftad=1/T_{AD})
0	0	fs/2
	1	fs/4
1	0	fs/8
	1	fx × 2

* as 800 ns < T_{AD} ≤ 15.26 µs

ANSH1	ANSH0	Sample and hold time
0	0	T_{AD} × 2
	1	T_{AD} × 6
1	0	T_{AD} × 18
	1	Not to use

Figure 12-2-1 A/D Control Register 0 (ANCTR0 : x'03FB0', R/W)

■A/D Converter Control Register 1 (ANCTR1)

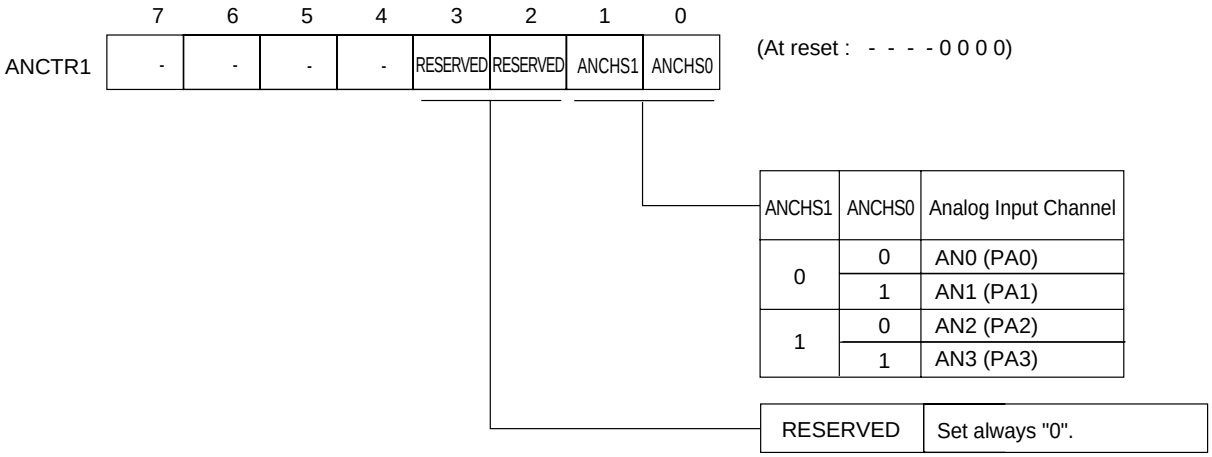

7 6 5 4 3 2 1 0
ANCTR1
- - - - RESERVED RESERVED ANCHS1 ANCHS0
(At reset : - - - - 0 0 0 0)
ANCHS1 ANCHS0 Analog Input Channel
0 0 AN0 (PA0)
1 AN1 (PA1)
1 0 AN2 (PA2)
1 AN3 (PA3)
RESERVED Set always "0".

Figure 12-2-2 A/D Converter Control Register 1 (ANCTR1 : x'03FB1', R/W)

■A/D Converter Control Register 2 (ANCTR2)

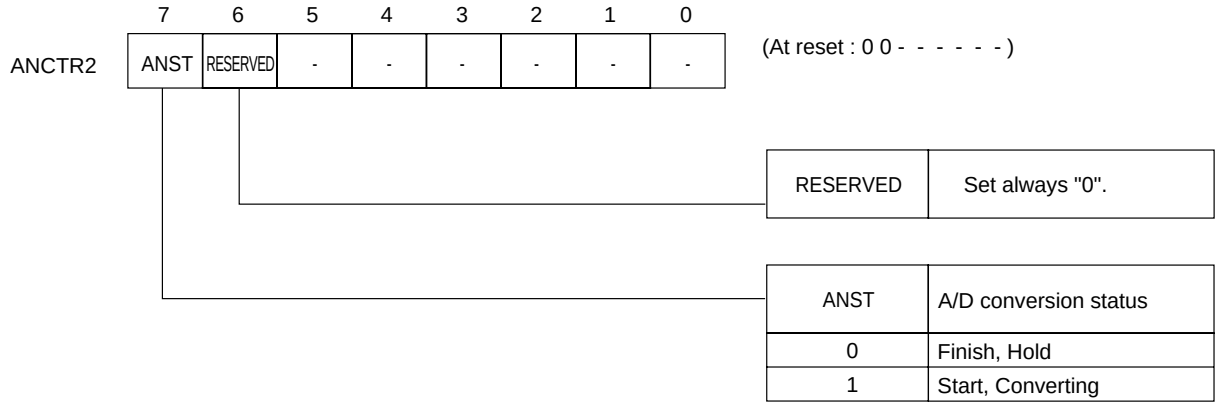

7 6 5 4 3 2 1 0
ANCTR2
ANST RESERVED - - - - - -
(At reset : 0 0 - - - - - -)
RESERVED Set always "0".
ANST A/D conversion status
0 Finish, Hold
1 Start, Converting

Figure 12-2-3 A/D Converter Control Register 2 (ANCTR2 : x'03FB2', R/W)

12-2-3 Data Buffers

■A/D Conversion Data Storage Buffer 0 (ANBUF0)

The lower 2 bits results from A/D conversion are stored to this register.

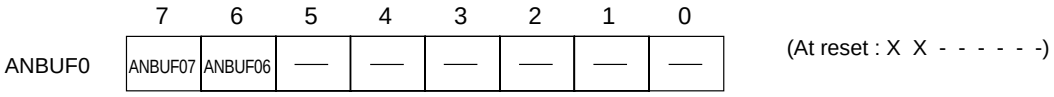


Figure 12-2-4 A/D Conversion Data Buffer 0 (ANBUF0 : x'03FB3', R)

■A/D Conversion Data Storage Buffer 1 (ANBUF1)

The upper 8 bits results from A/D conversion are stored to this register.

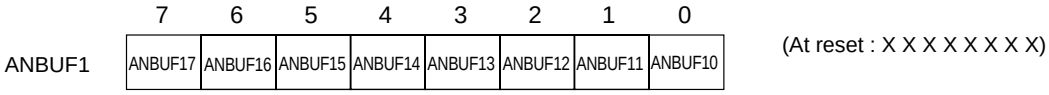


Figure 12-2-5 A/D Conversion Data Buffer 1 (ANBUF1 : x'03FB4', R)

12-3 Operation

Here is a description of A/D converter circuit setup procedure.

(1) Set the analog pins.
Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD).
* Setup of the port A input mode register should be done before analog voltage is put to pins.

(2) Select the analog input pin.
Select the analog input pin from AN3 to AN0 (PA3 to PA0) by the ANCHS1 to ANCHS0 flag of the A/D converter control register 1 (ANCTR1).

(3) Select the A/D converter clock.
Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
Setup should be such a way that converter clock (TAD) does not drop less than 800 ns with any oscillator.

(4) Set the sample hold time.
Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

(5) Set the A/D ladder resistance.
Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.
* (2) to (5) are not in order. (3), (4) and (5) can be operated simultaneously.

(6) Select the A/D converter activation factor, then start A/D conversion.
Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D converter.

(7) A/D conversion
After sampling with the sample and hold time, set in (3), A/D conversion is decided in comparison with MSB, in order.

(8) Complete the A/D conversion.
When A/D conversion is finished, the ANST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ANBUF0, 1). At the same time, the A/D complete interrupt request (ADIRQ) is generated.

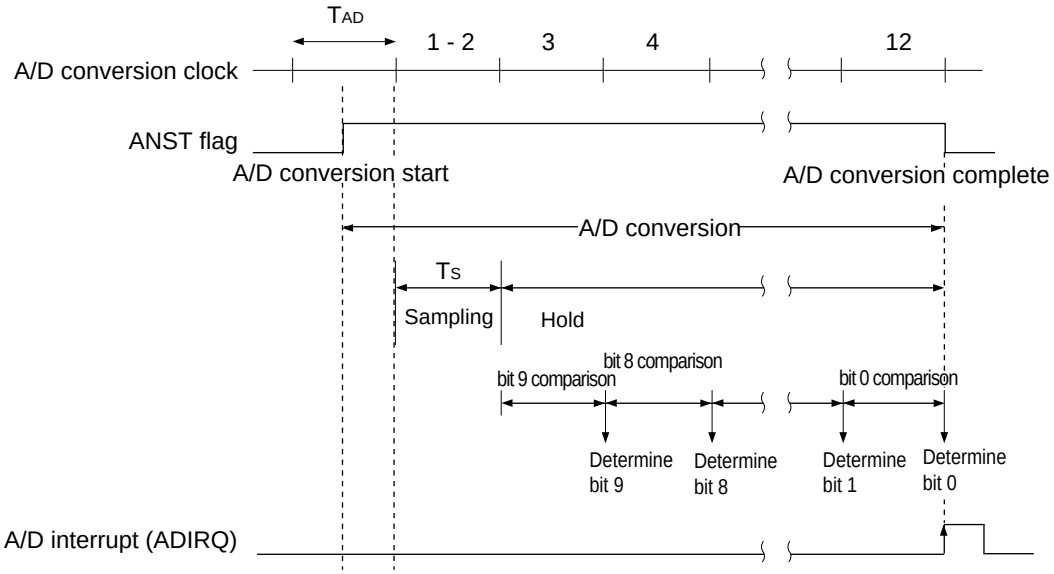


Figure 12-3-1 Operation of A/D Conversion

To read out the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

There is no problem for reference voltage V_{ref+} to be below V_{DD}. However, there should be difference more than 2 V between V_{ref+} and V_{ref-}.

12-3-1 Setup

■Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ANCH3 to 0 flag of the ANCTR1 register.

Table 12-3-1 Input Pins of A/D Converter Setup

ANCHS1	ANCHS0	A/D pin
0	0	AN0 pin
	1	AN1 pin
1	0	AN2 pin
	1	AN3 pin

■A/D Converter Clock Setup

The A/D converter clock is set with the ANCK1 to 0 flag of the ANCTR0 register. Set the A/D converter clock (T_{AD}) more than 800 ns and less than 15.26 µs. Table 12-3-2 shows the machine clock (fosc, fx, fs) and the A/D converter clock (T_{AD}). (calculated as fs = fosc/2, fx/2)

Table 12-3-2 A/D Conversion Clock and A/D Conversion Cycle

ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (T_{AD})		
			at oscillation for high speed		at oscillation for low speed
			at fosc=20 MHz	at fosc=8.38 MHz	at fx=32.768 kHz
0	0	fs/2	200.00 ns (unusable)	477.33 ns (unusable)	122.07 µs (unusable)
	1	fs/4	400.00ns (unusable)	954.65 ns	244.14 µs (unusable)
1	0	fs/8	800.00 ns	1.91 µs	488.28 µs (unusable)
	1	fx/2	15.26 µs	15.26 µs	15.26 µs

For the system clock (fs), refer to Chapter 2. 2-5 Clock Switching.

■A/D Converter Sampling Time (Ts) Setup

The sampling time of A/D converter is set with the ANSH1 to 0 flag of the ANCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table 12-3-3 Sampling Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sampling time (Ts)	A/D conversion time			
			at T_{AD}=800 ns	at T_{AD}=954.65 ns	at T_{AD}=1.91 µs	at T_{AD}=15.26 µs
0	0	T_{AD} x 2	9.60 µs	11.46 µs	22.92 µs	183.12 µs
	1	T_{AD} x 6	12.80 µs	15.27 µs	30.56 µs	244.16 µs
1	0	T_{AD} x 18	22.40 µs	26.73 µs	53.48 µs	427.28 µs
	1	Reserved	-	-	-	-

■Built-in Ladder Resistor Control

The ANLADE flag of the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. When A/D converter is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

Table 12-3-4 A/D Ladder Resistor Control

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF (A/D conversion stopped)
1	A/D ladder resistance ON (A/D conversion operated)

■A/D Conversion Starting Setup

A/D conversion starting is set with the ANST flag of the ANCTR2 register. The ANST flag of the ANCTR2 register is set to "1" to start A/D conversion. Also, the ANST flag of the ANCTR2 register is set to "1" during A/D conversion, then cleared to "0" as the A/D conversion complete interrupt is generated.

Table 12-3-5 A/D Conversion Starting

ANST	A/D conversion activation factor
1	A/D conversion started or in progress.
0	A/D conversion completed or stopped

12-3-2 Setup Example

■Example of A/D Converter Setup by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to TAD x 6. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD (x'3F3A') bp0 : PAIMD0 = 1 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0	(1) Set the analog input pin, set in (2), as the special function pin with the port A input mode register (PAIMD). Also, set no pull-up/pull-down resistance with the port A pull-up/pull-down resistance control register (PAPLUD).
(2) Select the analog input pin. ANCTR1 (x'3FB1') bp2-0 : ANCHS2-0 = 000	(2) Select the analog input pin from AN2-0 (PA3-0) by the ANCHS3-0 flag of the A/D converter control register 1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0 (x'3FB0') bp5-4 : ANCK1-0 = 01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
(4) Set the sample and hold time. ANCTR0 (x'3FB0') bp7-6 : ANSH1-0 = 01	(4) Set the sample and hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0).
(5) Set the interrupt level. ADICR (x'3FFA') bp7-6 : ADLV1-0 = 00	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it. [☞ Chapter 3. 3-1-4 Interrupt Flag Setting]
(6) Enable the interrupt. ADICR (x'3FFA') bp1 : ADIE = 1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".
(7) Set the A/D ladder resistance. ANCTR0 (x'3FB0') bp3 : ANLADE = 1	(7) Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.

Setup Procedure	Description
(8) Start the A/D conversion operation. ANCTR2 (x'3FB2') bp7 : ANST = 1	(8) Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start the A/D conversion.
(9) Complete the A/D conversion. ANBUF0 (x'3FB3') ANBUF1 (x'3FB4')	(9) When the A/D conversion is finished, the A/D conversion complete interrupt is generated and the ANST flag of the A/D converter control register 2 (ANCTR2) is cleared to "0". The result of the conversion is stored to the A/D converter buffer (ANBUF0, 1).

Note : The above (3) to (4) can be set at the same time.

12-3-3 Cautions

A/D conversion can be damaged by noise easily, therefore, anti-noise measures should be taken adequately .

■Anti-noise measures

To A/D input (analog input pin), add condenser near the V_{SS} pins of micro controller.

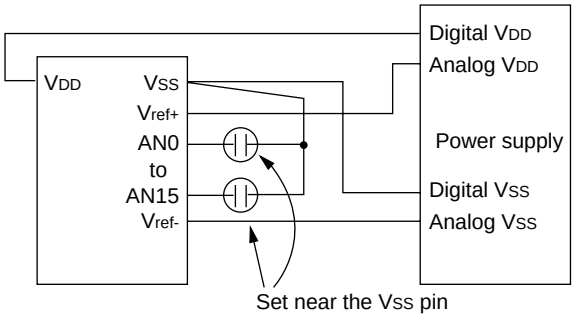


Figure 12-3-2 A/D Converter Recommended Example 1

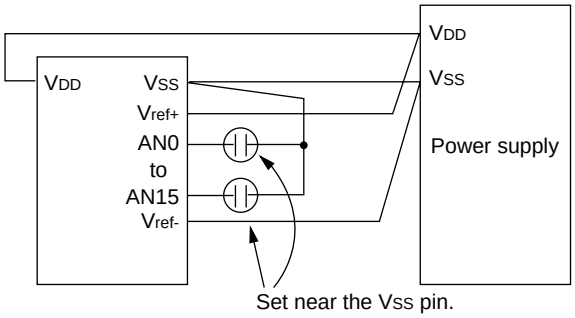
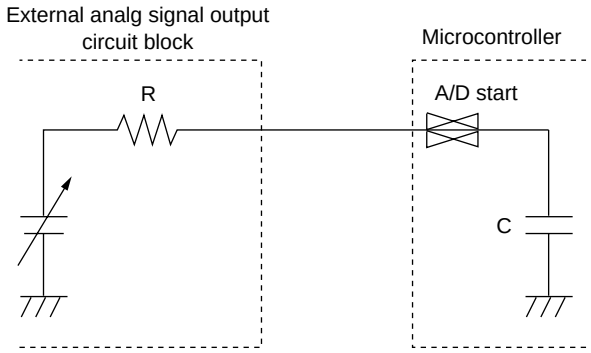


Figure 12-3-3 A/D Converter Recommended Example 2

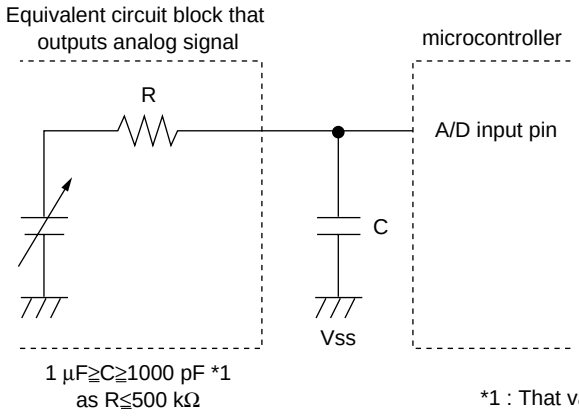
This microcontroller contains a sample hold capacitor (C) (app. 10 pF).
Set the sample hold time based on the capacitor (C) and the time constant of impedance R of the external analg signal output circuit.
For the sample hold time, 3 x the time constant CR or longer is recomended.
At A/D conversion cycle(T_{AD})=800 ns, 1.6 µs, 4.8 µs,and 14.4 µs can be selected as a sample hold time. Each impedance value of the external analog signal output circuit should be under the following values.

Sample hold time (At T_{AD}=800 ns)	Impedance of analog signal output circuit
T_{AD} x 2 = 1.6 µs	R < 1.6 µs / 10 pF / 3 = 53 kΩ
T_{AD} x 6 = 4.8 µs	R < 4.8 µs / 10 pF / 3 = 160 kΩ
T_{AD} x 18 = 14.4 µs	R < 14.4 µs / 10 pF / 3 = 480 kΩ



To maintain high precision of A/D conversion, following instructions on use of A/D converter should be strictly kept.

1. Input impedance R of A/D input pin should be under 500 kΩ*1. And connect the external capacitor C (over 1000 pF, under 1 µF)*1 between Vss and the A/D input pin.
2. Set the A/D conversion frequency depending on the time constant of R and C.
3. Changing the output level of the microcontroller or switching ON/OFF of the peripheral added circuit while the A/D conversion is in progress may lower the precision of A/D conversion, for these may fluctuate the values of the analog input pin and the power pin. Check the waveform of the analog input pin before the system evaluation.



*1 : That value is for reference.

Recommended Connection with A/D Converter

Chapter 13 LCD

13

13-1 Functions

This LSI contains an internal LCD driver circuit with 24 segment pins and 4 common pins. The LCD driver consists of a segment output latch, LCD control registers, a prescaler, a timing control circuit, a multiplexer, segment drivers, common drivers, a LCD voltage control circuit, voltage booster circuit and voltage divider resistors.

13-1-1 Functions

Table 13-1-1 shows the functions of the LCD driver circuits.

Table 13-1-1 LCD Functions

	LCD
Duty	Static 1/2 Duty 1/3 Duty 1/4 Duty
Segment Output Pins	SEG0 to SEG23
Common Output Pins	COM0 to COM3
LCD Power Supply	V_{LC1}, V_{LC2}, V_{LC3}
Booster Circuit to drive LCD	Selectable from either 2, 3 or 3/2,1/2 times of reference voltage input.
LCD Voltage Divider Resistor	V_{LC1} input voltage can be divided into 2/3, 1/3. Selectable from High resistance or low resistance.
Clock Source (LCDCLK)	$fosc/2^{11}$ $fosc/2^{12}$ $fosc/2^{13}$ $fosc/2^{14}$ $fosc/2^{15}$ $fosc/2^{16}$ $fosc/2^{17}$ $fosc/2^{18}$ $fx/2^{6}$ $fx/2^{7}$ $fx/2^{8}$ $fx/2^{9}$
fosc: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) LCDCLK: LCD clock source (selected with LCDCK0 to LCDCK3)	

When LCD function is unused, V_{LC1}, V_{LC2}, V_{LC3}, C1 and C2 pins should be fixed to V_{DD} level.

Use the LCD panel driver voltage V_{LCD} as $V_{DD} \leq V_{LCD} \leq 5.5$ V.

13-1-2 LCD Operation in Standby Mode

Certain LCD driver operation could be limited in standby mode.
Table 13-1-2 shows the LCD operation capabilities in standby mode.

Table 13-1-2 LCD Operation in Standby Mode

CPU Mode		LCD Clock	
		fosc	fx
Operation Mode	NORMAL	O	O
	SLOW	×	O
Standby Mode	HALT0	Δ	Δ
	HALT1	×	Δ
	STOP	×	×

O : LCD Operation is available
Δ : Holding Display is available
× : LCD Operation is not available.

OFF the LCD and switch from segment output to port before transition to the CPU mode in which LCD operation is disabled, .

13-1-3 Maximum Pixels

Table 13-1-3 shows the maximum pixels.

Table 13-1-3 Maximum Pixels

Duty	Maximum Pixels (Segment × Common)	8-segment LCD Panel	Common Pins	Segment Output Latch bits
Static	24(24 × 1)	3 figures	COM0	bit0, bit4
1/2	48(24 × 2)	6 figures	COM0 to COM1	bit0 to bit1, bit4 to bit5
1/3	72(24 × 3)	9 figures	COM0 to COM2	bit0 to bit2, bit4 to bit6
1/4	96(24 × 4)	12 figures	COM0 to COM3	bit0 to bit3, bit4 to bit7

13-1-4 Switching I/O ports and LCD segment pins

Switching of port output and segment output is controlled with the LCD output control register 1,2 (LCCTR1, LCCTR2). [☞ Chapter 13-2 LCD Control Registers]
Switching of normal port and common pin is controlled with the LCD mode control register 2 (LCCTR2). [☞ Chapter 13-2 LCD Control Registers]

Port 7 (SEG8 to 15) are switchable to I/O ports in 2-bit unit.
Port 8 (SEG0 to 7) is switchable to I/O ports in 2-bit unit.
Port 6 (SEG16 to 23) is switchable to I/O ports in 1-bit unit.
Port 3 (COM0 to 3) is switchable to I/O ports in 1-bit unit.

13-1-5 LCD Driver Circuit Block Diagram

■LCD Driver Circuit Block Diagram

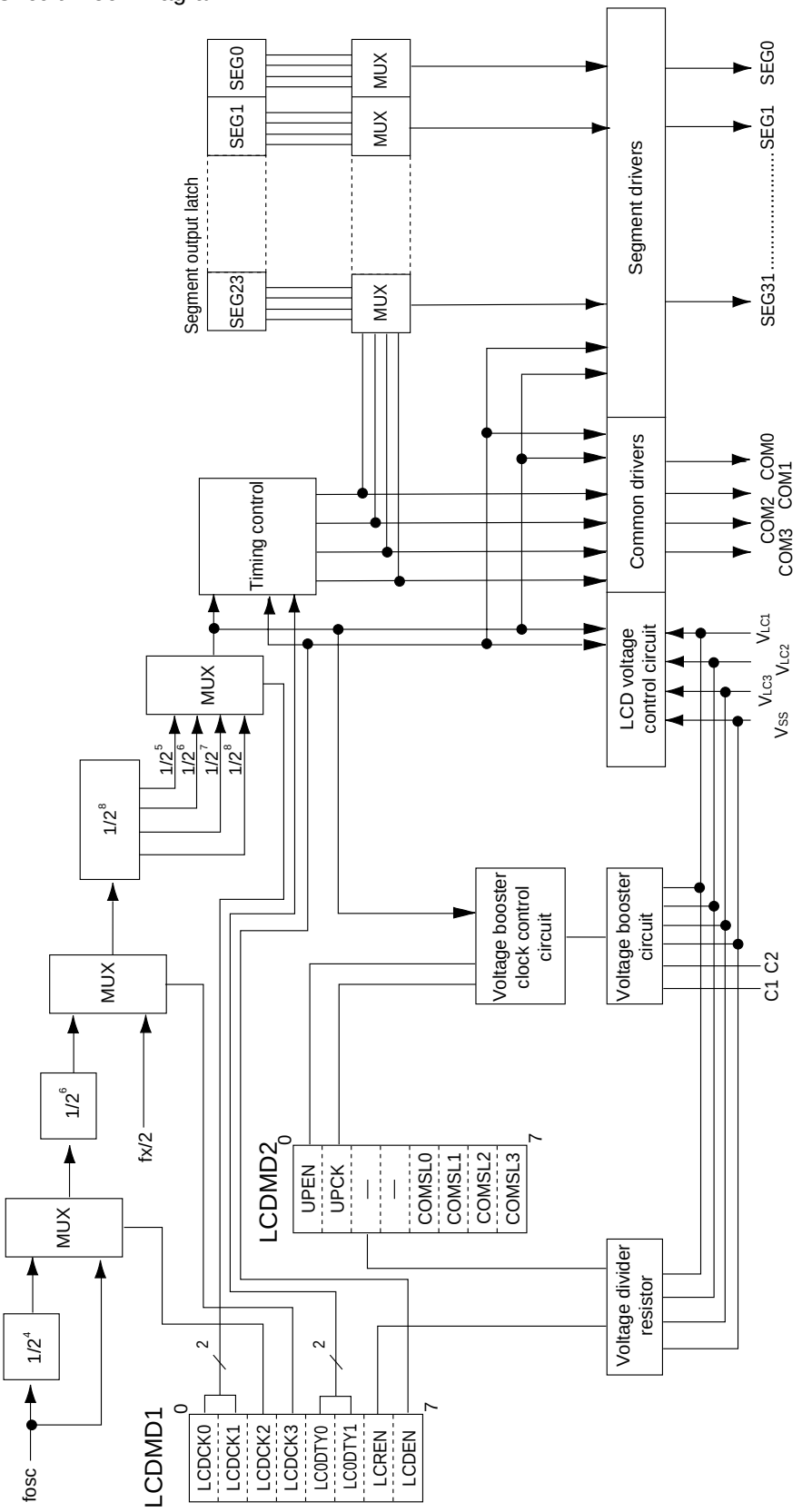


Figure 13-1-1 LCD Driver Circuit Block Diagram

13-2 Control Registers

The LCD is controlled by LCD mode control register 1 (LCDMD1), LCD mode control register 2 (LCDMD2), LCD output control register 1 (LCCTR1) and LCD output control register 2 (LCCTR2). The LCD display data is stored in the segment output latch.

13-2-1 Registers

Table 13-2-1 shows the LCD control registers.

Tabel 13-2-1 LCD Control Registers List

Register abbreviation	Address	R/W	Register Name	Page
LCDMD1	X'03FD9'	R/W	LCD mode control register 1	XIII - 6
LCDMD2	X'03FDA'	R/W	LCD mode control register 2	IV - 19, XIII - 7
LCCTR1	X'03FDB'	R/W	LCD output control register 1	IV - 33, 37 XIII - 8
LCCTR2	X'03FDC'	R/W	LCD output control register 2	IV- 28, XIII - 9

* Address x'02E00' to x'02E0B' are assigned to the segment output latch.
[☞ Chapter 13 13-2-6 Segment Output Latch]

13-2-2 Mode Control Register 1 (LCDMD1)

The LCD mode control register 1 (LCDMD1) is a 8-bit register that controls the LCD clock, LCD display ON/OFF, internal voltage divider resistors ON/OFF, and the display duty. The address assigned to this register is X'3FD9'. The value of the LCDMD1 register is initialized at reset.

	7	6	5	4	3	2	1	0	
LCDMD1	LCDEN	LCREN	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	(at reset: 00000000)

LCDCK3	LCDCK2	LCDCK1	LCDCK0	LCD clock source selection
0	0	0	0	OSC1/2^{11}
			1	OSC1/2^{12}
		1	0	OSC1/2^{13}
			1	OSC1/2^{14}
	1	0	0	OSC1/2^{15}
			1	OSC1/2^{16}
		1	0	OSC1/2^{17}
			1	OSC1/2^{18}
1	X	0	0	XI/2^{6}
			1	XI/2^{7}
		1	0	XI/2^{8}
			1	XI/2^{9}

LCDTY1	LCDTY0	LCD display duty selection
0	0	1/4 duty
	1	1/3 duty
1	0	1/2 duty
	1	Static

LCREN	Internal voltage divider resistor connection
0	No connection
1	Connection

LCDEN	LCD driver circuit start
0	Stop
1	Start

Figure 13-2-1 Mode Control Register1 (LCDMD1: X'3FD9', R/W)

13-2-3 Mode Control Register2 (LCDMD2)

The LCD mode control register 2 (LCDMD2) is a 6-bit register that controls switching of internal booster circuit operation ON/OFF and of Port I/O (P30 to P33) and common output. The address assigned to this register is x'3FDA'. The value of the LCDMD2 register is initialized at reset.

	7	6	5	4	3	2	1	0	
LCDMD2	COMSL3	COMSL2	COMSL1	COMSL0	—	—	UPCK	UPEN	(at reset: 00000000)

UPEN	Voltage booster enable / disable
0	Stop
1	Operate

UPCK	Voltage booster operation speed control
0	Normal speed
1	High speed

Set always '0'.

COMSL0	COM0 / Port 30 select
0	Port 30
1	COM0

COMSL1	COM1 / Port 31 select
0	Port 31
1	COM1

COMSL2	COM2 / Port 32 select
0	Port 32
1	COM2

COMSL3	COM3 / Port 33 select
0	Port 33
1	COM3

Figure 13-2-2 Mode Control Register 2 (LCDMD2: X'3FDA', R/W)

13-2-4 Output Control Register 1 (LCCTR1)

The LCD output control register 1 (LCCTR1) switches port output (P7,P8) and segment output (SEG0 to SEG15). The address assigned to this register is x'3FDB'. At reset, LCCTR1 is set to the input port values.

	7	6	5	4	3	2	1	0	
LCCTR1	LC1SL7	LC1SL6	LC1SL5	LC1SL4	LC1SL3	LC1SL2	LC1SL1	LC1SL0	(at reset: 00000000)

LC1SL0	SEG7 to 6 / Port 80 to 81 select
0	Port 80 to 81
1	SEG7 to 6

LC1SL1	SEG5 to 4 / Port 82 to 83 select
0	Port 82 to 83
1	SEG5 to 4

LC1SL2	SEG3 to 2 / Port 84 to 85 select
0	Port 84 to 85
1	SEG3 to 2

LC1SL3	SEG1 to 0 / Port 86 to 87 select
0	Port 86 to 87
1	SEG1 to 0

LC1SL4	SEG8 to 9 / Port 76 to 77 select
0	Port 76 to 77
1	SEG8 to 9

LC1SL5	SEG10 to 11 / Port 75 to 74 select
0	Port 75 to 74
1	SEG10 to 11

LC1SL6	SEG12 to 13 / Port 73 to 72 select
0	Port 73 to 72
1	SEG12 to 13

LC1SL7	SEG14 to 15 / Port 71 to 70 select
0	Port 71 to 70
1	SEG14 to 15

Figure 13-2-3 Output Control Register 1 (LCCTR1: X'3FDB', R/W)

13-2-5 Output Control Register 2 (LCCTR2)

The LCD output control register 2 (LCCTR2) switches port output (P6) and segment output (SEG16 to SEG23). The address assigned to this register is x'3FDC'. At reset, LCCTR2 is set to the input port values.

	7	6	5	4	3	2	1	0	
LCCTR2	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0	(at reset: 00000000)

LC2SL0	SEG16 / Port 67 select
0	Port 67
1	SEG16

LC2SL1	SEG17 / Port 66 select
0	Port 66
1	SEG17

LC2SL2	SEG18 / Port 65 select
0	Port 65
1	SEG18

LC2SL3	SEG19 / Port 64 select
0	Port 64
1	SEG19

LC2SL4	SEG20 / Port 63 select
0	Port 63
1	SEG20

LC2SL5	SEG 21 / Port 62 select
0	Port 62
1	SEG21

LC2SL6	SEG22 / Port 61 select
0	Port 61
1	SEG22

LC2SL7	SEG23 / Port 60 select
0	Port 60
1	SEG23

Figure 13-2-4 Output Control Register 2 (LCCTR2: X'3FDC', R/W)

13-2-6 Segment Output Latch

A 4-bit latch is allocated per segment. Bit0 and bit4 are read out at the timing of COM0, bit1 and bit5 are read out at that of COM1, bit2 and bit6 are read out at that of COM2, and bit3 and bit7 are read out at that of COM3. If a bit points “1”, the segment pin outputs the “selected voltage”, and if a bit points “0”, the segment pin outputs “non-selected voltage”.
The assigned address are X’2E00' to X’2E0B', and segment output latch value is indefined at reset. Figure 13-2-5 shows the matching of the segment output latch and the segment/common pins.

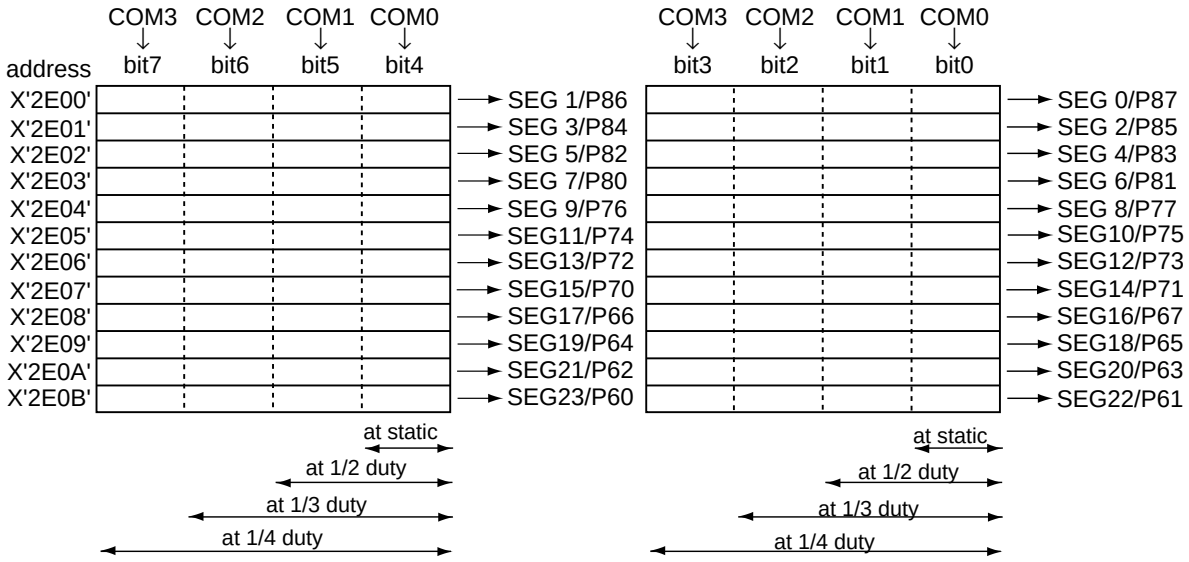


Figure 13-2-5 Matching of the Segment Output Latch and the Segment/Common Pins

13-3 Operation

13-3-1 Circuit Operation for LCD drive

The LCD driver is capable of static display and dynamic display (1/2 duty 1/2 bias, 1/3 duty 1/3bias, 1/4 duty 1/3 bias) through the segment output pins (SEG0 to SEG23) and the common output pins (COM0 to COM3).

■Circuit Operation for LCD drive

The LCD driver circuit generates the timing siginals, which are necessary for controling 1/2 duty, 1/3 duty, 1/4 duty and static, at the timing control circuit, based on the LCD clock divided by the prescaler, and supplies them to the common driver and the multiplexer.

The common driver outputs the common signals which are necessary for the LCD display, based on the voltage from the LCD power supply. When the LCD is OFF V_{SS} is output and the potential difference between the LCD electrodes becomes 0 V.

The multiplexer selects the segment output latched data in response to the signal from the timing control circuit and supplies it to the segment driver. The segment driver converts the content of the segment output latch into the signals, which is capable of driving the LCD, based on the voltage supplied to LCD power supply, then outputs the segment signal.

When the LCD is OFF V_{SS} is output and the potential difference between the LCD electrodes becomes 0 V.

At reset, common pins and segment pins become high impedance.
Therefore, when reset input from external sources is long, there could be some adverse effects such as blinks of the LCD display.

In STOP mode, supplies from the main clocks is stopped, and the LCD drive cannnot be operated. Set “0” to the enable flag of the LCD driver circuit before entering STOP mode.

13-3-2 Voltage Booster Circuit for LCD Drive

This LSI has internal booster circuit for LCD drive. This booster circuit contains reference voltage input pin (V_{LC2} or V_{LC3} pin), capacitor connection pins for boost operation (C1, C2), booster output pins (V_{LC2}, V_{LC3}). Either 2, 3, 3/2 or 1/2 times boost operation can be selected by changing deference voltage input pin (V_{LC3} or V_{LC2}).
Figure 13-3-1 shows a block diagram of LDC power section including booster circuit.

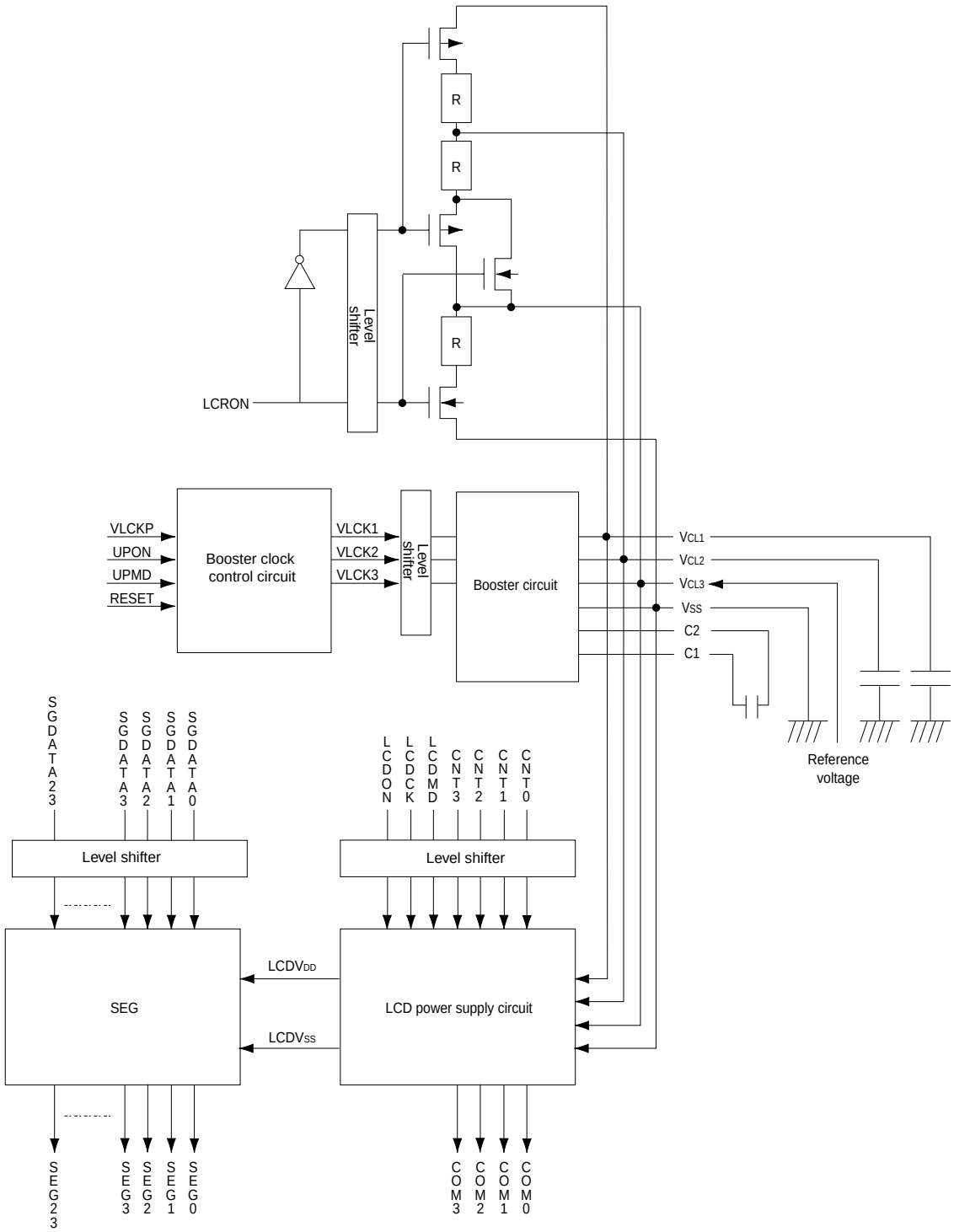


Figure 13-3-1 LCD Power Section Block Diagram (3 times boost)

■2 times, 3 times boosting

This is applied when LCD panel is used with 1/3 bias.

To operate 2 or 3 times voltage boost, input reference voltage to the V_{LC3} pin, and connect capacity to V_{LC1} and V_{LC2} pins to be connected to V_{SS}. Connect capacity between C1 and C2 pin, as well.

3 times of V_{LC3} reference voltage is applied to the V_{LC1} pin, and 2 times of V_{LC3} reference voltage is applied to V_{LC2} pin.

[☞ Chapter 13 13-3-3 Voltage supply when using internal voltage booster circuit]

■2/3 times, 1/2 times boosting

This is applied when LCD panel is used with 1/3 bias.

To operate 2/3 or 1/2 times voltage boost, input reference voltage to the V_{LC2} pin, and connect capacity V_{LC1} and V_{LC3} pins to be connected to V_{SS}. Connect capacity between C1 and C2 pin, as well.

2/3 times of V_{LC2} reference voltage is applied to the V_{LC1} pin, and 1/2 times of V_{LC2} reference voltage is applied to V_{LC3} pin.

[☞ Chapter 13 13-3-3 Voltage supply when using internal voltage booster circuit]

■2 times boosting

This is applied when LCD panel is used with 1/2 bias.

To operate 2 times voltage boost, input reference voltage to short-circuited V_{LC2} and V_{LC3} pins. Connect capacity between V_{LC1} and V_{SS} pins. Connect capacity between C1 and C2 pin, as well.

2 times of V_{LC2} (V_{LC3}) reference voltage is applied to V_{LC1} pin.

[☞ Chapter 13 13-3-3 Voltage supply when using internal voltage booster circuit]

When voltage booster circuit is active, internal voltage divider resistors cannot be used.

For 2 times, 3 times voltage boosting, input reference voltage V_{LC3} to voltage booster circuit in the range of $1/3\ V_{DD} \le V_{LC3} \le 1.8$ V.

For 3/2 times, 1/2 times voltage boosting, input reference voltage V_{LC2} to voltage booster circuit in the range of $2/3\ V_{DD} \le V_{LC2} \le 3.6$ V.

For 2 times voltage boosting, input reference voltage $V_{LC2}(= V_{LC3})$ to voltage booster circuit in the range of $1/2\ V_{DD} \le V_{LC2} \le 2.7$ V.

To generate LCD power supply (V_{LC1}) using LCD voltage booster circuit, start the LCD voltage booster circuit and supply voltage right after reset. For transition to STOP mode, disable (set 0 to) the start flag of the LCD driver circuit, and stop (set 0 to) the voltage booster start flag in advance. Power from microcontroller (V_{DD}) is supplied to the LCD power supply (V_{LC1}) by this procedure after voltage booster circuit is switched to STOP mode.

13-3-3 Power Supply

The LCD driver power pins are V_{LC1}, V_{LC2} and V_{LC3}. This LSI contains the internal voltage booster circuit as a dedicated power source for LCD drive and the voltage divider resistor to divide voltage for LCD drive. There are three ways to supply voltage to the LCD driver; to supply voltage to the V_{LC1}, V_{LC2} and V_{LC3} pins from external source (when external voltage divider resistor is used), to supply voltage to V_{LC1} pin from external source and use internal divider resistor, and to supply voltage to the V_{LC1} pin from external source and use the internal voltage divider resistor.
The power source for LCD drive and V_{DD} power supply for the microcontroller are separated so that the voltage V_{DD} for LCD panel drive can be used at higher voltage than the V_{DD} power supply (usable at $V_{DD} \leq V_{LCD} \leq 5.5$ V).
The LCD driver voltage supplied through the LCD driver power pins (V_{LC1}, V_{LC2} and V_{LC3}) is converted by the LCD clock signal and the timing control signal, and then supplied to the segment driver and the common driver.

Use the LCD panel driver voltage V_{LCD} at $V_{DD} \leq V_{LCD} \leq 5.5$ V.

If internal voltage divider resistor or voltage booster circuit is used, voltages of V_{LC1}, V_{LC2}, and V_{LC3} could be dropped depending on used LCD panel, and that may lower the brightness of LCD display. Use the external divider resistor when this is occured.

When LCD function is used without voltage booster circuit (when voltage is supplied to the V_{LC1}, V_{LC2} and V_{LC3} pins from external source and internal voltage devider resistor is used), fix C1 and C2 pins to following potential.

C1=V_{LC3} C2=V_{LC1}

■Supplying voltage with the external voltage divider resistor
Supply the voltage shown in table 13-3-1.

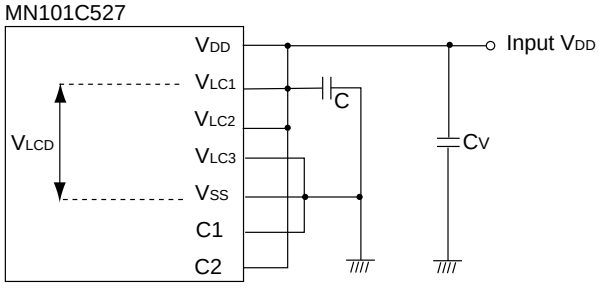
Table 13-3-1 LCD Power Supply

Bias / Method / LCD Power Supply	Static	1/2	1/3
V_{LC1}	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$
V_{LC2}		$1/2V_{LCD} + V_{SS}$	2/3 $V_{LCD} + V_{SS}$
V_{LC3}	V_{SS}		1/3 $V_{LCD} + V_{SS}$

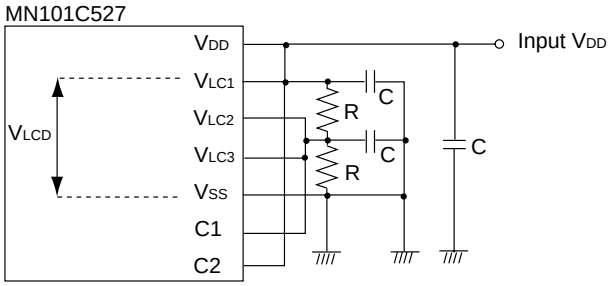
V_{LCD}: LCD panel driver voltage (Maximum voltage to the LCD panel)

Figure 13-3-2 shows examples of the LCD power supply connection.
Stabilization condenser C for LCD power supply is recommended to be C=0.1 µF.
$C_V \geq 0.1$ µF should be connected as Stabilization condenser C_V for V_{DD} power supply.

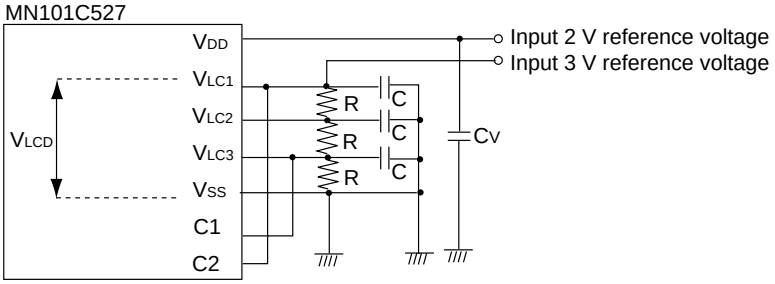
(a) Static ($V_{DD}=V_{LCD}$)



(b) 1/2 duty 1/2 bias ($V_{DD}=V_{LCD}$)



(c) 1/3 duty 1/3 bias, 1/4 duty 1/3 bias (V_{DD}=2 V, V_{LCD}=3 V)



(d) 1/3 duty 1/3 bias, 1/4 duty 1/3 bias ($V_{DD}=V_{LCD}$)

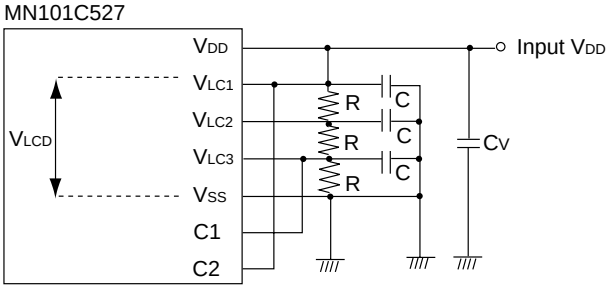


Figure 13-3-2 LCD power supply connection (when external divider resistor is used)

1. In figure 13-3-2, current always flows through the voltage divider resistors. The following connection is used to cut the current flowing through these dividing resistors. (at $V_{LC1}=V_{DD}$)

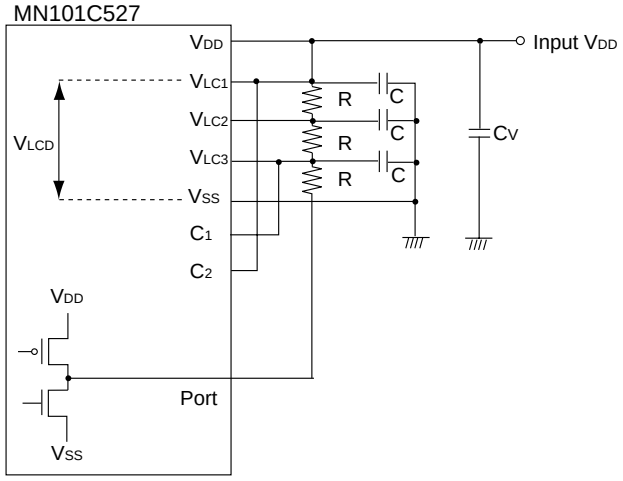


Figure 13-3-3 LCD Power Supply Connection

2. The LCD power supply V_{LC1} to 3 is supplied as shown in the following figure 13-3-4. V_{LCD} value varies depending on the type of LCD. Refer to the specifications of LCD for the appropreate value.

$V_{LC1} = V_{LCD} + V_{SS}$

$V_{LC2} = 2/3\ V_{DD} + V_{SS}$

$V_{LC3} = 1/3\ V_{LCD} + V_{SS}$

Usually V_{DD} - V_{SS} are divided by resistors and supplied to the LCD. Standard registance voltage ranges from tens to several hundreds kΩ. In figure 13-3-4, a bypass capacitor C (app. 0.1 μF) is used to lower the impedance of power supply.

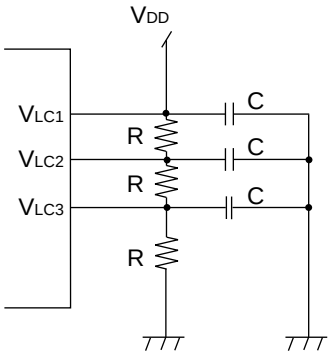


Figure 13-3-4 Supplying voltage to V_{LC1} to 3

■Supplying voltage when using the internal voltage divider circuit

Supply the voltage as shown in table 13-3-2.

Table 13-3-2 LCD Power Supply

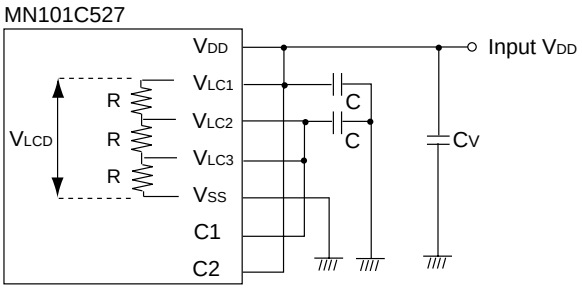
Bias Method / LCD Power Supply	Static	1/2	1/3
V_{LC1}	Not used	V_{LCD}	V_{LCD}
V_{LC2}		Connect V_{LC2} to V_{LC3} ($1/2\ V_{LCD}$ is output.)	$\overline{(2/3\ V_{LCD}\ \text{is output.})}$
V_{LC3}			$\overline{(1/3\ V_{LCD}\ \text{is output.})}$

Figure 13-3-5 shows examples of the LCD power supply connection.

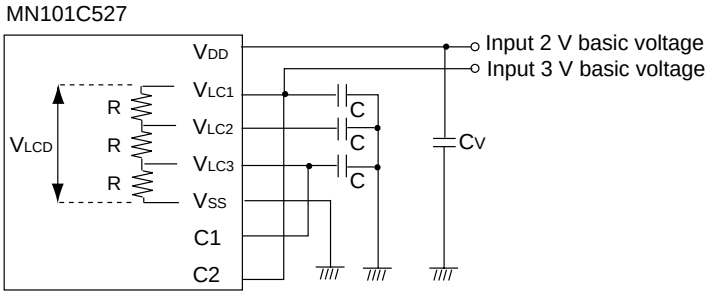
Stabilization condenser C for LCD power supply is recommended to be C=0.1 μF.

$C_V \geq 0.1$ μF should be connected as Stabilization condenser C_V for V_{DD} power supply.

(a) 1/2 duty 1/2 bias ($V_{DD}=V_{LCD}$)



(b) 1/3 duty 1/3 bias, 1/4 duty 1/3 bias (V_{DD}=2 V, V_{LCD}=3 V)



(c) 1/3 duty 1/3 bias, 1/4 duty 1/3 bias ($V_{DD}=V_{LCD}$)

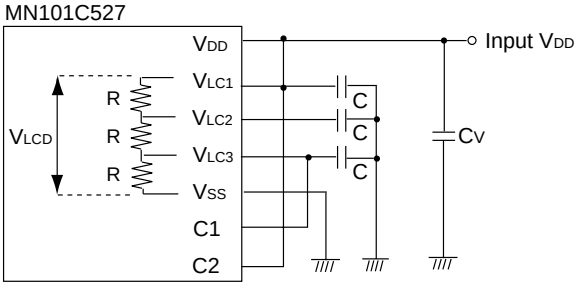


Figure 13-3-5

■Supplying voltage when using the internal voltage booster circuit

Supply the voltage as shown in table 13-3-3.

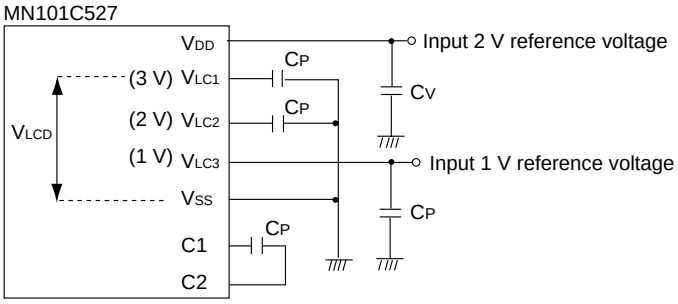
Table 13-3-3 LCD Power Supply

Voltage booster Action	2 times voltage booster	2 times voltage booster	2 times, 3 times voltage booster	3/2 times, 1/2 times voltage booster
LCD Power Supply \ Bias Method	Static	1/2	1/3	1/3
V_{LC1}	(2 V_{LC2} is output.)		(3 V_{LC3} is output.)	(3/2 V_{LC2} is output.)
V_{LC2}	Connect V_{LC2} and V_{LC3}, and intput 1/2 V_{LCD}		(2 V_{LC3} is output.)	Input 2/3 V_{LCD}
V_{LC3}			Input 1/3 V_{LCD}	(1/2 V_{LC2} is output.)

Figure 13-3-6 shows examples of the LCD power supply connection.

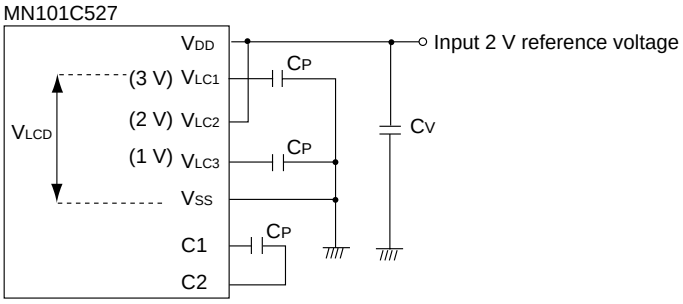
(a) 1/3 duty 1/3 bias , 1/4 duty 1/3 bias (V_{DD}=2 V, V_{LCD}=3 V)

(2 and 3 times voltage booster)



(b) 1/3 duty 1/3 bias , 1/4 duty 1/3 bias (V_{DD}=2 V, V_{LCD}=3 V)

(3/2 and 1/2 times voltage booster)



(c) Static, 1/2 duty 1/2 bias (V_{DD}=2.5 V, V_{LCD}=5 V)

(2 times voltage booster)

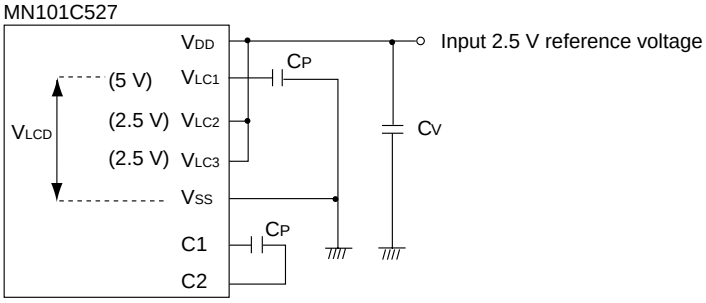


Figure 13-3-6

13-3-4 Frame Cycle

■Setup of the LCD frame cycle

The clock fosc or fx is divided by the prescaler and supplied as the LCD clock. Set the LCD clock with bit0 to 3 and set the LCD frame cycle with bit4 to 5 of the LCDMD1 register. Table 13-3-4 shows reference input frequencies and the matching of the LCD clock and the LCD frame cycle.

Table 13-3-4 Input Frequency and the LCD Clock

		Input frequency									
Input clock	Duty	20 MHz		16 MHz		8 MHz		4 MHz		32.768 kHz	
LCDCK3 to 0	LCDTY1 to 0	LCD clock	frame	LCD clock	frame	LCD clock	frame	LCD clock	flame	LCD clock	frame
0000 ($OSC1/2^{11}$)	00 (1/4 duty)	9766 Hz	2441 Hz	7813 Hz	1953 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz		
	01 (1/3 duty)		3255 Hz		2604 Hz		1302 Hz		651 Hz		
	10 (1/2 duty)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
	11 (static)		9766 Hz		7813 Hz		3906 Hz		1953 Hz		
0001 ($OSC1/2^{12}$)	00 (1/4 duty)	4883 Hz	1221 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz	977 Hz	244 Hz		
	01 (1/3 duty)		1628 Hz		1302 Hz		651 Hz		326 Hz		
	10 (1/2 duty)		2441 Hz		1953 Hz		977 Hz		488 Hz		
	11 (static)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
0010 ($OSC1/2^{13}$)	00 (1/4 duty)	2441Hz	610 Hz	1953 Hz	488 Hz	977 Hz	244 Hz	488 Hz	122 Hz		
	01 (1/3 duty)		814 Hz		651 Hz		326 Hz		163 Hz		
	10 (1/2 duty)		1221 Hz		977 Hz		488 Hz		244 Hz		
	11 (static)		2441 Hz		1953 Hz		977 Hz		488 Hz		
0011 ($OSC1/2^{14}$)	00 (1/4 duty)	1221 Hz	305 Hz	977 Hz	244 Hz	488 Hz	122 Hz	244 Hz	61 Hz		
	01 (1/3 duty)		407 Hz		326 Hz		163 Hz		81 Hz		
	10 (1/2 duty)		610 Hz		488 Hz		244 Hz		122 Hz		
	11 (static)		1221 Hz		977 Hz		488 Hz		244 Hz		
0100 ($OSC1/2^{15}$)	00 (1/4 duty)	610 Hz	153 Hz	488 Hz	122 Hz	244 Hz	61 Hz	122 Hz	31 Hz		
	01 (1/3 duty)		203 Hz		163Hz		81 Hz		41 Hz		
	10 (1/2 duty)		305 Hz		244 Hz		122 Hz		61 Hz		
	11 (static)		610 Hz		488 Hz		244 Hz		122 Hz		
0101 ($OSC1/2^{16}$)	00 (1/4 duty)	305 Hz	76 Hz	244 Hz	61 Hz	122 Hz	31 Hz	61 Hz	15 Hz		
	01 (1/3 duty)		102 Hz		81 Hz		41 Hz		20 Hz		
	10 (1/2 duty)		153 Hz		122 Hz		61 Hz		31 Hz		
	11 (static)		305 Hz		244 Hz		122 Hz		61 Hz		
0110 ($OSC1/2^{17}$)	00 (1/4 duty)	153 Hz	38 Hz	122 Hz	31 Hz	61 Hz	15 Hz	31 Hz	8 Hz		
	01 (1/3 duty)		51 Hz		41 Hz		20 Hz		10 Hz		
	10 (1/2 duty)		76 Hz		61 Hz		31 Hz		15 Hz		
	11 (static)		153 Hz		122 Hz		61 Hz		31 Hz		
0111 ($OSC1/2^{18}$)	00 (1/4 duty)	76 Hz	19 Hz	61 Hz	15 Hz	31 Hz	8 Hz	15 Hz	4 Hz		
	01 (1/3 duty)		25 Hz		20 Hz		10 Hz		5 Hz		
	10 (1/2 duty)		38 Hz		31 Hz		15 Hz		8 Hz		
	11 (static)		76 Hz		61 Hz		31 Hz		15 Hz		
1×00 ($XI/2^{6}$)	00 (1/4 duty)									512 Hz	128 Hz
	01 (1/3 duty)										171 Hz
	10 (1/2 duty)										256 Hz
	11 (static)										512 Hz
1×01 ($XI/2^{7}$)	00 (1/4 duty)									256 Hz	64 Hz
	01 (1/3 duty)										85 Hz
	10 (1/2 duty)										128 Hz
	11 (static)										256 Hz
1×10 ($XI/2^{8}$)	00 (1/4 duty)									128 Hz	32 Hz
	01 (1/3 duty)										43 Hz
	10 (1/2 duty)										64 Hz
	11 (static)										128 Hz
1×11 ($XI/2^{9}$)	00 (1/4 duty)									64 Hz	16 Hz
	01 (1/3 duty)										21 Hz
	10 (1/2 duty)										32 Hz
	11 (static)										64 Hz

13-3-5 Setup Example of the LCD Driver Circuit

■Setup example of the LCD driver circuit (using internal voltage booster circuit)
An example of setup procedure to display “23” in 1/4 duty, 1/3 bias with both segment signals (SEG0 to SEG3) and common signals (COM0 to COM3), using internal voltage booster circuit is shown below. Refer to XIII-18. fig.13-3-6 for the LCD power supply connection. Refer to 13-4. LCD display for connection of LCD panel.

Setup Procedure	Description
(1) Start the voltage booster circuit operation LCDMD2(X’3FDA’) bp0 : UPEN = 1 bp1 : UPCK = 0	(1) Set the UPEN flag of the LCD mode control register 2 (LCDMD2) to “1” to operate voltage booster circuit. Set the UPCK frag to “0” to set up the voltage booster speed to normal.
(2) Setup pins LCDMD2(X’3FDA’) bp7-4 : COMSL3-0 = 1111 LCCTR1(X’3FDB’) bp3-2 : LC1SL3-2 = 11	(2) Set COMSL3 to 0 flags of the LCD mode control register 2 (LCDMD2) to “1111”, to set up the common pins 3 to 0. Set the LC1SL3-2 flag of the LCD output control register (LCCTR1) to “11”, to set up the segment pins 3 to 0.
(3) Select the LCD clock source LCDMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0111	(3) Select OSC1/2^{18} as the LCD clock source by LCDCK3 to 0 flags of the LCD mode control register 1 (LCDMD1).
(4) Select the LCD display duty LCDMD1(X’3FD9’) bp5-4 :LCDTY1-0 = 00	(4) Set LCDTY1 to 0 flags of the LCD mode control register 1 (LCDMD1) to “00” to set up the display duty.
(5) Setup the LCD panel display data X’2E00’ = X’E5’ X’2E01’ = X’C7’	(5) Set up the display data on the address X’2E00’, X’2E01’ of the segment output latch. [☞ Refer to 13-4 Display]
(6) Start the LCD driver circuit LCDMD1(X’3FD9’) bp7 :LCDEN = 1	(6) Set the LCDEN flag of the LCD mode control register 1 (LCDMD1) to “1” to start the LCD driver circuit.

If internal voltage booster circuit is used, voltages of V_{LC1}, V_{LC2}, and V_{LC3} could be dropped depending on the load of used LCD panel, and that may lower the brightness of LCD display. In this case, set "1" to the voltage booster operation speed control bit of the LCD mode control register 2 (LCDMD2) to increase the operation speed. This also increases charge supply capacity of the voltage booster circuit.

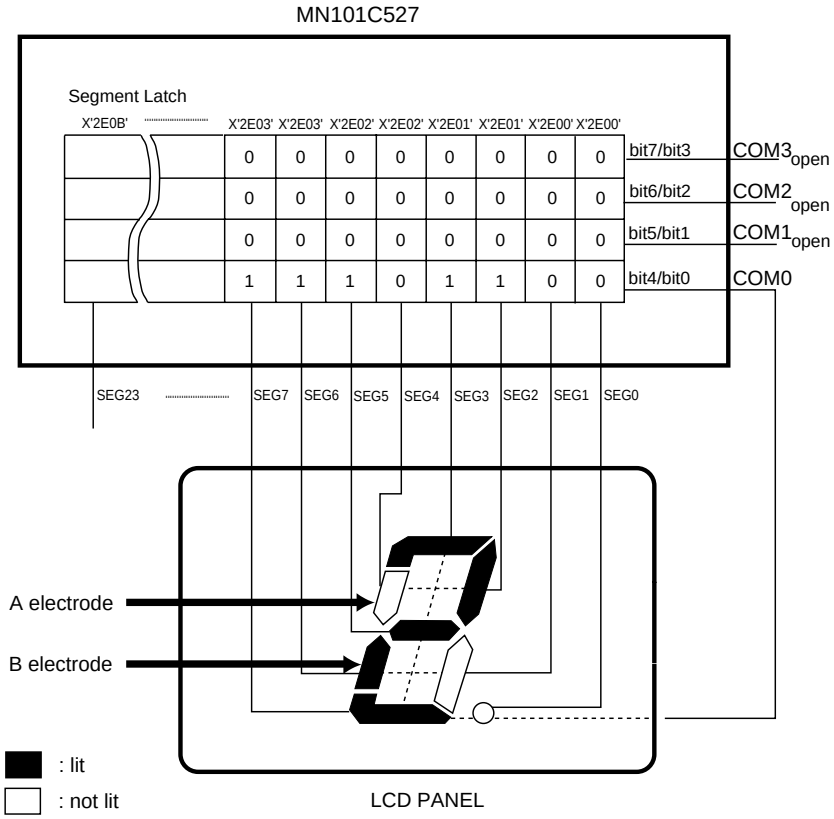
To use the voltage booster circuit, start the voltage booster operation right after the power is turned on or reset is released.

13-4 Display

Figures 13-4-1 to 13-4-4 show examples of connections, displays and waveforms of the LCD panel in these condition - in 1/2 duty, 1/3 duty, 1/4 duty and static.

13-4-1 Static

■**Static**


MN101C527
Segment Latch
X'2E0B'
X'2E03' X'2E03' X'2E02' X'2E02' X'2E01' X'2E01' X'2E00' X'2E00'
0 0 0 0 0 0 0 0 bit7/bit3 COM3open
0 0 0 0 0 0 0 0 bit6/bit2 COM2open
0 0 0 0 0 0 0 0 bit5/bit1 COM1open
1 1 1 0 1 1 0 0 bit4/bit0 COM0
SEG23
SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0
A electrode
B electrode
: lit
: not lit
LCD PANEL

		LCD ON		LCD OFF
		COM=S SEG=S	COM=S SEG=N	
LCD clock				undefined
Data		"1"	"0"	undefined
COM	V_{LC1}			
	V_{SS}			
SEG	V_{LC1}			
	V_{SS}			
COM-SEG	V_{LCD}			
	0			
	$-V_{LCD}$			
		Lit	Not lit	Not lit

S: selective voltage N: non-selective voltage V_{LCD}: LCD driver voltage

In case of static, COM(COM0) always outputs selective voltage.

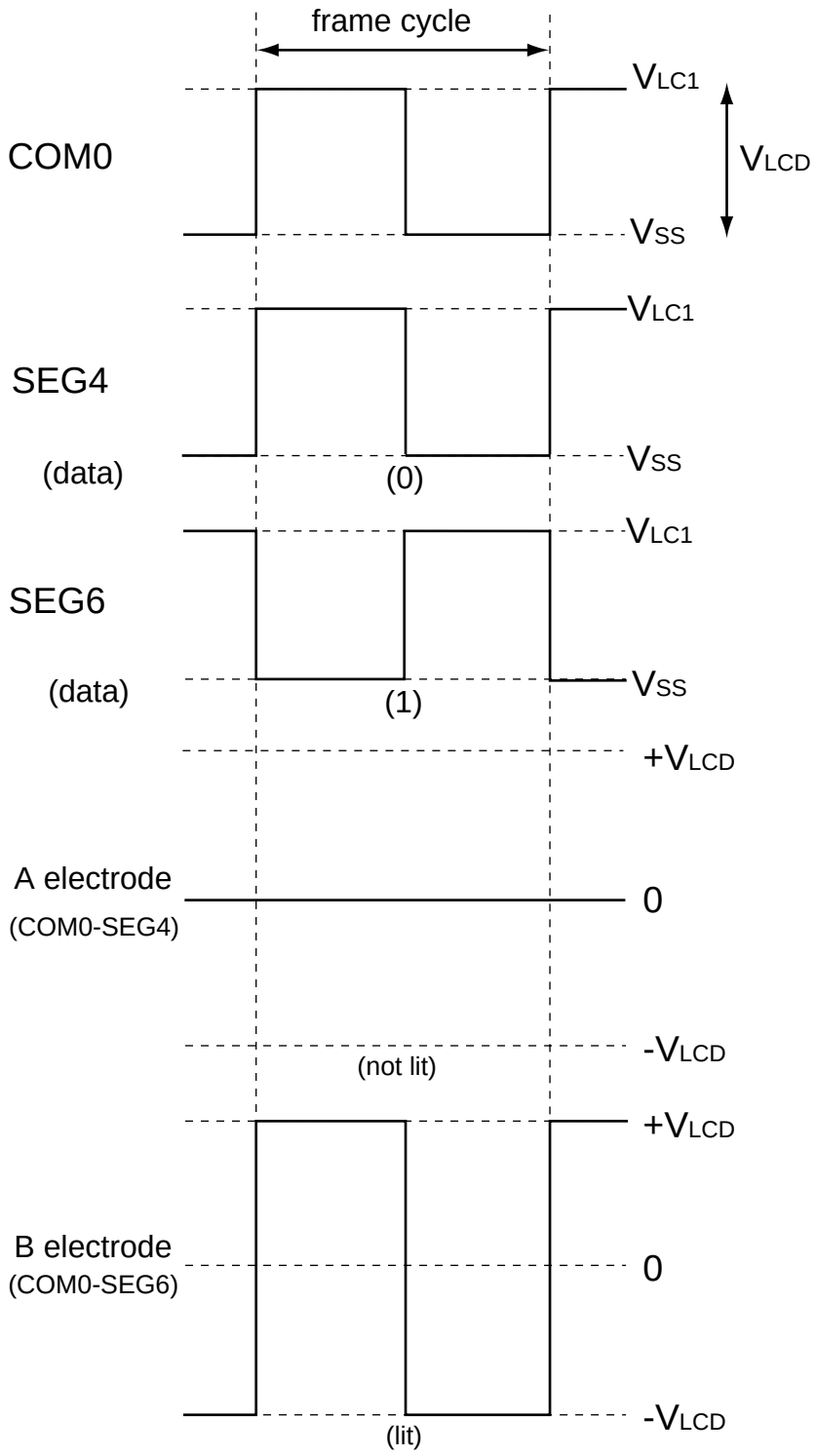


Figure 13-4-1 LCD Display in Static

13-4-2 Setup Example (static)

■Setup example of the LCD (static)

An example of setup procedure to display “2” with both segment signals (SEG0 to SEG7) and common signals (COM0), using an external divider resistor is shown below.

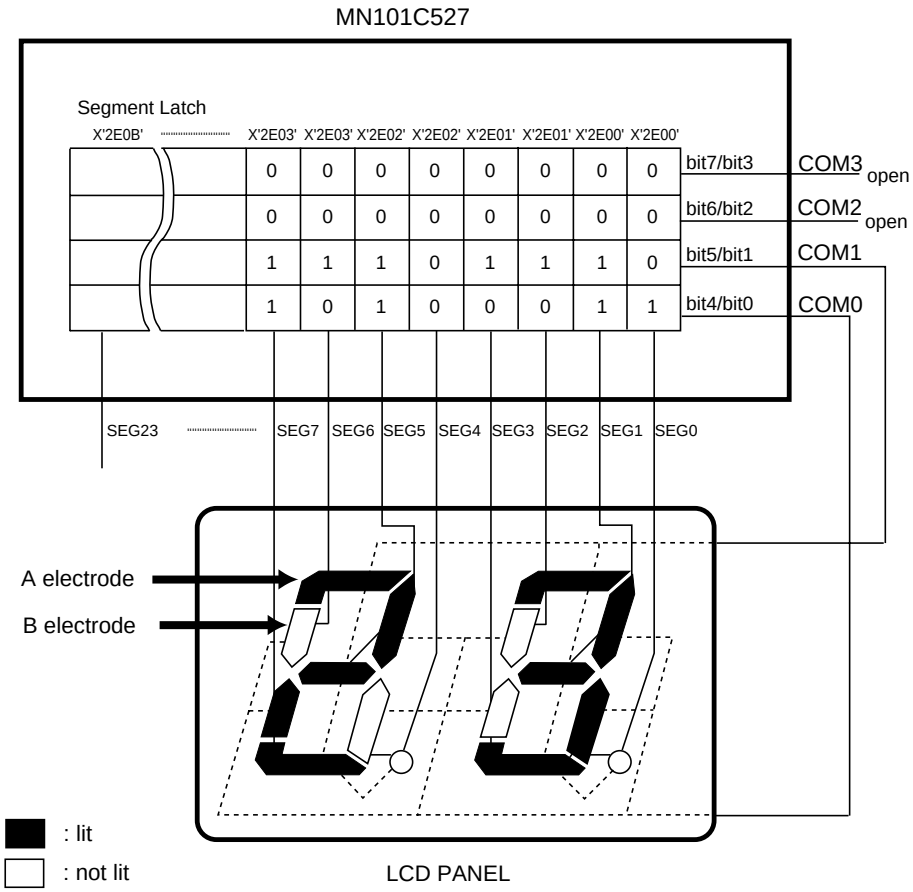
[☞ Chapter 13 13-4-1. LCD Display (static)]

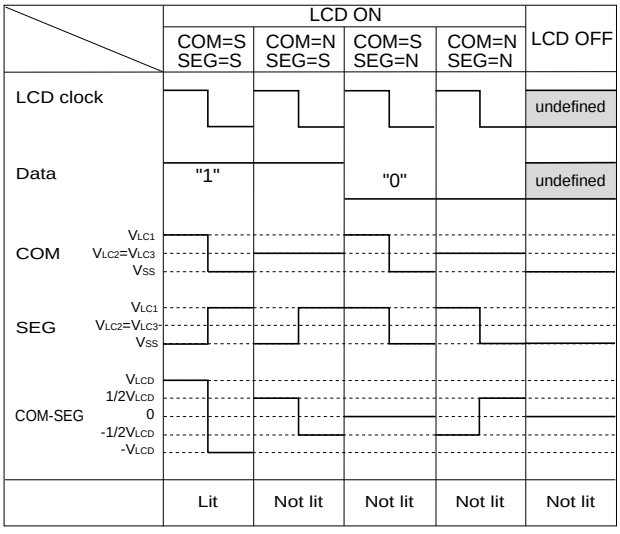
Clock source fosc=4 MHz, a LDC clock source fosc/2^{15} =122 Hz, and flame cycle=122 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register (LCMD) to stop the LCD operation.
(2) Setup the display duty LCMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LC1SEL flag of the LCD mode control register (LCMD) to enter the static drive mode.
(3) Select the LCD clock source LCMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as a LCD clock source with LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Select the segment output/port pin Select the common output/port pin LCCTR1(X’3FDB’) bp3-0 :LC1SL3-0 = 1111 LCCTR2(X’3FDA’) bp4 :COMSL0 = 1	(4) Select SEG0 to 7 with the output control register (LCCTR1), and select COM1 with the COMSL0 with the LCD mode control register 2 (LCDMD2).
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’00’ Segment output latch SEG3-2 (X’2E01’) = X’11’ Segment output latch SEG5-4 (X’2E02’) = X’10’ Segment output latch SEG7-6 (X’2E03’) = X’11’	(5) Display “2” on the display panel with the address X’2E00’ to X’2E03’ of the segment output latch SEG0-7. [☞Chapter 14 14-4-1 the LCD display example (static)]
(6) Start the LCD operation LCMD1(X’3FD9’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register (LCMD1) to start the LCD operation.

13-4-3 1/2 duty

■1/2 Duty





S: selective voltage N: non-selective voltage V_{LCD}: LCD driver voltage

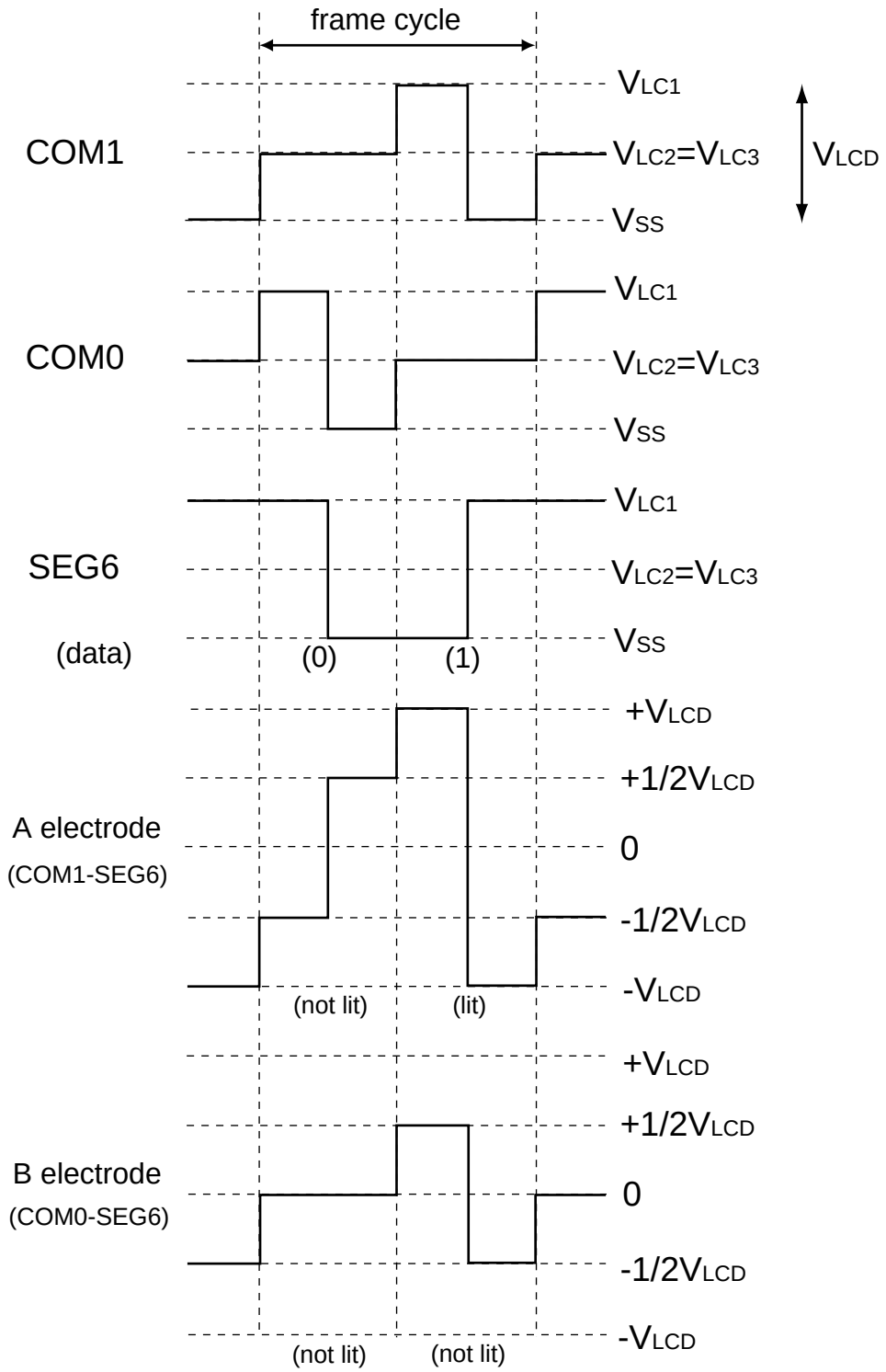


Figure 13-4-2 LCD Display (1/2 Duty)

13-4-4 Setup Example (1/2 duty)

■Setup example of the LCD (1/2 duty)

An example of setup procedure to display 8-shaped double figures “23” with both segment signals (SEG0 to SEG7) and common signals (COM0 to COM1) in 1/2 duty, 1/2 bias, using an external divider resistor is shown below.

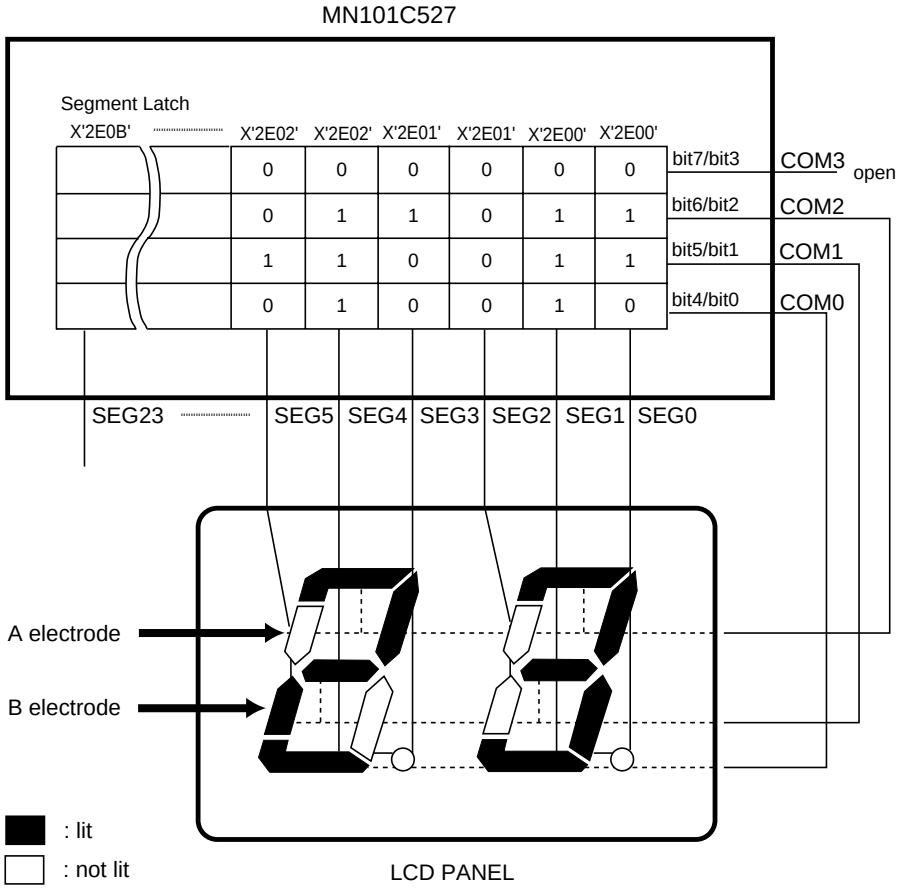
[☞ Chapter 13 13-4-3. LCD Display (1/2 duty)]

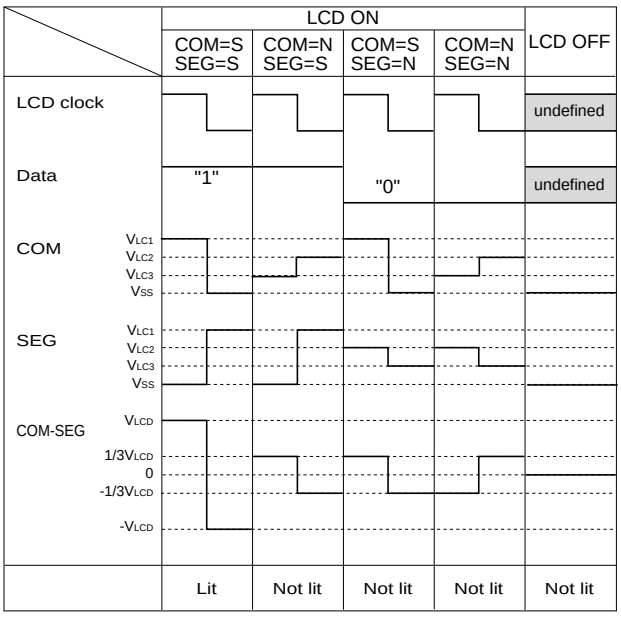
Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=61 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCDMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register 1 (LCDMD1) to stop the LCD operation.
(2) Setup the display duty LCDMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LCDTY1-0 flag of the LCD mode control register 1 (LCDMD1) to set the display duty 1/2.
(3) Select the LCD clock source LCDMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register 1 (LCDMD1).
(4) Select the segment output/port pin Select the common output/port pin LCCTR2(X’3FDB’) bp3-0 :LC1SL3-0 = 1111 LCDMD2(X’3FDA’) bp5-4 :COMSL1-0 = 11	(4) Select SEG0 to 7 with the LC1SL3-0 of the output control register (LCCTR1), and select COM1-0 with the COMSL1-0 of the LCD mode control register 2(LCDMD2).
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’31’ Segment output latch SEG3-2 (X’2E01’) = X’22’ Segment output latch SEG5-4 (X’2E02’) = X’30’ Segment output latch SEG7-6 (X’2E03’) = X’32’	(5) Display “23” on the display panel with the address X’2E00’ to X’2E03’ of the segment output latch SEG0-7. [☞ Chapter 13 13-4-3 the LCD display example (1/2 duty)]
(6) Start the LCD operation LCDMD1(X’3FD9’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register 1 (LCMD1) to start the LCD operation.

13-4-5 1/3 duty

■1/3 Duty





S: selective voltage N: non-selective voltage V_{LCD}: LCD driver voltage

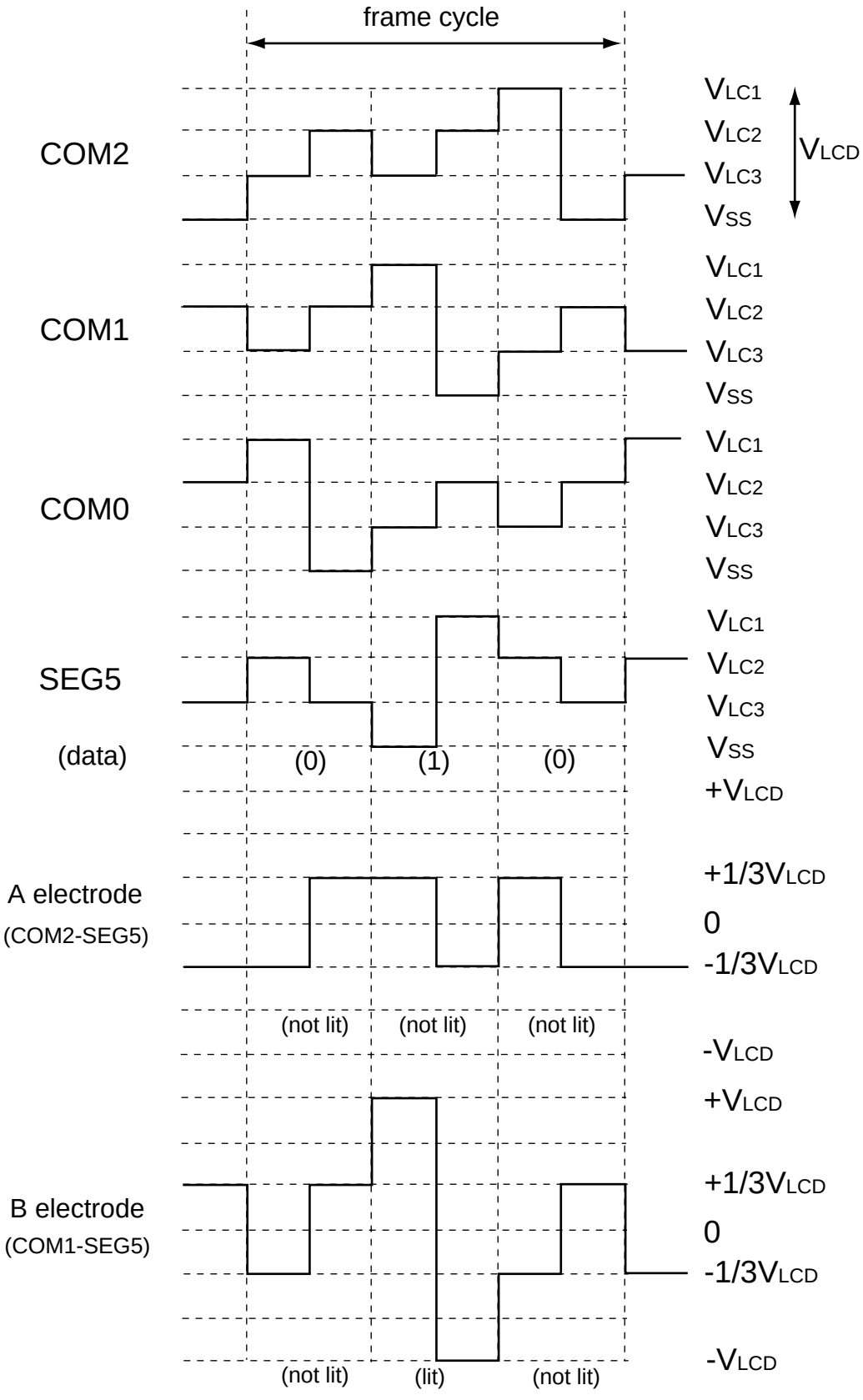


Figure 13-4-3 LCD Display (1/3 Duty)

13-4-6 Setup Example (1/3 duty)

■Setup example of the LCD (1/3 duty)

An example of setup procedure to display 8-shaped double figures “23” with both segment signals (SEG0 to SEG5) and common signals (COM0 to COM2) in 1/3 duty, 1/3 bias, using an external divider resistor is shown below.

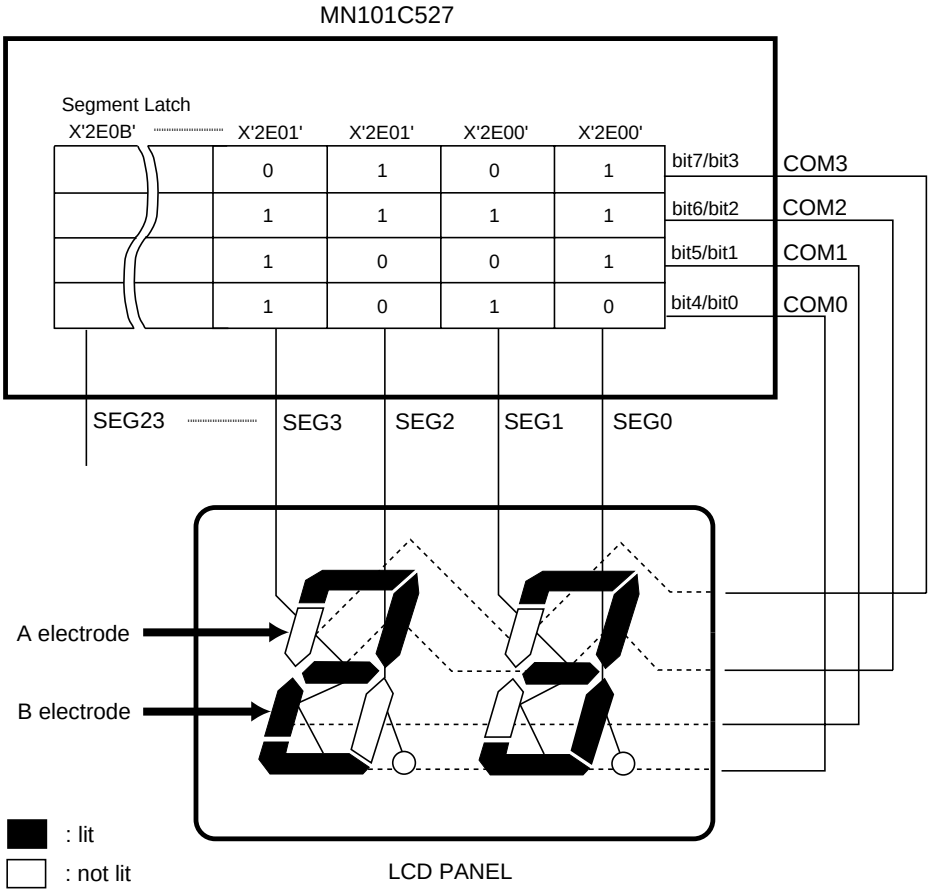
[☞ Chapter 13 13-4-5. LCD Display (1/3 duty)]

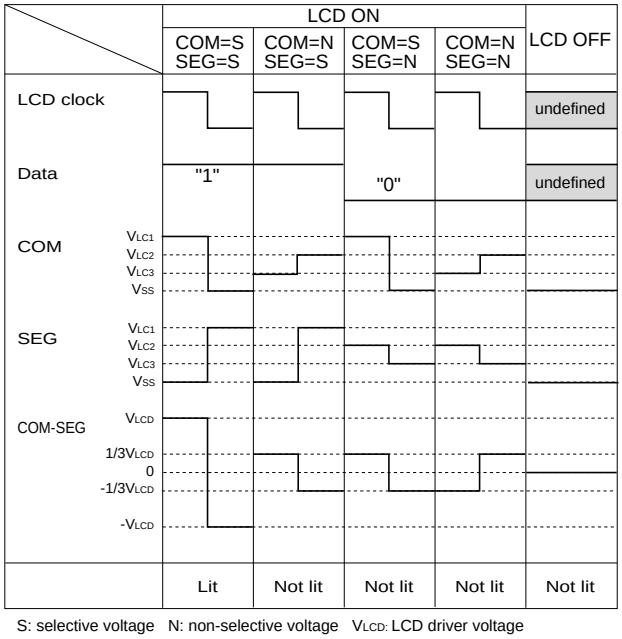
Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=41 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register 1 (LCDMD1) to stop the LCD operation.
(2) Setup the display duty LCMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LC1SEL flag of the LCD mode control register 1 (LCDMD1) to set display duty 1/3.
(3) Select the LCD clock source LCMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register 1 (LCDMD1).
(4) Select the segment output/port pin Select the common output/port pin LCCTR1(X’3FDB’) bp1 :LC1SL1 = 1 LCCTR2(X’3FDA’) bp6-4 :COMSK2-0 = 111	(4) Select SEG0 to 5 with the LC1SL3 of the output control register (LCCTR1), and select COM2-0 with the COMSL2-0 of the LCD mode control register 2 (LCDMD2).
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’76’ Segment output latch SEG3-2 (X’2E01’) = X’40’ Segment output latch SEG5-4 (X’2E02’) = X’27’	(5) Display “23” on the display panel with the address X’2E00’ to X’2E02’ (segment output latch SEG0-5). [☞ Chapter 13 13-4-5. the LCD display example (1/3 duty)]
(6) Start the LCD operation LCDMD1(X’3FD9’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register 1 (LCDMD1) to start the LCD operation.

13-4-7 1/4 duty

■1/4 Duty





S: selective voltage N: non-selective voltage V_{LCD}: LCD driver voltage

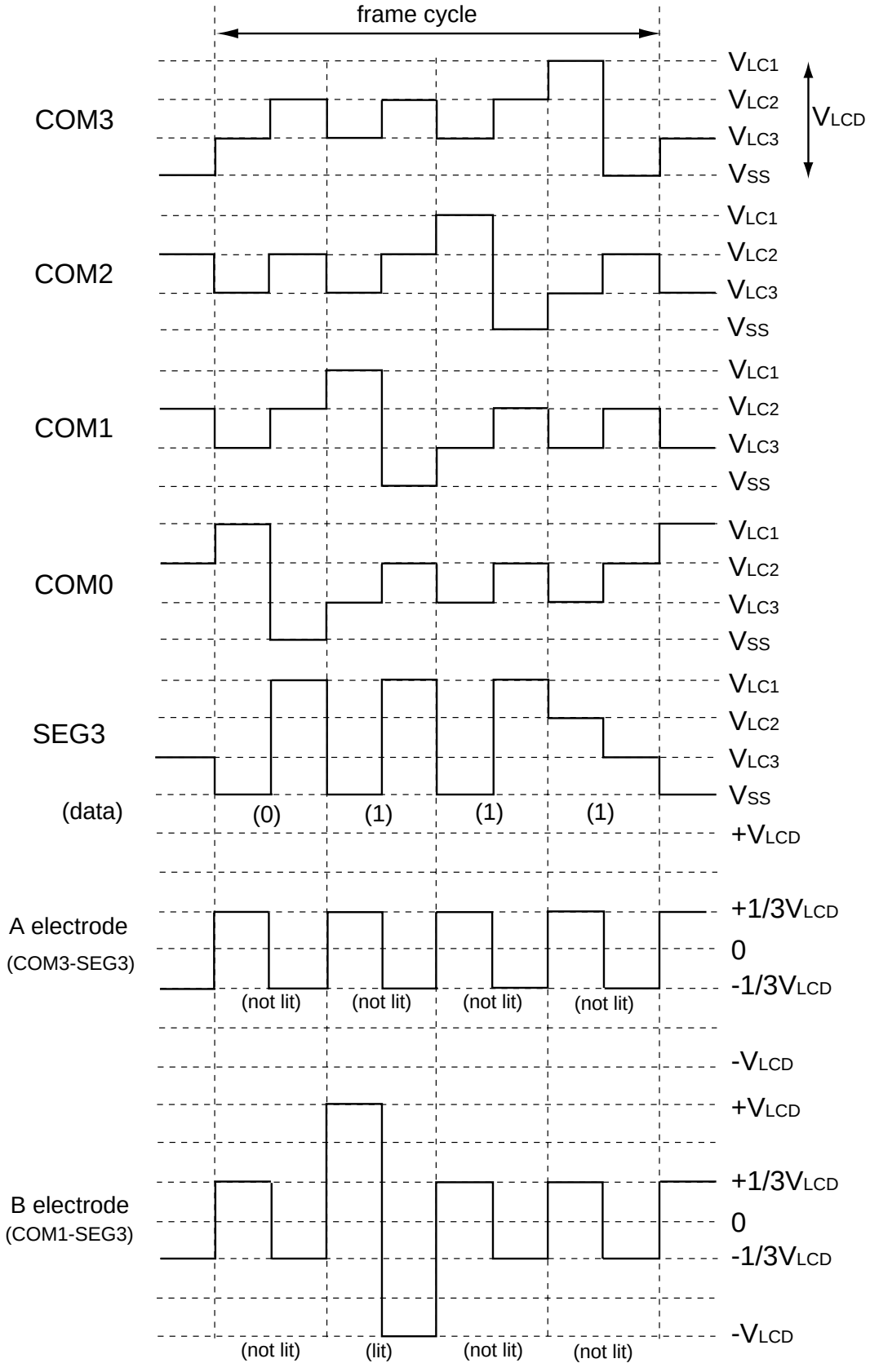


Figure 13-4-4 LCD Display (1/4 Duty)

13-4-8 Setup Example (1/4 duty)

■Setup example of the LCD (1/4 duty)

An example of setup procedure to display 8-shaped 2 figures “23” with both segment signals (SEG0 to SEG3) and common signals (COM0 to COM3) in 1/4 duty, 1/3 bias, using an external divider resistor is shown below.

[☞ Chapter 13 13-4-7. LCD Display (1/4 duty)]

Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=31 Hz are selected in this exmple.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register 1 (LCDMD1) to stop the LCD operation.
(2) Setup the display duty LCDMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 00	(2) Set the display duty 1/4 with the LC0DTY1-0 flag of the LCD mode control register 1 (LCDMD1).
(3) Select the LCD clock source LCDMD1(X’3FD9’) bp3-0 : LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register 1 (LCMD1).
(4) Select the segment output/port pin Select the common output/port pin LCCTR1(X’3FDB’) bp3-2 :LC1SL3-2 = 11 LCDMD2(X’3FDA’) bp1 :LC1SL1 = 1 bp7-4 :COMSL3-0 = 1111	(4) Select SEG0 to 3 with the LS1SL3-2 of the output control register 1 (LCCTR1) and select COM3-0 with the COSL3-0 of the LCD mode control register 2 (LCDMD2).
(5) Setup the LCD panel display data Segment output latch SEG1-0 X’2E00’ = X’5E’ Segment output latch SEG3-2 X’2E01’ = X’7C’	(5) Display “23” on the display panel with the ad dress X’2E00’ to X’2ED1’ (SEG0-3). [☞ Chapter 13 13-4-7. the LCD display example (1/4 duty)]
(6) Start the LCD operation LCDMD1(X’3FD9’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register 1 (LCDMD1) to start the LCD operation.

Chapter 14 Appendices

14-1 EPROM Version

14-1-1 Overview

The EPROM version is equivalent to MN101C527 excepts its Mask ROM is substituted with an electrically programmable EPROM.
We offer MN101CP52ABL and PX-AP101C52-BC for MN101C527.

The MN101CP52ABL is sealed in plastic.
Once a data is written to the internal EPROM, it cannnot be erased.
PX-AP101C52-BC is sealed in a ceramic package with a window. Written data can be erased by exposing the physical chip to intense ultraviolet radiation. We offer 64-pin flat package for the PX-AP101C52-BC.

When the EPROM version is set to EPROM programming mode, its functions as a microcontroller is halted, and then the internal EPROM can be programmed. For EPROM mode pin connection, refer to figure 14-1-2. Programming Adapter Connection.

The specification for writing to the internal EPROM are the same as for a general-purpose 1 M-bit EPROM (V_{PP} = 12.5 V; tpw = 0.2 ms). Therefore, by useing a dedicated programming adapter (supplied by Panasonic) which can convert the 64-pin EPROM versions to 32 pin, having the same configuration as a normal EPROM, a general-purpose EPROM writer can be used for read and write operations.

This EPROM Version is described on the following items;

- Cautions on use of the internal EPROM
- Erasing data in windowed package (PX-AP101C52-BC)
- Differences between Mask ROM version and EPROM versions
- Writing to the EPROM built-in microcontroller
- Cautions on use of the ROM writer

14-1-2 Caution on Use

EPROM Version differs from the MN101C527 series mask ROM version in some of its electrical characteristics. The user should be aware of the following cautions :

(1) To prevent data from being erased by ultraviolet light after a program is written, affix seals impermeable to UV rays to the glass sections at the top and side sections of the CPU. (PX-AP101C52-BC)

(2) Because of device characteristics of the MN101CP52ABL, a writing test cannot be performed on all bits.Therefore, the reliability of data writing may not be 100% ensured.

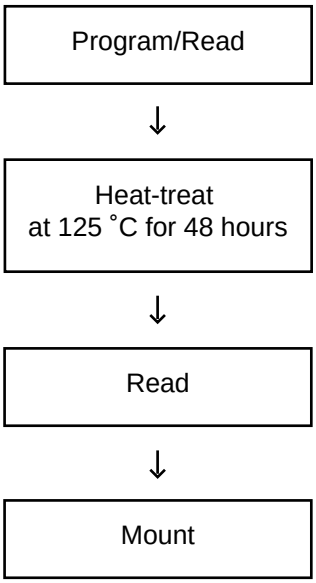
(3) When a program is written, be sure that V_{DD} power supply (6 V) is connected before applying the V_{PP} power supply (12.5 V). Disconnect the V_{PP} supply before disconnecting the V_{DD} supply.

(4) V_{PP} should never exceed 13.5 V including overshoot.

(5) If a device is removed while a V_{PP} of +12.5 V is applied, device reliability may be damaged.

(6) At NCE=V_{IL}, do not change Vpp from V_{IL} to +12.5 V or from +12.5 V to V_{IL}.

(7) After a program is written, screening at a high temperature storage is recommended before mounting.



14-1-3 Erasing Data in Windowed Package (PX-AP101C52-BC)

Irradiating the chip through the window (PX-AP101C52-BC) with 253.7 nm ultraviolet radiation erases the data by changing all "0" bits to "1".

The recommended exposure is 10 W•s/cm^2 -the equivalent of 15 to 20 minutes 2 cm to 3 cm below a commercial ultraviolet lamp producing an illumination intensity of 12,000 µW/cm^2 at the package surface. Remove any filters attached to the lamp. Installing a lamp reflector increases the illumination intensity by a factor of 1.4 to 1.8, decreasing the erasure time.

If the window becomes dirty with oil, adhesive, etc., UV light permeability will decrease, causing the erasure time to increase considerably. If this happens, clean with alcohol or another solvent that will not harm the package. The recommended above provides sufficient leeway, with several times the amount of time it takes to erase all the bits. However, this value will reliably erase data over all temperature and voltage ranges, and should not be altered. The level of illumination should be regularly checked and the lamp operation verified.

Erasure begins when the EPROM is exposed to light with a wavelength shorter than 400 nm. Since fluorescent light and sunlight have wavelengths in this range, exposure to these light sources for extended periods of time could cause inadvertant erasure. To prevent this, cover the window with an opaque label.

Data is not erased at wavelengths. However, because of typical semiconductor characteristics, the circuit may malfunction if the chip is exposed to an extremely high illumination intensity. The chip will operate normally if this exposure is stopped. However, for areas where it is continuous, take necessary precautions.

14-1-4 Differences between Mask ROM Version and EPROM Version

The differences between the Mask ROM version and the EPROM version of this LSI are as follows ;

Table 14-1-1 Differences between the Mask ROM version and the EPROM version

	MN101C527 (Masked ROM Version)	EPROM version
Operationg voltage (*)	4.5 V to 5.5 V (at 0.1 µs/20 MHz) 2.7 V to 5.5 V (at 0.25 µs/8 MHz) 2.0 V to 5.5 V (at 1.00 µs/2 MHz)	4.5 V to 5.5 V (at 0.1 µs/20 MHz) 2.7 V to 5.5 V (at 0.25 µs/8 MHz) 2.3 V to 5.5 V (at 1.00 µs/2 MHz)
Pin DC characteristics	The masked ROM and EPROM versions share the same design specifications for I/O currents, input levels, etc.	
ROM capacity	16 KB	32 KB
Oscillation characteristics	Matching evaluation of each version is neccessary when these versions are rotated for mass production	
Noise characteristics	Matching evaluation of each version is neccessary when these versions are rotated for mass production	
Operating tempreture	-40 °C to +85 °C	-20 °C to +70 °C

(*s) At machine cycle is 2 x cycle of the oscillation clock.

There are no other functional differences.

14-1-5 Writing to EPROM built-in Microcontroller

The device type set by each ROM writer should be set to the mode for writing 1 M-bit EPROM. Set the writing voltage to 12.5 V.

■ Mounting the device on the programming adapter and the position of the No.1 pin

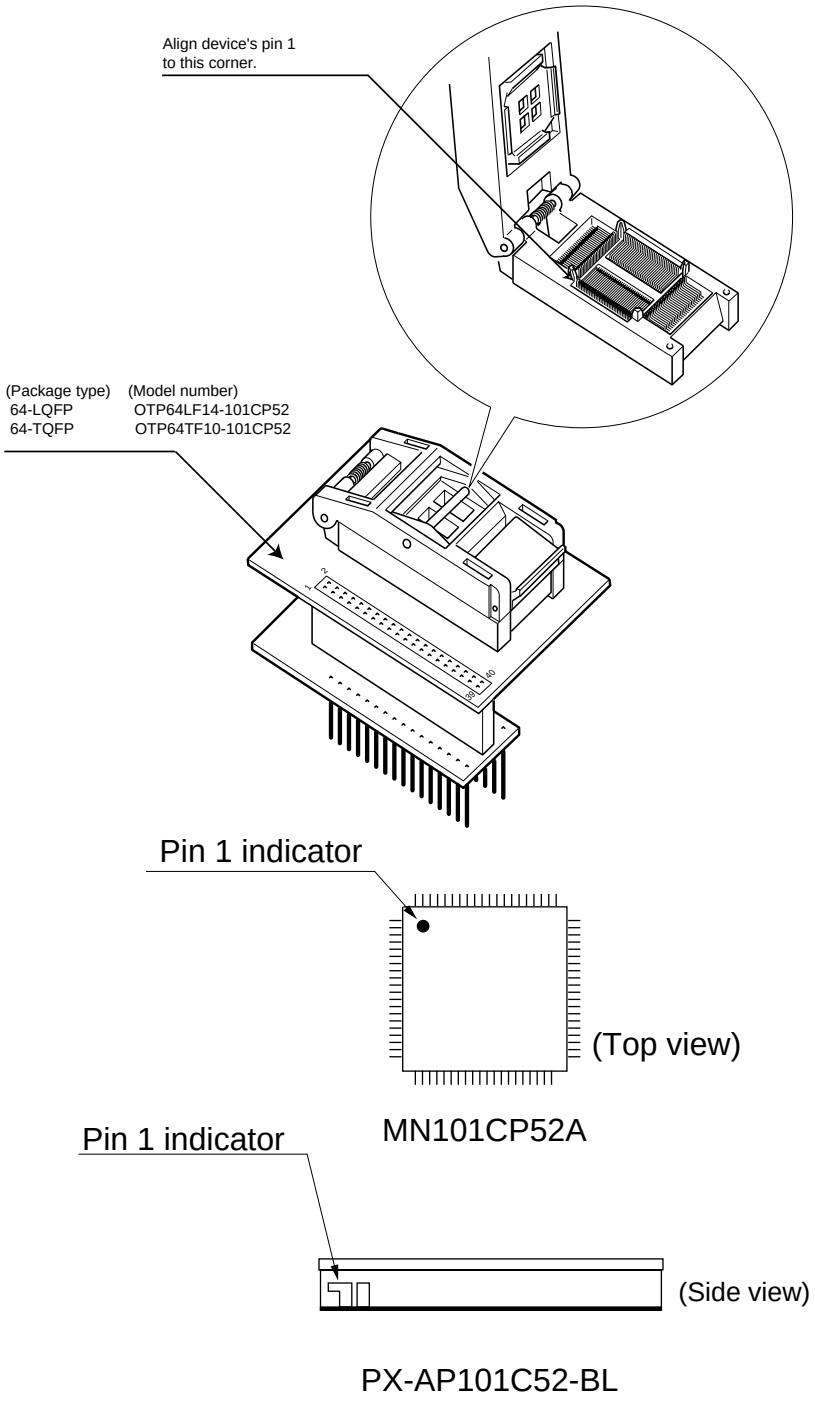


Figure 14-1-1 Mounting a Device on Programming Adapter and the Position of No.1 Pin

■ ROM writer

Refer followig table for device type selection.

Table 14-1-2 Device Type Selection

Type	Manufacturer	Device	Remarks
Pecker30	Aval Data Corporation	Hitachi 27C101	
R4945A	Advantest Corporation	Hitachi 27C101	
LabSite	Data I/O Corporation	Hitachi 27C101	ID check and pin connection check are forbidden.
AF-9704 AF-9705	Ando Electric Co., Ltd.	Hitachi 27C101	

14-1-6 Cautions on Operation of ROM Writer

■Cautions on Handling the ROM writer

(1) The V_{PP} programming voltage for the EPROM versions is 12.5 V.
Programming with a 21 V ROM writer can lead to damage. The ROM writer specifications must match those for standard 1 M-bit EPROM : V_{PP}=12.5 V ; tpw=0.2 ms.

(2) Make sure that the socket adapter matches the ROM writer socket and that the chip is correctly mounted in the socket adapter. Faulty connections can damage the chip.

(3) After clearing all memory of the ROM writer, load the program to the ROM writer.
(Write data X'FF to address X'00000' to X'1FFFF').

(4) After confirming the device type, write the loaded program in (3) to this LSI address, from x'4000' to the final address of the internal ROM.

The internal ROM space of this LSI starts from x'4000' .
[☞ Chapter 2 Memory Space]

This writer has no internal ID codes of "Silicon Signature" and "Intelligent Identifier" of the auto-device selection command of ROM writer. If the auto-device selection command is to be executed for this writer, the device is likely damaged. Therefore, never use this command.

■When the writing is disabled

When the writing is disabled, check the following points.

(1) Check that the device is mounted correctly on the socket (pin bending, connection failure).

(2) Check that the erase check result is no problem.

(3) Check that the adapter type is identical to the device name.

(4) Check that the writing mode is set correctly.

(5) Check that the data is correctly transferred to the ROM writer.

(6) Recheck the check points (1), (2) and (3) provided on the above paragraph of 'Cautions on Handling the ROM writer'.

14-1-7 Programming Adapter Connection

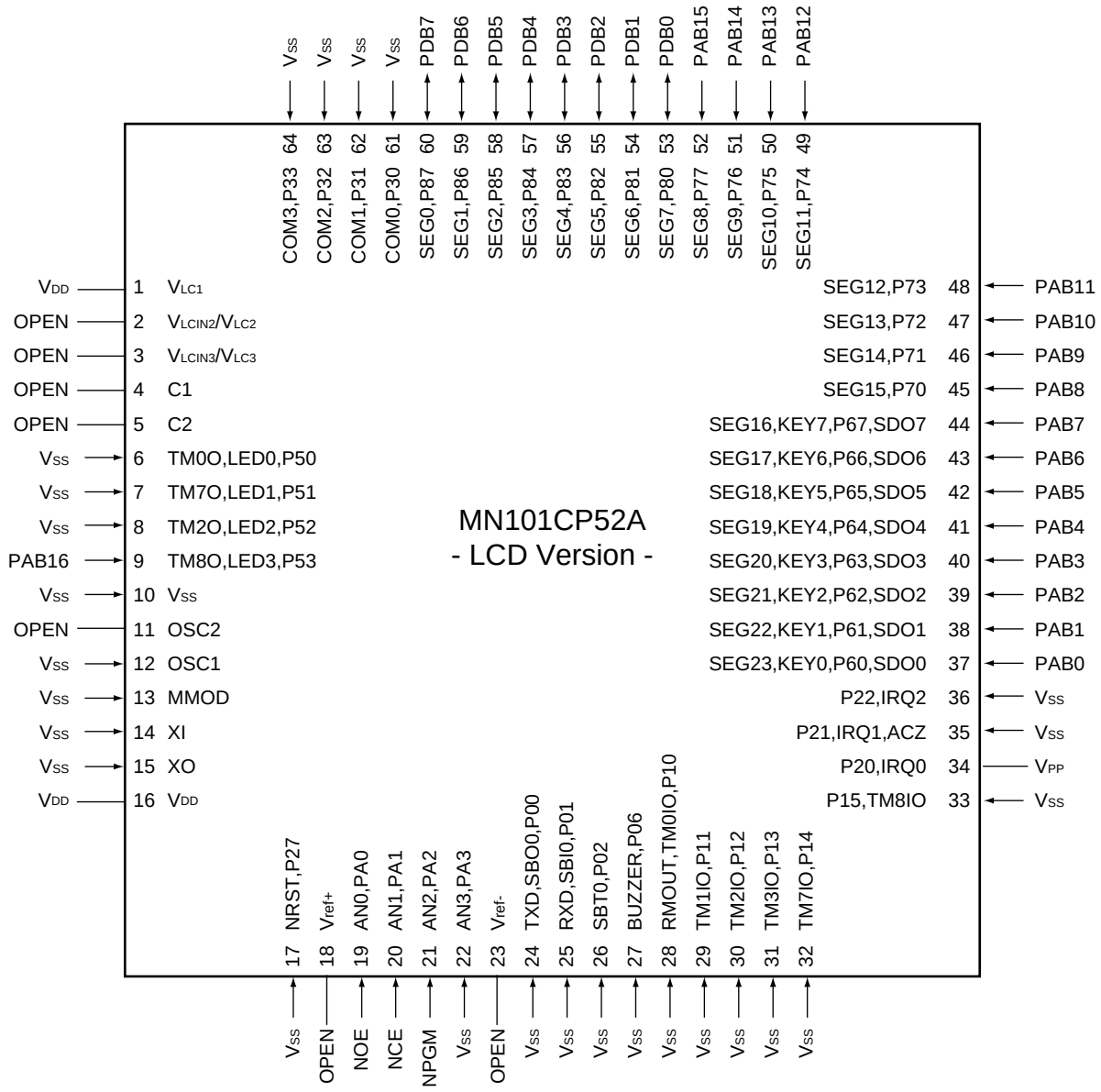


Figure 14-1-2 EPROM Programming Adapter Connection

14-2 Probe Switches

14-2-1 PRB-MBB101C52-M

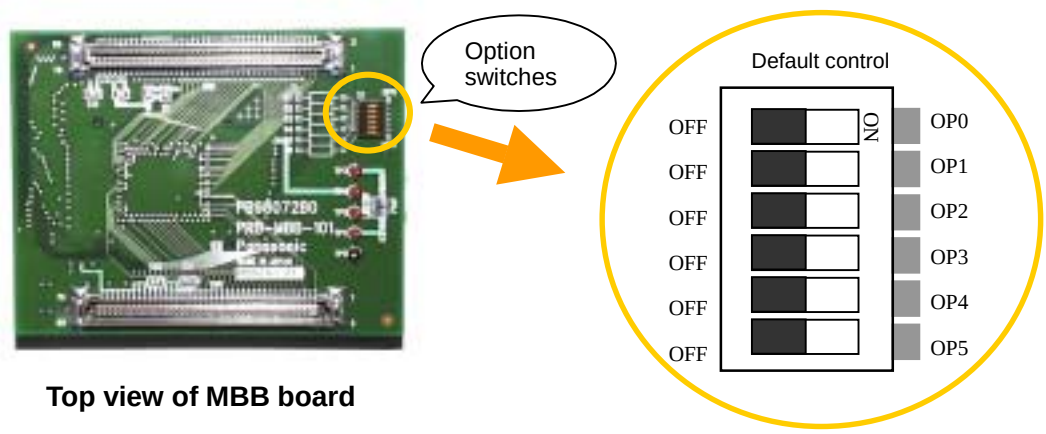
- This probe must be used with the following boards.

  - Connector board : PX-CN101-M
  - MBB board : PRB-MBB101C52-M
  - Adapter board : PRB-ADP101C64-M
  - Dummy target : PRB-DMY101C52-M

    The dummy target should be connected when ICE is operated independently, the adapter board should be connected at connection to the target.

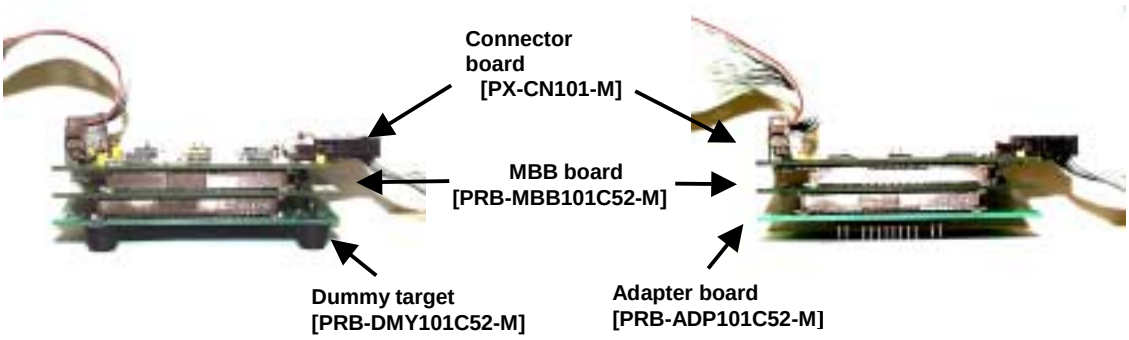
- This probe is mounted the switches for mask option.
- The option switches are not available.

Figure1.Layout of option switches



Top view of MBB board

Figure2.Composition with PRB-MBB101C52-M



- When ICE is operated independently.

- At connection to the target

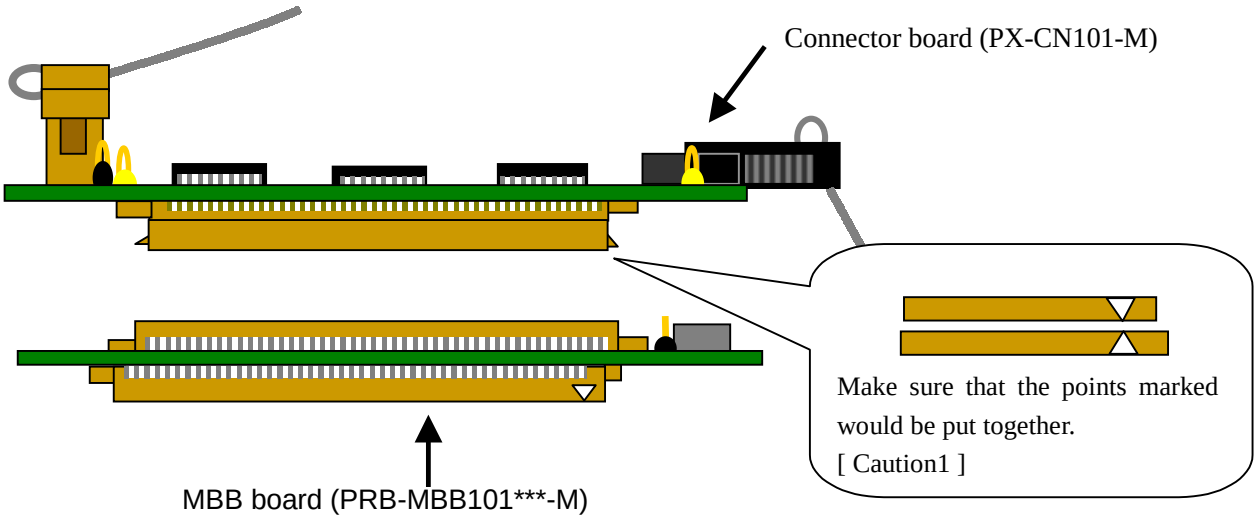
14-2-2 PX-CN101-M

This board can be used for any MBB models(product No.PRB-MBB101***-M) of MN101 series.
(Please visit our website for the latest information on the product.)

Figure1.PX-CN101-M Layout

< How to connect >

Figure2.Connecting a PX-CN101-M to a MBB board



[Caution1]
Connect CNC of PX-CN101-M to CNC of PRB-MBB101***-M, and
CND of PX-CN101-M to CND of PRB-MBB101***-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

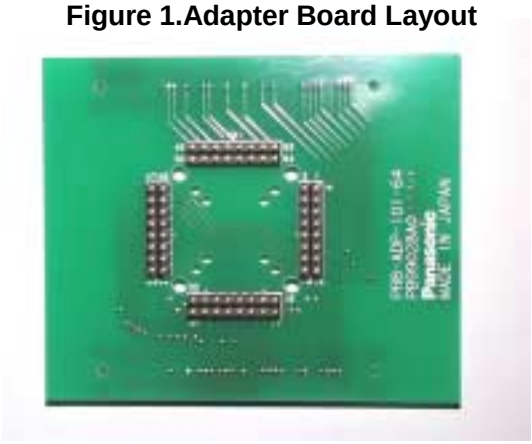
14-2-3 PRB-ADP101-64-M

When connected to the target, use this board with MBB board.
This board can be used with the following boards.
(The product type is subject to change without prior notice. The latest information should be confirmed on our web site.)

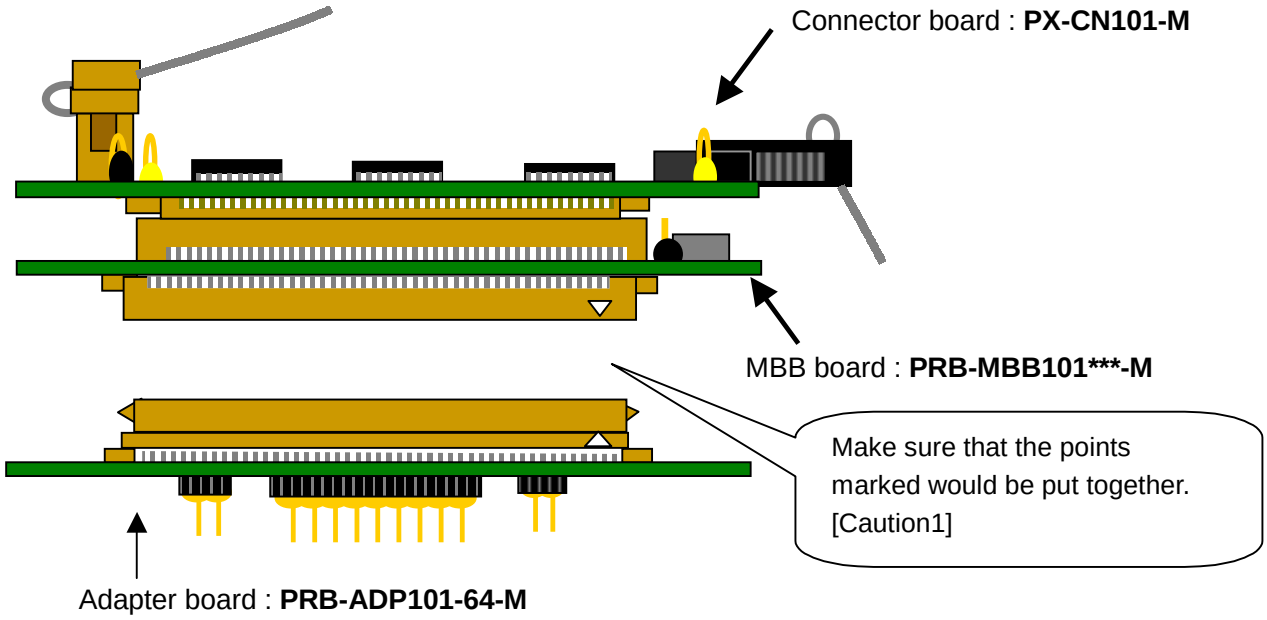
- PRB-MBB101C52-M
- PRB-MBB101C58-M

Improper matching may cause any damage to the ICE.

Figure 1.Adapter Board Layout



< How to connect >


Connector board : **PX-CN101-M**
MBB board : **PRB-MBB101***-M**
Make sure that the points marked would be put together. [Caution1]
Adapter board : **PRB-ADP101-64-M**

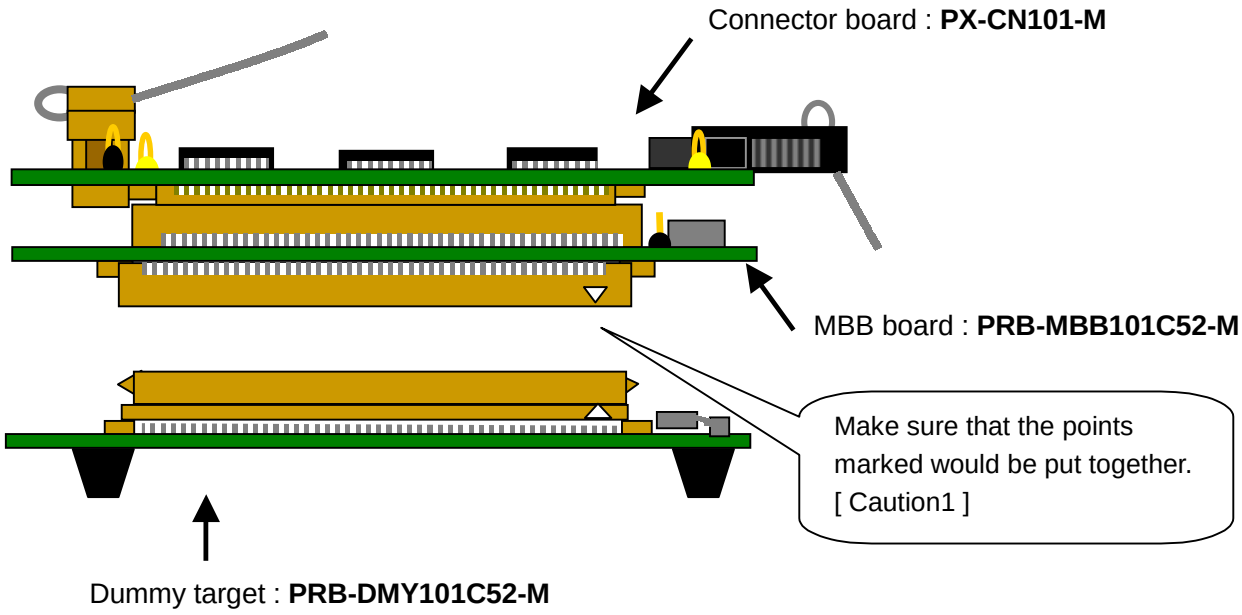
[Caution1]
Connect CNE of PRB-MBB101***-M to CNE of PRB-ADP101-64-M, and
CNF of PRB-MBB101***-M to CNF of PRB-ADP101-64-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

14-2-4 PRB-DMY101C52-M

Dummy target boards differ depending upon the models. This board can be used for only 101C52.
When unconnected to the target, use this board with the PRB-MBB101C52-M.
Improper matching may cause any damage to the ICE

Figure 1.PRB-DMY101C52-M Layout

< How to connect >


Connector board : **PX-CN101-M**
MBB board : **PRB-MBB101C52-M**
Make sure that the points marked would be put together.
[Caution1]
Dummy target : **PRB-DMY101C52-M**

[Caution1]
Connect CNE of PRB-MBB101C52-M to CNE of PRB-DMY101C52-M, and CNF of PRB-MBB101C52-M to CNF of PRB-DMY101C52-M.
When connect the boards, make sure that they are connected without tilt.
If put pressure on one side of the board, that cause any damage to the pins.

14-3 Instruction Set

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Machine Code Ext.	1	2	3	4	5	6	7	8	9	10	11	Notes
Data Move Instructions																						
MOV	MOV Dn,Dm	Dn→Dm	--	--	--	--	2	1			1010	DnDm										
	MOV imm8,Dm	imm8→Dm	--	--	--	--	4	2			1010	DmDm	<#8.	...>								
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3		0010	1001	01Dn										
	MOV PSW,Dm	PSW→Dm	--	--	--	--	3	2		0010	0001	01Dm										
	MOV (An),Dm	mem8(An)→Dm	--	--	--	--	2	2			0100	1ADm										
	MOV (d8,An),Dm	mem8(d8+An)→Dm	--	--	--	--	4	2			0110	1ADm	<d8.	...>								*1
	MOV (d16,An),Dm	mem8(d16+An)→Dm	--	--	--	--	7	4		0010	0110	1ADm	<d16	....	....	...>						
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	--	--	--	--	3	2			0110	01Dm	<d4>									*2
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	--	--	--	--	5	3		0010	0110	01Dm	<d8.	...>								*3
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	--	--	--	--	7	4		0010	0110	00Dm	<d16	....	....	...>						
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	--	--	--	--	4	2			0110	00Dm	<io8	...>								
	MOV (abs8),Dm	mem8(abs8)→Dm	--	--	--	--	4	2			0100	01Dm	<abs	8..>								
	MOV (abs12),Dm	mem8(abs12)→Dm	--	--	--	--	5	2			0100	00Dm	<abs	12..	...>							
	MOV (abs16),Dm	mem8(abs16)→Dm	--	--	--	--	7	4		0010	1100	00Dm	<abs	16..	....	...>						
	MOV Dn,(Am)	Dn→mem8(Am)	--	--	--	--	2	2			0101	1aDn										
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	--	--	--	--	4	2			0111	1aDn	<d8.	...>								*1
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	--	--	--	--	7	4		0010	0111	1aDn	<d16	....	....	...>						
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	--	--	--	--	3	2			0111	01Dn	<d4>									*2
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	--	--	--	--	5	3		0010	0111	01Dn	<d8.	...>								*3
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	--	--	--	--	7	4		0010	0111	00Dn	<d16	....	....	...>						
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	--	--	--	--	4	2			0111	00Dn	<io8	...>								
	MOV Dn,(abs8)	Dn→mem8(abs8)	--	--	--	--	4	2			0101	01Dn	<abs	8..>								
	MOV Dn,(abs12)	Dn→mem8(abs12)	--	--	--	--	5	2			0101	00Dn	<abs	12..	...>							
	MOV Dn,(abs16)	Dn→mem8(abs16)	--	--	--	--	7	4		0010	1101	00Dn	<abs	16..	....	...>						
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	--	--	--	--	6	3			0000	0010	<io8	...>	<#8.	...>						
	MOV imm8,(abs8)	imm8→mem8(abs8)	--	--	--	--	6	3			0001	0100	<abs	8..>	<#8.	...>						
	MOV imm8,(abs12)	imm8→mem8(abs12)	--	--	--	--	7	3			0001	0101	<abs	12..	...>	<#8.	...>					
	MOV imm8,(abs16)	imm8→mem8(abs16)	--	--	--	--	9	5		0011	1101	1001	<abs	16..	....	...>	<#8.	...>				
	MOV Dn,(HA)	Dn→mem8(HA)	--	--	--	--	2	2			1101	00Dn										
MOVW	MOVW (An),DWm	mem16(An)→DWm	--	--	--	--	2	3			1110	00Ad										
	MOVW (An),Am	mem16(An)→Am	--	--	--	--	3	4		0010	1110	10Aa										*4
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	--	--	--	--	3	3			1110	011d	<d4>									*2
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	--	--	--	--	3	3			1110	010a	<d4>									*2
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	--	--	--	--	5	4		0010	1110	011d	<d8.	...>								*3
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	--	--	--	--	5	4		0010	1110	010a	<d8.	...>								*3
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	--	--	--	--	7	5		0010	1110	001d	<d16	....	....	...>						
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	--	--	--	--	7	5		0010	1110	000a	<d16	....	....	...>						
	MOVW (abs8),DWm	mem16(abs8)→DWm	--	--	--	--	4	3			1100	011d	<abs	8..>								
	MOVW (abs8),Am	mem16(abs8)→Am	--	--	--	--	4	3			1100	010a	<abs	8..>								
	MOVW (abs16),DWm	mem16(abs16)→DWm	--	--	--	--	7	5		0010	1100	011d	<abs	16..	....	...>						
	MOVW (abs16),Am	mem16(abs16)→Am	--	--	--	--	7	5		0010	1100	010a	<abs	16..	....	...>						
	MOVW DWn,(Am)	DWn→mem16(Am)	--	--	--	--	2	3			1111	00aD										
	MOVW An,(Am)	An→mem16(Am)	--	--	--	--	3	4		0010	1111	10aA										*4
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	--	--	--	--	3	3			1111	011D	<d4>									*2
	MOVW An,(d4,SP)	An→mem16(d4+SP)	--	--	--	--	3	3			1111	010A	<d4>									*2
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	011D	<d8.	...>								*3
	MOVW An,(d8,SP)	An→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	010A	<d8.	...>								*3
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	001D	<d16	....	....	...>						
	MOVW An,(d16,SP)	An→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	000A	<d16	....	....	...>						
	MOVW DWn,(abs8)	DWn→mem16(abs8)	--	--	--	--	4	3			1101	011D	<abs	8..>								
	MOVW An,(abs8)	An→mem16(abs8)	--	--	--	--	4	3			1101	010A	<abs	8..>								
	MOVW DWn,(abs16)	DWn→mem16(abs16)	--	--	--	--	7	5		0010	1101	011D	<abs	16..	....	...>						
	MOVW An,(abs16)	An→mem16(abs16)	--	--	--	--	7	5		0010	1101	010A	<abs	16..	....	...>						
	MOVW DWn,(HA)	DWn→mem16(HA)	--	--	--	--	2	3			1001	010D										
	MOVW An,(HA)	An→mem16(HA)	--	--	--	--	2	3			1001	011A										
	MOVW imm8,DWm	sign(imm8)→DWm	--	--	--	--	4	2			0000	110d	<#8.	...>								*5
	MOVW imm8,Am	zero(imm8)→Am	--	--	--	--	4	2			0000	111a	<#8.	...>								*6
	MOVW imm16,DWm	imm16→DWm	--	--	--	--	6	3			1100	111d	<#16	....	....	...>						

*1 d8 sign-extension *4 A=An, a=Am
*2 d4 zero-extension *5 #8 sign-extension
*3 d8 zero-extension *6 #8 zero-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
	MOVW imm16,Am	imm16→Am	--	--	--	--	6	3			1101	111a	<#16	....	....	...>						
	MOVW SP,Am	SP→Am	--	--	--	--	3	3			0010	0000	100a									
	MOVW An,SP	An→SP	--	--	--	--	3	3			0010	0000	101A									
	MOVW DWn,DWm	DWn→DWm	--	--	--	--	3	3			0010	1000	00Dd									*1
	MOVW DWn,Am	DWn→Am	--	--	--	--	3	3			0010	0100	11Da									
	MOVW An,DWm	An→DWm	--	--	--	--	3	3			0010	1100	11Ad									
	MOVW An,Am	An→Am	--	--	--	--	3	3			0010	0000	00Aa									*2
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	--	--	--	--	2	3			1111	10Dn										
	PUSH An	SP-2→SP,An→mem16(SP)	--	--	--	--	2	5			0001	011A										
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	--	--	--	--	2	3			1110	10Dn										
	POP An	mem16(SP)→An,SP+2→SP	--	--	--	--	2	4			0000	011A										
EXT	EXT Dn,DWm	sign(Dn)→DWm	--	--	--	--	3	3			0010	1001	000d									*3
Arithmetic manupulation instructions																						
ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2			0011	0011	DnDm									
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2			1000	00Dm	<#4>									*6
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2			0000	10Dm	<#8.	...>								
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○		0011	1011	DnDm									
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○		0010	0101	00Dd									*1
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○		0010	0101	10Da									
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2			1110	110a	<#4>									*6
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3			0010	1110	110a	<#8.	...>							*7
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4			0010	0101	011a	<#16	....	....	...>					
	ADDW imm4,SP	SP+sign(imm4)→SP	--	--	--	--	3	2			1111	1101	<#4>									*6
	ADDW imm8,SP	SP+sign(imm8)→SP	--	--	--	--	4	2			1111	1100	<#8.	...>								*7
	ADDW imm16,SP	SP+imm16→SP	--	--	--	--	7	4			0010	1111	1100	<#16	....	....	...>					
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4			0010	0101	010d	<#16	....	....	...>					
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○		0010	1000	1aDn									*8
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○		0010	1001	1aDn									
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○		0010	1010	DnDm									
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1			1000	01Dn										
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3			0010	1010	DmDm	<#8.	...>							
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○		0010	1011	DnDm									
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3			0010	0100	00Dd									*1
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3			0010	0100	10Da									
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4			0010	0100	010d	<#16	....	....	...>					
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4			0010	0100	011a	<#16	....	....	...>					
MULU	MULU Dn,Dm	Dm*Dn→DWk	0	●	●	●	3	8			0010	1111	111D									*4
DIVU	DIVU Dn,DWm	DWm/Dn→DWm-l...DWm-h	●	●	●	●	3	9			0010	1110	111d									*5
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2			0011	0010	DnDm									
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100	00Dm	<#8.	...>								
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000	0100	<abs 8..>	<#8.	...>							
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000	0101	<abs 12..	...>	<#8.	...>						
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5			0011	1101	1000	<abs 16..	....	...>	<#8.	...>				
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3			0010	1000	01Dd									*1
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3			0010	0101	11Da									
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3			0010	0000	01Aa									*2
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100	110d	<#16	....	....	...>						
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101	110a	<#16	....	....	...>						
Logical manipulation instructions																						
AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2			0011	0111	DnDm									
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2			0001	11Dm	<#8.	...>								
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3			0010	1001	0010	<#8.	...>							
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2			0011	0110	DnDm									
	OR imm8,Dm	DmIimm8→Dm	0	●	0	●	4	2			0001	10Dm	<#8.	...>								
	OR imm8,PSW	PSWIimm8→PSW	●	●	●	●	5	3			0010	1001	0011	<#8.	...>							
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2			0011	1010	DnDm									*9
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3			0011	1010	DmDm	<#8.	...>							

*1 D=DWn, d=DWm
*2 A=An, a=Am
*3 d=DWm
*4 D=DWk
*5 D=DWm
*6 #4 sign-extension
*7 #8 sign-extension
*8 Dn zero extension
*9 m≠n

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
NOT	NOT Dn	¯Dn→Dn=	0	●	0	●	3	2		0010	0010	10Dn										
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	--	●	●	3	2	○	0010	0011	10Dn										
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○	0010	0011	11Dn										
ROR	ROR Dn	Dn.Isb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○	0010	0010	11Dn										

Bit manipulation instructions

BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	●	0	●	5	5		0011	1000	0bp.	<io8	...>								
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	●	0	●	4	4			1011	0bp.	<abs	8..>								
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	●	0	●	7	6		0011	1100	0bp.	<abs	16..	....	...>						
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	●	0	●	5	5		0011	1000	1bp.	<io8	...>								
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	●	0	●	4	4			1011	1bp.	<abs	8..>								
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	●	0	●	7	6		0011	1100	1bp.	<abs	16..	....	...>						
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3		0010	0000	11Dm	<#8.	...>								
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5		0011	1101	0bp.	<abs	16..	....	...>						

Branch instructions

Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	--	--	--	--	3	2/3			1001	000H	<d4>									*1
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	--	--	--	--	4	2/3			1000	1010	<d7.	...H								*2
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	--	--	--	--	5	2/3			1001	1010	<d11	....	...H							*3
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	--	--	--	--	3	2/3			1001	001H	<d4>									1
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	--	--	--	--	4	2/3			1000	1011	<d7.	...H								*2
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	--	--	--	--	5	2/3			1001	1011	<d11	....	...H							*3
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	--	--	--	--	4	2/3			1000	1000	<d7.	...H								*2
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	--	--	--	--	5	2/3			1001	1000	<d11	....	...H							*3
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	--	--	--	--	4	2/3			1000	1100	<d7.	...H								*2
	BCC label	if(CF=0), PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	--	--	--	--	5	2/3			1001	1100	<d11	....	...H							*3
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	--	--	--	--	4	2/3			1000	1101	<d7.	...H								*2
	BCS label	if(CF=1), PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	--	--	--	--	5	2/3			1001	1101	<d11	....	...H							*3
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	--	--	--	--	4	2/3			1000	1110	<d7.	...H								*2
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	--	--	--	--	5	2/3			1001	1110	<d11	....	...H							*3
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	--	--	--	--	4	2/3			1000	1111	<d7.	...H								*2
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	--	--	--	--	5	2/3			1001	1111	<d11	....	...H							*3
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0001	<d7.	...H								*2

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	Re-peat	Exten-sion	Machine Code											Notes
			VF	NF	CF	ZF					1	2	3	4	5	6	7	8	9	10	11	
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0001	<d11	....	...H						*3
	BHI label	if(CFIZF=0),PC+5+d7(label)+H→PC if(CFIZF=1), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0010	<d7.	...H							*2
	BHI label	if(CFIZF=0),PC+6+d11(label)+H→PC if(CFIZF=1), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0010	<d11	....	...H						*3
	BLS label	if(CFIZF=1),PC+5+d7(label)+H→PC if(CFIZF=0), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0011	<d7.	...H							*2
	BLS label	if(CFIZF=1),PC+6+d11(label)+H→PC if(CFIZF=0), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0011	<d11	....	...H						*3
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0100	<d7.	...H							*2
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0100	<d11	....	...H						*3
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0101	<d7.	...H							*2
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0101	<d11	....	...H						*3
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0110	<d7.	...H							*2
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0110	<d11	....	...H						*3
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0111	<d7.	...H							*2
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0111	<d11	....	...H						*3
	BRA label	PC+3+d4(label)+H→PC	--	--	--	--	3	3				1110	111H	<d4>								*1
	BRA label	PC+4+d7(label)+H→PC	--	--	--	--	4	3				1000	1001	<d7.	...H							*2
	BRA label	PC+5+d11(label)+H→PC	--	--	--	--	5	3				1001	1001	<d11	....	...H						*3
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4				1100	10Dm	<#8.	...>	<d7.	...H					*2
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4				1101	10Dm	<#8.	...>	<d7.	..H>					*2
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0000	0bp.	<abs	8..>	<d7.	...H					*2
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0000	1bp.	<abs	8..>	<d11	....	...H				*3

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0100	0bp.	<io8	...>	<d7.	...H					*1
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0100	1bp.	<io8	...>	<d11	....	...H				*2
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8			0011	1110	0bp.	<abs	16..	....	...>	<d7.	...H			*1
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8			0011	1110	1bp.	<abs	16..	....	...>	<d11	....	...H		*2
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7			0011	0001	0bp.	<abs	8..>	<d7.	...H					*1
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7			0011	0001	1bp.	<abs	8..>	<d11	....	...H				*2
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7			0011	0101	0bp.	<io8	...>	<d7.	...H					*1
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7			0011	0101	1bp.	<io8	...>	<d11	....	...H				*2
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8			0011	1111	0bp.	<abs	16..	....	...>	<d7.	...H			*1
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8			0011	1111	1bp.	<abs	16..	....	...>	<d11	....	...H		*2
JMP	JMP (An)	0→PC.17-16,An→PC.15-0,0→PC.H	---	---	---	---	3	4			0010	0001	00A0									
	JMP label	abs18(label)+H→PC	---	---	---	---	7	5			0011	1001	0aaH	<abs	18.b	p15~	0..>					*5
JSR	JSR (An)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 0→PC.bp17-16 An→PC.bp15-0,0→PC.H	---	---	---	---	3	7			0010	0001	00A1									
	JSR label	SP-3→SP,(PC+5).bp7-0→mem8(SP) (PC+5).bp15-8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+5).bp17-16→mem8(SP+2).bp1-0 PC+5+d12(label)+H→PC	---	---	---	---	5	6			0001	000H	<d12	....	...>							*3
	JSR label	SP-3→SP,(PC+6).bp7-0→mem8(SP) (PC+6).bp15-8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+6).bp17-16→mem8(SP+2).bp1-0 PC+6+d16(label)+H→PC	---	---	---	---	6	7			0001	001H	<d16	....	....	...>						*4
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+7).bp17-16→mem8(SP+2).bp1-0 abs18(label)+H→PC	---	---	---	---	7	8			0011	1001	1aaH	<abs	18.b	p15~	0..>					*5
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 mem8(x'004080+tbl4<<2)→PC.bp7-0 mem8(x'004080+tbl4<<2+1)→PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp1-0→ PC.bp17-16	---	---	---	---	3	9			1111	1110	<t4>									
NOP	NOP	PC+2→PC	---	---	---	---	2	1	○		0000	0000										

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
RTS	RTS	mem8(SP)→(PC).bp7-0 mem8(SP+1)→(PC).bp15-8 mem8(SP+2).bp7→(PC).H mem8(SP+2).bp1-0→(PC).bp17-16 SP+3→SP	---	---	---	---	2	7			0000 0001											
RTI	RTI	mem8(SP)→PSW mem8(SP+1)→(PC).bp7-0 mem8(SP+2)→(PC).bp15-8 mem8(SP+3).bp7→(PC).H mem8(SP+3).bp1-0→(PC).bp17-16 mem8(SP+4)→HA-l mem8(SP+5)→HA-h SP+6→SP	●	●	●	●	2	11			0000 0011											
Contorl instructions																						
REP	REP imm3	imm3-1→RPC	---	---	---	---	3	2			0010 0001 1rep											*1

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101C Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions		replaced instructions		remarks
INC	Dn	ADD	1,Dn	
DEC	Dn	ADD	-1,Dn	
INC	An	ADDW	1,An	
DEC	An	ADDW	-1,An	
INC2	An	ADDW	2,An	
DEC2	An	ADDW	-2,An	
CLR	Dn	SUB	Dn,Dm	n=m
ASL	Dn	ADD	Dn,Dm	n=m
LSL	Dn	ADD	Dn,Dm	n=m
ROL	Dn	ADDC	Dn,Dm	n=m
NEG	Dn	NOT ADD	Dn 1,Dn	
NOPL		MOVW	DWn,DWm	n=m
MOV	(SP),Dn	MOV	(0,SP),Dn	
MOV	Dn,(SP)	MOV	Dn,(0,SP)	
MOVW	(SP),DWn	MOVW	(0,SP),DWn	
MOVW	DWn,(SP)	MOVW	DWn,(0,SP)	
MOVW	(SP),An	MOVW	(0,SP),An	
MOVW	An,(SP)	MOVW	An,(0,SP)	

Ver3.2(2002.01.31)

14-4 Instruction Map

MN101C SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nible\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2		BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3		BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

Extension code: b'0011'

2nd nibble\ 3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)			CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

Ver2.1(2001.03.26)

14-5 Special Function Registers List

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F00'	CPUM	-	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0	II - 23
		Set always "0".	Devision Rate Setup		Internal System Clock Setup	STOP mode Setup	HALT mode Setup	Oscillation Control		
X'3F01'	MEMCTR	IOW1	IOW0	IVBM	EXMEM	RESERVED	IRWE	RESERVED	RESERVED	II - 16
		I/O Wait Setup		Interuupt Vector Address	Set always "0".	Set always "1".	Software Write Setup	Set always "11".		
X'3F02'	WDCTR	-	-	WDTC2	WDTC1	WDTC0	WDTS1	WDTS0	WDEN	IX - 3
				The lowest value for WDT clear setup			Watchdog Time-out period Setup		WDT Activation	
X'3F03'	DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-	II - 28 X - 3
		P06 Output Selection	Buzzer Output Frequency Setup			Oscillation Stabilization Wait Cycle Setup				
X'3F10'	P0OUT	-	P0OUT6	-	-	-	P0OUT2	P0OUT1	P0OUT0	IV - 7
		Port 0 Output Data								
X'3F11'	P1OUT	-	-	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	IV - 11
		Port 1 Output Data								
X'3F12'	P2OUT	P2OUT7	-	-	-	-	-	-	-	IV - 15
		Port 2 Output Data								
X'3F13'	P3OUT	-	-	-	-	P3OUT3	P3OUT2	P3OUT1	P3OUT0	IV - 18
		Port 3 Output Data								
X'3F15'	P5OUT	-	-	-	-	P5OUT3	P5OUT2	P5OUT1	P5OUT0	IV - 22
		Port 5 Output Data								
X'3F16'	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	IV - 26
		Port 6 Output Data								
X'3F17'	P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	IV - 31
		Port 7 Output Data								
X'3F18'	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV - 36
		Port 8 Output Data								
X'3F1E'	P6SYO	P6SYO7	P6SYO6	P6SYO5	P6SYO4	P6SYO3	P6SYO2	P6SYO1	P6SYO0	IV - 27
		Port 6 Synchronous Output Control								
X'3F20'	P0IN	-	P0IN6	-	-	-	P0IN2	P0IN1	P0IN0	IV - 7
		Port 0 Input Data								
X'3F21'	P1IN	-	-	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	IV - 11
		Port 1 Input Data								
X'3F22'	P2IN	P2IN7	-	-	-	-	P2IN2	P2IN1	P2IN0	IV - 15
		Port 2 Input Data								
X'3F23'	P3IN	-	-	-	-	P3IN3	P3IN2	P3IN1	P3IN0	IV - 18
		Port 3 Input Data								

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F25'	P5IN	-	-	-	-	P5IN3	P5IN2	P5IN1	P5IN0	IV - 22
		Port 5 Input Data								
X'3F26'	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	IV - 26
		Port 6 Input Data								
X'3F27'	P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	IV - 31
		Port 7 Input Data								
X'3F28'	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	IV - 36
		Port 8 Input Data								
X'3F2A'	PAIN	-	-	-	-	PAIN3	PAIN2	PAIN1	PAIN0	IV - 40
		Port A Input Data								
X'3F2E'	FLOAT	-	PARDWN	P7RDWN	P6RDWN	-	-	SYOEVS1	SVOEVS0	IV - 27,32,41
			PA Pull up/down Resistor Selection	P7 Pull up/down Resistor Selection	P6 Pull up/down Resistor Selection			P6 Synchronous Output Event Selection		
X'3F2F'	P1OMD	-	-	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0	IV - 12
				I/O Port, Timer 8 Output Selection	I/O Port, Timer 7 Output Selection	I/O Port, Timer 3 Output Selection	I/O Port, Timer 2 Output Selection	I/O Port, Timer 1 Output Selection	I/O Port, Timer 0 Output Selection	
X'3F30'	P0DIR	-	P0DIR6	-	-	-	P0DIR2	P0DIR1	P0DIR0	IV - 7
		Port 0 I/O Derection Control								
X'3F31'	P1DIR	-	-	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	IV - 11
		Port 1 I/O Derection Control								
X'3F33'	P3DIR	-	-	-	-	P3DIR3	P3DIR2	P3DIR1	P3DIR0	IV - 18
		Port 3 I/O Derection Control								
X'3F35'	P5DIR	-	-	-	-	P5DIR3	P5DIR2	P5DIR1	P5DIR0	IV - 22
		Port 5 I/O Derection Control								
X'3F36'	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	IV - 26
		Port 6 I/O Derection Control								
X'3F37'	P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	IV - 31
		Port 7 I/O Derection Control								
X'3F38'	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	IV - 36
		Port 8 I/O Derection Control								
X'3F3A'	PAIMD	-	-	-	-	PAIMD3	PAIMD2	PAIMD1	PAIMD0	IV - 40
		I/O Port, Analog n Input Pin Selection								
X'3F3E'	P6IMD	P6KYEN7	P6KYEN6	P6KYEN5	P6KYEN4	P6KYEN3	P6KYEN2	P6KYEN1	P6KYEN0	III - 41
		P67 KEY Interrupt Selection	P66 KEY Interrupt Selection	P65 KEY Interrupt Selection	P64 KEY Interrupt Selection	P63 KEY Interrupt selection	P62 KEY Interrupt Selection	P61 KEY Interrupt Selection	P60 KEY Interrupt Selection	
X'3F3F'	P5OMD	-	-	-	-	P5OMD3	P5OMD2	P5OMD1	P5OMD0	IV - 23
						I/O Port, Timer 8 Output Selection	I/O Port, Timer 2 Output Selection	I/O Port, Timer 7 Output Selection	I/O Port, Timer 0 Output Selection	

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F40'	P0PLU	-	P0PLU6	-	-	-	P0PLU2	P0PLU1	P0PLU0	IV - 7
		Port 0 Pull-up Resistor ON / OFF Control								
X'3F41'	P1PLU	-	-	P1PLU5	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	IV - 11
		Port 1 Pull-up Resistor ON / OFF Control								
X'3F42'	P2PLU	-	-	-	-	-	P2PLU2	P2PLU1	P2PLU0	IV - 15
		Port 2 Pull-up Resistor ON / OFF Control								
X'3F43'	P3PLU	-	-	-	-	P3PLU3	P3PLU2	P3PLU1	P3PLU0	IV - 18
		Port 3 Pull-up Resistor ON / OFF Control								
X'3F45'	P5PLU	-	-	-	-	P5PLU3	P5PLU2	P5PLU1	P5PLU0	IV - 22
		Port 5 Pull-up Resistor ON / OFF Control								
X'3F46'	P6PLUD	P6PLUD7	P6PLUD6	P6PLUD5	P6PLUD4	P6PLUD3	P6PLUD2	P6PLUD1	P6PLUD0	IV - 26
		Port 6 Pull-up/pull-down Resistor ON / OFF Control								
X'3F47'	P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0	IV - 31
		Port 7 Pull-up/pull-down Resistor ON / OFF Control								
X'3F48'	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	IV - 36
		Port 8 Pull-up Resistor ON / OFF Control								
X'3F4A'	PAPLUD	-	-	-	-	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	IV - 40
		Port A Pull-up/pull-down Resistor ON / OFF Control								
X'3F50'	TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	VI - 9
		Timer 0 Binary Coutner								
X'3F51'	TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	VI - 9
		Timer 1 Binary Coutner								
X'3F52'	TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	VI - 8
		Timer 0 Compare Register								
X'3F53'	TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	VI - 8
		Timer 1 Compare Register								
X'3F54'	TM0MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0	VI - 10
				Pulse Width Measure Control	Timer 0 Operation Mode Selection	Timer 0 Count countrol	Clock Source Selection			
X'3F55'	TM1MD	-	-	-	TM1CAS	TM1EN	TM1CK2	TM1CK1	TM1CK0	VI - 11
					Timer 1 Operation Mode Selection	Timer 1 Count Countrol	Clock Source Selection			
X'3F56'	CK0MD	-	-	-	-	-	TM0PSC1	TM0PSC0	TM0BAS	V - 7
							Count Clock Selection (Prescaler Output)			
X'3F57'	CK1MD	-	-	-	-	-	TM1PSC1	TM1PSC0	TM1BAS	V - 7
							Count Clock Selection (Prescaler Output)			

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F58'	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	VI - 9
		Timer 2 Binary Counter								
X'3F59'	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	VI - 9
		Timer 3 Binary Counter								
X'3F5A'	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	VI - 8
		Timer 2 Compare Register								
X'3F5B'	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	VI - 8
		Timer 3 Compare Register								
X'3F5C'	TM2MD	TM2ADD2	TM2ADD1	TM2MOD	TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0	VI - 12
		Position of Additional Pulse		Pulse Width Measure Control	Timer 2 Operation Mode Selection	Timer 2 Count Control	Clock Source Selection			
X'3F5D'	TM3MD	-	-	-	TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0	VI - 13
					Timer 3 Operation Mode Selection	Timer 3 Count Control	Clock Source Selection			
X'3F5E'	CK2MD	-	-	-	-	-	TM2PSC1	TM2PSC0	TM2BAS	V - 8
							Count Clock Selection (Prescaler Output)			
X'3F5F'	CK3MD	-	-	-	-	-	TM3PSC1	TM3PSC0	TM3BAS	V - 8
							Count Clock Selection (Prescaler Output)			
X'3F68'	TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	VIII - 5
		Timer 6 Binary Counter								
X'3F69'	TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	VIII - 5
		Timer 6 Compare Register								
X'3F6A'	TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0	VIII - 6
		Timer 6 Binary Counter Clear Selection	Time Base Interrupt Cycle Selection			Timer 6 Clock Source Selection			Timer Base Timer Clock Source Selection	
X'3F6B'	TBCLR	-	-	-	-	-	-	-	-	VIII - 5
		Time Base Timer Clear Register (Write Only)								
X'3F6E'	RMCTR	-	-	-	TM0RM	RMOEN	-	RMDTY0	RMBTMS	VI - 14
					P10 Special Function Output Selection	Remote Control Carrier Output Enable		Remote Control Carrier Output Duty Selection	Remote Control Carrier Base Timer Selection	
X'3F6F'	PSCMD	-	-	-	-	-	-	-	PSCEN	V - 6
									Prescaler Operation Enable	
X'3F70'	TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	VII - 8
		Timer 7 Binary Counter Lower 8 Bit								
X'3F71'	TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	VII - 8
		Timer 7 Binary Counter Upper 8 Bit								
X'3F72'	TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	VII - 6
		Timer 7 Compare Register 1 Lower 8 Bit								

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F73'	TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	VII - 6
		Timer 7 Compare Register 1 Upper 8 Bit								
X'3F74'	TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	VII - 7
		Timer 7 Preset Register 1 Lower 8 Bit								
X'3F75'	TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	VII - 7
		Timer 7 Preset Register 1 Upper 8 Bit								
X'3F76'	TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	VII - 9
		Timer 7 Input Capture Register Lower 8 Bit								
X'3F77'	TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	VII - 9
		Timer 7 Input Capture Register Upper 8 Bit								
X'3F78'	TM7MD1	RESERVED	RESERVED	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0	VII - 10
		Set always "0".		Timer Output Reset Control	Timer 7 Count Control	Count Clock Selection		Clock Source Selection		
X'3F79'	TM7MD2	T7ICEDG	T7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0	VII - 11
		Capture Trigger Edge Selection	PWM Mode Selection	Timer 7 Counter Clear Factor Selection	Timer Output Waveform Selection	Timer 7 Interrupt Factor Selection	Input Capture Operation Enable	Capture Trigger Selection		
X'3F7A'	TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	VII - 6
		Timer 7 Compare Register 2 Lower 8 Bit								
X'3F7B'	TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	VII - 6
		Timer 7 Compare Register 2 Upper 8 Bit								
X'3F7C'	TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	VII - 7
		Timer 7 Preset Register 2 Lower 8 Bit								
X'3F7D'	TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	VII - 7
		Timer 7 Preset Register 2 Upper 8 Bit								
X'3F80'	TM8BCL	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0	VII - 8
		Timer 8 Binary Counter Lower 8 Bit								
X'3F81'	TM8BCH	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0	VII - 8
		Timer 8 Binary Counter Upper 8 Bit								
X'3F82'	TM8OC1L	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0	VII - 6
		Timer 8 Compare Register 1 Lower 8 Bit								
X'3F83'	TM8OC1H	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0	VII - 6
		Timer 8 Compare Register 1 Upper 8 Bit								
X'3F84'	TM8PR1L	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR1L3	TM8PR1L2	TM8PR1L1	TM8PR1L0	VII - 7
		Timer 8 Preset Register 1 Lower 8 Bit								
X'3F85'	TM8PR1H	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0	VII - 7
		Timer 8 Preset Register 1 Upper 8 Bit								

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F86'	TM8ICL	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0	VII - 9
		Timer 8 Input Capture Register Lower 8 Bit								
X'3F87'	TM8ICH	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0	VII - 9
		Timer 8 Input Capture Register Upper 8 Bit								
X'3F88'	TM8MD1	RESERVED	TM8CAS	TM8CL	TM8EN	TM8PS1	TM8PS0	TM8CK1	TM8CK0	VII - 12
		Set always "0".	Timer 7, 8 Cascade Control	Timer Output Reset Control	Timer 8 Count Control	Count Clock Selection		Clock Source Selection		
X'3F89'	TM8MD2	TM8ICEDG	RESERVED	TM8BCR	TM8PWM	TM8IRS1	TM8ICEN	TM8ICT1	TM8ICT0	VII - 13
		Capture Trigger Edge Selection	Set always "0".	Timer 8 Counter Clear Factor Selection	Timer Output Waveform Selection	Timer 8 Interrupt Factor Selection	Input Capture Operation Enable	Capture Trigger Selection		
X'3F8E'	NFCTR	P21IM	NF1SCK1	NF1SCK0	NF1EN	-	NF0SCK1	NF0SCK0	NF0EN	III - 40
		ACZ Input Enable	IRQ1/Noise Filter Sampling Cycle Selection		IRQ1/Noise Filter Operation Setup		IRQ0/Noise Sampling Cycle Selection		IRQ0/Noise Filter Operation Setup	
X'3F8F'	EDGDT	-	-	-	-	-	EDGSEL2	-	-	III - 41
						Set always "0".	IRQ2 both edge Interrupt Operation Setup			
X'3F90'	SC0MD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	XI - 6
		Transmission /Reception Data Edge Selection	Reception Data Polarity Change	Reception Data Polarity Change	Specify First Bit To be Transferred	Start Condition Selection	Synchronous Serial Transfer Bit Count Selection			
X'3F91'	SC0MD1	SC0IOM	SC0SBTS	SC0SBIS	SC0SBOS	SC0CKM	SC0MST	-	SC0CMD	XI - 7
		Serial Data Input Selection	SBT Pin Function Selection	Serial Input Control	SBO Pin Function Selection	Transfer Clock Divided by 8 Selection	Clock Master/Slave Selection		Synchronous Serial/ Duplex UART Selection	
X'3F92'	SC0MD2	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE	XI - 8
		Specify Frame Mode		Added Bit Specify		Parity Enable		Break Status Reception Monitor	Break Status Transmit Control	
X'3F93'	SC0MD3	SC0TBSY	SC0RBSY	SC0TEMP	SC0REMP	SC0FEF	SC0PEK	SC0ORE	SC0ERE	XI - 9
		Serial Bus Status	Serial Bus Status	Transmission Buffer Empty flag	Reception Buffer Empty flag	Frame Error Detection	Parity Error Detection	Overrun Error Detection	Error Monitor Flag	
X'3F94'	RXBUF0	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00	XI - 5
		Serial Interface 0 Reception Buffer								
X'3F95'	TXBUF0	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00	XI - 5
		Serial Interface 0 Transmission Buffer								
X'3F96'	SC0ODC	-	-	-	-	-	-	SC0ODC1	SC0ODC0	XI - 10
								P02 N-ch Open Drain Control	P00 N-ch Open Drain Control	
X'3F97'	SC0CKS	-	-	-	-	-	SC0PSC2	SC0PSC1	SC0PSC0	V - 9 XI - 11
							Transmission Clock Selection (Prescaler Output)			
X'3FB0'	ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	-	-	-	XII - 5
		Sample Hold Time		Conversion Clock		A/D Rudder Resistance Control				
X'3FB1'	ANCTR1	-	-	-	-	RESERVED	RESERVED	ANCHS1	ANCHS0	XII - 6
						Set always "0".		Analog Input Channel		
X'3FB2'	ANCTR2	ANST	RESERVED	-	-	-	-	-	-	XII - 6
		A/D Conversion Status	Set always "0".							

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FB3'	ANBUF0	ANBUF07	ANBUF06	-	-	-	-	-	-	XII - 7
		A/D Conversion Data Storage Register (Lower 2 Bits)								
X'3FB4'	ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	XII - 7
		A/D Conversion Data Storage Register (Upper 8 Bits)								
X'3FD9'	LCDMD1	LCDEN	LCREN	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	XIII - 6
		LCD Driver Circuit Start	Internal Voltage Divider Resistor Selection	LCD Display Duty Selection		LCD Clock Source Selection				
X'3FDA'	LCDMD2	COMSL3	COMSL2	COMSL1	COMSL0	-	-	UPCK	UPEN	IV - 19 XIII - 7
		COM3/Port 33 Selection	COM2/Port 32 Selection	COM1/Port 31 Selection	COM0/Port 30 Selection	Set always "0".		Voltage Booster Operation Speed Control	Voltage Booster Operation Star	
X'3FDB'	LCCTR1	LC1SL7	LC1SL6	LC1SL5	LC1SL4	LC1SL3	LC1SL2	LC1SL1	LC1SL0	IV - 33,37 XIII - 8
		SEG14-15/ Port 71-70 Selection	SEG12-13/ Port 73-72 Selection	SEG10-11/ Port 75-74 Selection	SEG8-9/ Port 77-76 Selection	SEG1-0/ Port 86-87 Selection	SEG3-2/ Port 84-85 Selection	SEG5-4/ Port 82-83 Selection	SEG7-6/ Port 80-81 Selection	
X'3FDC'	LCCTR2	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0	IV - 28 XIII - 9
		SEG23/Port 60 Selection	SEG22/Port 61 Selection	SEG21/Port 62 Selection	SEG20/Port 63 Selection	SEG19/Port 64 Selection	SEG18/Port 65 Selection	SEG17/Port 66 Selection	SEG16/Port 67 Selection	
X'3FE1'	NMICR	-	-	-	-	-	PIR	WDIR	RESERVED	III - 16
							Program Interrupt Request	Watchdog Interrupt Request	Set always "0".	
X'3FE2'	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR	III - 19
		Specify External Interrupt Level		External Interrupt Valid Edge				External Interrupt Enable	External Interrupt Request	
X'3FE3'	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR	III - 20
		Specify External Interrupt Level		External Interrupt Valid Edge				External Interrupt Enable	External Interrupt Request	
X'3FE4'	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR	III - 21
		Specify External Interrupt Level		External Interrupt Valid Edge				External Interrupt Enable	External Interrupt Request	
X'3FE6'	IRQ4ICR	IRQ4LV1	IRQ4LV0	-	-	-	-	IRQ4IE	IRQ4IR	III - 22
		Specify External Interrupt Level		Set always "0".				External Interrupt Enable	External Interrupt Request	
X'3FE9'	TM0ICR	TM0LV1	TM0LV0	-	-	-	-	TM0IE	TM0IR	III - 23
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FEA'	TM1ICR	TM1LV1	TM1LV0	-	-	-	-	TM1IE	TM1IR	III - 24
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FEB'	TM2ICR	TM2LV1	TM2LV0	-	-	-	-	TM2IE	TM2IR	III - 25
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FEC'	TM3ICR	TM3LV1	TM3LV0	-	-	-	-	TM3IE	TM3IR	III - 26
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FEF'	TM6ICR	TM6LV1	TM6LV0	-	-	-	-	TM6IE	TM6IR	III - 27
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FF0'	TBICR	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR	III - 28
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	

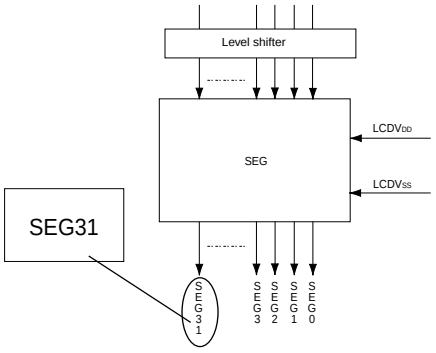
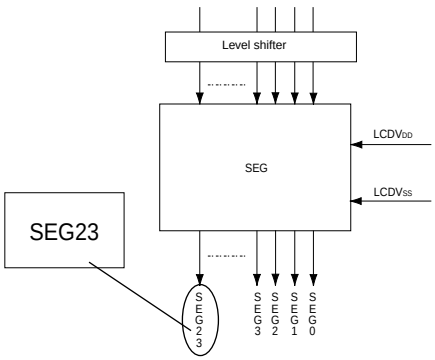
Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FF1'	TM7ICR	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR	III - 29
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FF2'	T7OC2ICR	T7OC2LV1	T7OC2LV0	-	-	-	-	T7OC2IE	T7OC2IR	III - 30
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FF3'	TM8ICR	TM8LV1	TM8LV0	-	-	-	-	TM8IE	TM8IR	III - 31
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FF5'	SC0RICR	SC0RLV1	SC0RLV0	-	-	-	-	SC0RIE	SC0RIR	III - 32
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FF6'	SC0TICR	SC0TLV1	SC0TLV0	-	-	-	-	SC0TIE	SC0TIR	III - 33
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	
X'3FFA'	ADICR	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR	III - 34
		Specify Interrupt Level						Interrupt Enable	Interrupt Request	

Record of Changes

MN101C527 LSI User's Manual Record of Changes (Ver.3.3 to Ver.3.4) (1/2)

Page	Section	Definiti-on	Details of Changes	
			PreviousEdition (Ver.3.3)	New Edition (Ver.3.4)
-	-	Deletion	Descriptions about TQFP064-P-1010B	-
1-3	Line 8-9	Addition	-	- Machine cycle (at 2-divide of crystal oscillation) High speed mode: 1.0 µs/ 2 MHz (2.0 V to 5.5 V) *1 Low speed mode: 62.5 µs / 32 kHz (2.0 V to 5.5 V) *1 *1: Minimum rating for EPROM vers. is 2.3 V to 5.5 V.
1-10	Table 1-3-2 (1/6)	Change	If a capacitor is to be inserted between NRST and VDD,it is recommended that a discharge diode be placed between NRST and VDD.	If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD.
1-28	Line 1	Change	Unused Pins (only for output)	Unused Pins (output exclusive pins and LCD output pins)
	Line 2	Change	Unused pins only for output should be open.	Set unused pins (output exclusive pins and LCD output pins) open.
2-12	Key mark	Addition	-	Set the MMOD pin always to "L" level.
2-19	Key mark	Addition	-	System clock (fs) changes depending on the CPU operation mode. It changes to fosc (high frequency) in NORMAL and HALT0 modes, and to fx (low frequency) in SLOW, IDLE and HALT1 modes.
2-22	Key mark	Addition	-	Insert three nop instructions right after the instruction of transition to HALT, SLOW modes.
3-3	Table 3-1-1	Change	Maskable interrupt Vector number: 2 to 28 Table address: xx'04008' to x'04070'	Maskable interrupt Vector number: 2 to 30 Table address: xx'04008' to x'04078'
3-6	Key mark	Addition	-	Write an address to which the RTI instruction is written to memory space of the vector addresss of reserved or unused instruction.
3-8	Key mark	Addition	-	When set as xxxLV1=1, xxxLV0=1, interrupt of the set interrupt vector address is disabled dispite of the values of xxxIE, XXXIR.
3-16	Key mark	Addition	-	This LSI generates non-maskable interrupt and sets the program interrupt request flag (PIR) at the same time before undefined instruction is exected. If setting of the PIR flag is detected in the non-maskable interrupt service routine, use the software reset which outputs "0" to the reset pin (P27).
	Caution	Addition	-	Once a non-maskable interrupt is generated and value of the WDIR turns to "1", the value does not return to "0" unless it is cleared by program.
3-17	Caution	Addition	-	Cautions about interrrupts generated by undefined instructions
3-43	Caution	Addition	-	Cautions for use of both edges interrupts
3-47	Key mark	Addition	-	When fosc/28, fosc/29 or fosc/210 is selected as a sampling cycle, set the PSCEN flag of the prescaler control register (PSCMD) to "1" for the prescaler to be in operating state in advance.
4-3	Key mark	Addition	-	How to determine pull-up / pull-down resistor values

MN101C527 LSI User's Manual Record of Changes (Ver.3.3 to Ver.3.4) (2/2)

Page	Section	Definiti-on	Details of Changes	
			PreviousEdition (Ver.3.3)	New Edition (Ver.3.4)
6-18	Key mark	Addition	-	When fx is selected as a count clock source and if binary counter value is read out during opeartion, the read value may be uncertain. To prevent this, select synchronous fx as a count clock source. To do so timer n counts up the binary counter with a signal that is sync with the system clock, and you can always read out correct value from the binary counter. But with synchronous fx, return from STOP/HALT modes is disabled.
6-25 7-27	Key mark	Addition	-	Compare register value calculation; Compare register value = $\frac{\text{Timer pulse output cycle}}{\text{Selected clock cycle x 2}}$ -1
6-42	Key mark	Addition	-	If you want to clear the binary counter by rewrite of the compare register value during cascade connection, set the TMnEN flag of the mode register of both upper / lower 8-bit timers to "0" to stop counting before rewrite.
6-35 11-11, 16,29, 35,40,48	Caution	Addition	-	When timer output is selected as serial interface transfer clock, select fosc as a clock source of the timer. If other clock is selected, normal transfer of serial interface data is not guaranteed.
7-15	Caution	Addition	-	Cautions about write timing to16-bit timer preset register
11-33	Caution	Change	Do not set as following combination; "no parity bit" to parity enable flag and "data 7 bits + stop 2 bits" to flame mode selection flag .	Do not set following flame modes when SC0NPE flag is "1" and parity bit is disabled, Character 7 bits + Stop 2 bits of the flame mode (Set the SC0FM1, SC0FM0 flags to "0, 1".) Character 7 bits + Stop 1 bit of the flame mode (Set the SC0FM1, SC0FM0 flags to "0, 0".)
11-47	Caution	Addition	-	Cautions about full-duplex UART communication using serial interface 0
13-3	Key mark	Addition	-	OFF the LCD and switch from segment output to port before transition to the CPU mode in which LCD operation is disabled, .
13-13	Figure 13-3-1	Change	Figure 13-3-1 LCD Power Section Block Diagram (3 times boost) 	Figure 13-3-1 LCD Power Section Block Diagram (3 times boost) 
Chapter 14	-	Deletion	Description about MN101CP52AHT, MPX-AP101C52-HC	-
14-5	Table 14-1-1	Addition	-	Oscillation characteristics Noise characteristics Operating tempreture
14-8	Key mark	Addition	-	The internal ROM space of this LSI starts from x'4000' .
14-14 to 14-19	14-3	Change	Instruction Set (Ver. 3.1)	Instruction Set (Ver. 3.2)

MN101C527 LSI User's Manual Record of Changes (Ver.3.2 to Ver.3.3)

Page	Section	Definiti-on	Details of Changes	
			PreviousEdition (Ver.3.2)	New Edition (Ver.3.3)
All chapters	-	Change	RST	NRST
1-31		Addition	-	1-8-5 Oscillation Pins
2-13	Cautions	Addition	-	The value of internal RAM is uncertain when power is applied to it. It needs to be initialized before it is used.
11-36		Addition	-	Description of transfer bit count of 7 bits data and the first transfer bit in UART communication is added
11-37		Delition	Following reference page guide is delited Transfer Bit Count and First Transfer Bit Refer to: XI-14 Reception Bit Count and First Transfer Bit Refer to: XI-14	-
13-1 | 13-4		Change		Organization of the section is changed.

MN101C527
LSI User's Manual

July, 2002 3rd Edition 4th Printing

Issued by Matsushita Electric Industrial Co., Ltd.

© Matsushita Electric Industrial Co., Ltd.

Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

Nagaokakyo, Kyoto 617-8520, Japan
Tel: (075) 951-8151
http://www.panasonic.co.jp/semicon/

SALES OFFICES

■ NORTH AMERICA

●U.S.A. Sales Office:

Panasonic Industrial Company [PIC]

• New Jersey Office:
Two Panasonic Way Secaucus, New Jersey 07094 U.S.A.
Tel: 1-201-348-5257 Fax:1-201-392-4652

• Chicago Office:
1707 N. Randall Road Elgin, Illinois 60123-7847 U.S.A.
Tel: 1-847-468-5720 Fax:1-847-468-5725

• Milpitas Office:
1600 McCandless Drive Milpitas, California 95035 U.S.A.
Tel: 1-408-942-2912 Fax:1-408-946-9063

• Atlanta Office:
1225 Northbrook Parkway Suite 1-151 Suwanee, GA 30024 U.S.A.
Tel: 1-770-338-6953 Fax:1-770-338-6849

• San Diego Office:
9444 Balboa Avenue, Suite 185, San Diego, California 92123 U.S.A.
Tel: 1-619-503-2903 Fax:1-858-715-5545

●Canada Sales Office:

Panasonic Canada Inc. [PCI]
5770 Ambler Drive 27 Mississauga, Ontario, L4W 2T3 CANADA
Tel: 1-905-238-2315 Fax:1-905-238-2414

■ LATIN AMERICA

●Mexico Sales Office:

Panasonic de Mexico, S.A. de C.V. [PANAMEX]
Amores 1120 Col. Del Valle Delegacion Benito Juarez C.P. 03100 Mexico, D.F. MEXICO
Tel: 52-5-488-1000 Fax:52-5-488-1073

• Guadalajara Office:
SUCURSAL GUADALAJARA
Av. Lazaro Cardenas 2305 Local G-102 Plaza Comercial Abastos; Col. Las Torres Guadalajara, Jal. 44920 MEXICO
Tel: 52-3-671-1205 Fax:52-3-671-1256

●Brazil Sales Office:

Panasonic do Brasil Ltda. [PANABRAS]
Caixa Postal 1641, Sao Jose dos Campos, Estado de Sao Paulo
Tel: 55-12-335-9000 Fax:55-12-331-3789

■ EUROPE

●Europe Sales Office:

Panasonic Industrial Europe GmbH [PIE]

• U.K. Sales Office:
Willoughby Road, Bracknell, Berks., RG12 8FP, THE UNITED KINGDOM
Tel: 44-1344-85-3671 Fax:44-1344-85-3853

• Germany Sales Office:
Hans-Pinsel-Strasse 2 85540 Haar, GERMANY
Tel: 49-89-46159-119 Fax:49-89-46159-195

■ ASIA

●Singapore Sales Office:

Panasonic Semiconductor of South Asia [PSSA]
300 Beach Road, #16-01, The Concourse, Singapore 199555 THE REPUBLIC OF SINGAPORE
Tel: 65-6390-3688 Fax:65-6390-3689

●Malaysia Sales Office:

Panasonic Industrial Company (M) Sdn. Bhd. [PICM]

• Head Office:
Tingkat 16B, Menara PKNS Petaling Jaya, No.17, Jalan Yong Shook Lin 46050 Petaling Jaya, Selangor Darul Ehsan, MALAYSIA
Tel: 60-3-7951-6601 Fax:60-3-7954-5968

• Penang Office:
Suite 20-07,20th Floor, MWE Plaza, No.8, Lebuh Farquhar,10200 Penang, MALAYSIA
Tel: 60-4-201-5113 Fax:60-4-261-9989

• Johore Sales Office:
Menara Pelangi, Suite8.3A, Level8, No.2, Jalan Kuning Taman Pelangi, 80400 Johor Bahru, Johor, MALAYSIA
Tel: 60-7-331-3822 Fax:60-7-355-3996

●Thailand Sales Office:

Panasonic Industrial (THAILAND) Ltd. [PICT]
252-133 Muang Thai-Phatra Complex Building, 31st Fl. Rachadaphisek Rd., Huaykwang, Bangkok 10320, THAILAND
Tel: 66-2-693-3428 Fax:66-2-693-3422

●Philippines Sales Office: [PISP]

Panasonic Indsutrial Sales Philippines Division of Matsushita Electric Philippines Corporation
102 Laguna Boulevard,Bo.Don Jose Laguna Technopark, Santa. Rosa, Laguna 4026 PHILIPPINES
Tel: 63-2-520-8615 Fax:63-2-520-8629

●India Sales Office:

National Panasonic India Ltd. [NPI]
E Block, 510, International Trade Tower Nehru Place, New Delhi_110019 INDIA
Tel: 91-11-629-2870 Fax:91-11-629-2877

●Indonesia Sales Office:

P.T.MET & Gobel [M&G]
JL. Dewi Sartika (Cawang 2) Jakarta 13630, INDONESIA
Tel: 62-21-801-5666 Fax:62-21-801-5675

●China Sales Office:

Panasonic Industrial (Shanghai) Co., Ltd. [PI(SH)]
Floor 6, Zhong Bao Mansion, 166 East Road Lujian Zui, PU Dong New District, Shanghai, 200120 CHINA
Tel: 86-21-5866-6114 Fax:86-21-5866-8000

Panasonic Industrial (Tianjin) Co., Ltd. [PI(TJ)]
Room No.1001, Tianjin International Building 75, Nanjin Road, Tianjin 300050, CHINA
Tel: 86-22-2313-9771 Fax:86-22-2313-9770

Panasonic SH Industrial Sales (Shenzhen) Co., Ltd. [PSI(SZ)]
7A-107, International Bussiness & Exhibition Centre, Futian Free Trade Zone, Shenzhen 518048, CHINA
Tel: 86-755-8359-8500 Fax:86-755-8359-8516

Panasonic Shun Hing Industrial Sales (Hong Kong) Co., Ltd. [PSI(HK)]
11th Floor, Great Eagle Center 23 Harbour Road, Wanchai, HONG KONG
Tel: 852-2529-7322 Fax:852-2865-3697

●Taiwan Sales Office:

Panasonic Industrial Sales (Taiwan) Co.,Ltd. [PIST]

• Head Office:
6F, 550, Sec. 4, Chung Hsiao E. RD. Taipei, 110, TAIWAN
Tel: 886-2-2757-1900 Fax:886-2-2757-1906

• Kaohsiung Office:
6th Floor, Hsin Kong Bldg. No.251, Chi Hsien 1st Road Kaohsiung 800, TAIWAN
Tel: 886-7-346-3815 Fax:886-7-236-8362

●Korea Sales Office:

Panasonic Industrial Korea Co., Ltd. [PIKL]
Kukje Center Bldg. 11th Fl., 191 Hangangro 2ga, Youngsan-ku, Seoul 140-702, KOREA
Tel: 82-2-795-9600 Fax:82-2-795-1542

050702

© Matsushita Electric Industrial Co., Ltd. 2002

Printed in JAPAN